Electrical Characterization of a 4H-SiC JFET Wafer: DC Parameter Variations for Extreme Temperature IC Design

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Abstract. This work reports DC electrical characterization of a 76 mm diameter 4H-SiC JFET test wafer fabricated as part of NASA's on-going efforts to realize medium-scale ICs with prolonged and stable circuit operation at temperatures as high as 500 °C. In particular, these measurements provide quantitative parameter ranges for use in JFET IC design and simulation. Larger than expected parameter variations were observed both as a function of position across the wafer as well as a function of ambient testing temperature from 23 °C to 500 °C.

Introduction

In order for SiC electronics to benefit applications in the harshest envisioned environments, circuit operation for thousands of hours or more in the demanding application conditions is necessary. The NASA Glenn Research Center previously has demonstrated prolonged and stable packaged operation of very simple (< 5 transistors) 6H-SiC junction field-effect transistor (JFET) integrated circuits (ICs) for thousands of hours at 500 °C in air ambient [1,2]. Others have demonstrated more complicated SiC ICs, but without reporting thousands of hours of stable electrical operation at 500 °C [3,4]. This work reports electrical characterization of a 76 mm diameter 4H-SiC JFET test wafer fabricated as part of NASA's on-going efforts to realize medium-scale ICs (>100 transistors/chip) with prolonged and stable circuit operation at ambient temperature (T) as high as 500 °C. In particular, these measurements provide quantitative DC parameter ranges for use in JFET IC design and simulation, both as a function of position across the wafer as well as a few initial measurements of parameter changes with T from 23 °C to 500 °C.

Experimental

All measurements were carried out on devices fabricated at NASA Glenn starting from a single 76-mm diameter 4H-SiC wafer with epilayers purchased in 2009 [5] (Fig. 1). The 4H-SiC JFET structure features dry-etch patterned p^+ gate and n-channel epilayers with gate length (L_G) and minimum feature size of 6 µm. In addition to a patterned high-dose ion implantation to facilitate n-layer ohmic contact formation, a self-aligned shallow N implant (3.6 x 10^{12} cm^{-2} at 70 keV) was performed at room temperature into surface-exposed n-epilayer regions to reduce parasitics [6].

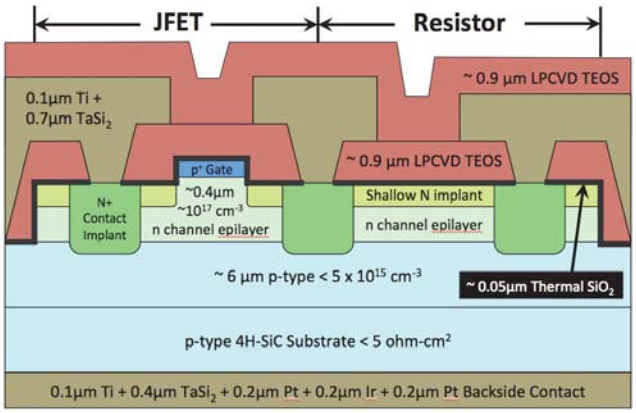

Fig. 1. Simplified cross-sectional schematic of NASA Glenn 4H-SiC JFET and resistor (sharing common n-type layer mesa).

Wafer mapping was carried out at T = 23 °C on a probing system using source-measure units for DC current vs. voltage (I-V) measurements. Data was collected from diagnostic process test chips arrayed across the wafer every 9 mm. Mapped test devices included W_G=12µm/L_G=6µm JFETs, L_R=120µm x W_R=12µm (= 10 squares) resistors, and 54 µm wide transmission line method (TLM) devices with 48 µm wide x 24 µm long contact openings at separation spacings of 12 µm, 66 µm, and 126 µm. Negative substrate bias was applied for most measurements consistent with the intended circuit approach of Krasowski [2,7]. Measured resistance (R) values were calculated from I-V slopes while JFET threshold voltages (V_T) were calculated from x-intercepts of the linear region of $\sqrt{I_D}$ (I_D = drain current) vs. gate voltage (V_G) plots at drain voltage (V_D) of 20V. After mapping, the wafer was diced into 3 mm x 3 mm chips. Three chips were then custom-packaged [8] and mounted in an oven and connected to outside-oven instruments via gold wires with fiberglass insulation for carrying out DC I-V measurements from 23 °C to 500 °C.

Results and Discussion

Room Temperature Wafer Mapping. Room temperature prober mapping reveals significant radial variation in n-channel electrical properties across the epi-wafer. Fig. 2 illustrates the variation of V_T measured from 12µm/6µm test JFETs across the wafer. The smallest V_T's (i.e., closest to 0 V) occur in the central region of the wafer, and significantly increase as position progresses outward towards the wafer edge. For the JFET structure of Fig. 1, V_T is determined by the n-channel epilayer immediately underneath the JFET gate. As there are no processing changes to this electrically critical region following epilayer growth (such as implantation or etching), the observed V_T variation directly reflects the variation in doping concentration and thickness of the as-grown n-channel epilayer. Therefore, the n-epilayer sheet charge density and conductivity (a function of n-epilayer doping x thickness product) in the wafer central region is significantly smaller than at the wafer periphery.

In contrast to measured V_T that is strictly a function of the as-grown epilayers, measured resistance values have additional dependence on post-epilayer processing such as ion implantation and contacts. Fig. 3 shows the measured variation in JFET drain-to-source resistance (R_{DS}) of the 12µm/6µm test JFETs, L_R=120µm x W_R=12µm resistors (R_{10}), and sheet resistance (R_{Sheet}) extracted from TLMs plotted as a function of radial distance from the wafer center. To better compare the magnitude of positional variation, plotted R values are respectively normalized to the statistical mean of resistance accumulated for each device type. Linear data fits for the respective device types are shown as dashed lines. The resistances exhibit spatial variation across the wafer generally consistent with the observed V_T variation, in which higher R values correspond to central wafer regions of less negative V_T (i.e., less n-epilayer conductivity).

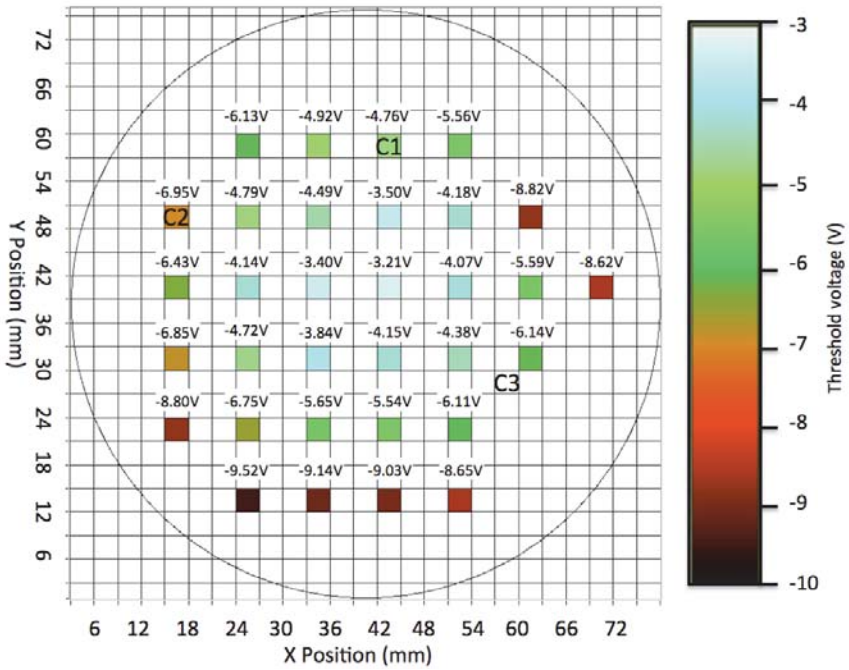

Fig. 2. Wafer map of 12µm/6µm JFET V_T measured at T=23 °C and $V_{Substrate}$ = -15 V. Locations of packaged chips C1, C2 & C3 are shown.

However, the spatial dependence of R_{10} and R_{Sheet} is significantly weaker than the spatial variation of R_{DS} (i.e., reduced slope in the linear fit dashed lines). This is inferred to arise from the shallow implant extending the entire length of TLMs and R_{10} resistors (Fig. 1) with good uniformity across the wafer surface, whereas R_{DS} is dominated by the spatially more-variant n-epilayer resistance of the JFET channel region that has no implant.

With the exception of two high-resistance outlier points, specific contact resistivity extracted from measured TLM data for the $Ti/TaSi_2$ contact [9] to high-dose N source/drain implanted regions ranged from 2 x 10^{-4} to 2 x 10^{-5} Ω-cm^2 and did not exhibit an experimentally significant trend as a function of wafer position. The fact that measured R_{10} is larger than 10 squares x TLM R_{Sheet} indicates that end resistance and contact resistance effects are non-negligible.

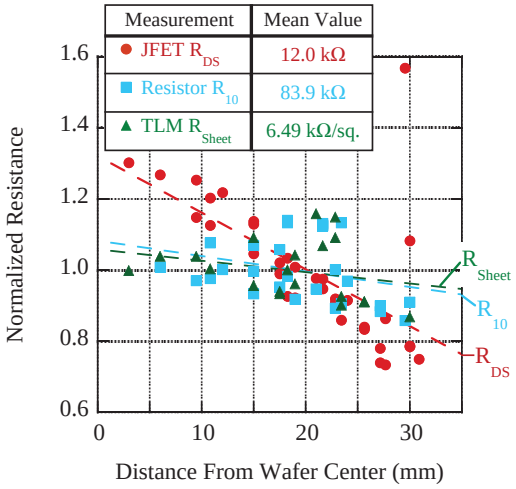

Fig. 3. Normalized measured resistances plotted as a function of distance from the wafer center.

Temperature Dependence of Packaged Devices. The ratio of transistor ON-state current to OFF-state current degrades with increasing T and often dictates maximum useful temperature of an IC technology for an application. Even at 500 °C, all three packaged 4H-SiC JFETs demonstrated OFF-state currents below 0.1 µA and ON to OFF state current ratios better than 900. Fig. 4 compares the turn-off characteristics of two packaged JFETs with significantly different W_G and V_T at 23 °C and 500 °C. V_T exhibited nearly linear change over this T range, from -4.47 V and –6.15 V at 23 °C to –5.06 V and –6.54 V at 500 °C for the respective W_G=12µm and W_G=192µm devices. Linear fits of V_T vs. T data (recorded at T = 23, 100, 200, 300, 400, and 500 °C) for these two JFETs yield slopes of -1.20 mV/°C and -0.796 mV/°C, respectively.

The changes observed in measured device resistance from 23 °C to 500 °C are comparatively illustrated in Fig. 5. For more clear comparison of relative change magnitudes, all values are plotted normalized to each respective device's measured value at 23 °C ($R_{23°C}$). Qualitatively consistent with prior understanding, resistances for all tested devices increase with temperature presumably due to declining electron mobility arising from increased thermal carrier scattering in the n-doped current-carrying device regions [10]. Importantly however, the resistor devices plotted in Fig. 5 exhibit substantially larger resistance increase (not far from 2X larger at 500 °C) with temperature than JFET devices, even for cases where the JFET and resistor physically reside on the same packaged die. Packaged TLM device behavior preliminarily indicates that this is caused by the greater temperature sensitivity of the n-type sheet resistance (epi with implant, see TLM R_{Sheet}, Fig. 5) relative to the JFET n-channel resistance (epi without implant). Specific contact resistivity, which changes only slightly from 300 °C to 500 °C (remaining near 4 x 10^{-4} Ω-cm^2), did not exhibit comparable temperature dependence as measured resistor values.

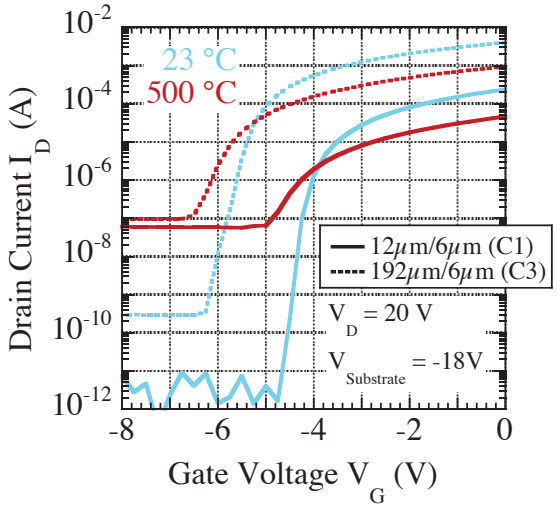

Fig. 4. Turn-off characteristics of two high-temperature packaged 4H-SiC JFETs at 23 °C and 500 °C. See Fig. 2 for wafer locations of chips C1 and C3.

The temperature-induced resistance increase of resistors (relative to room temperature R value) shown in Fig. 5 is significantly larger than reported in prior studies of similar 4H-SiC n-channel devices [10]. Furthermore, the increasing disparity between resistor R vs. JFET R at higher T is much greater than the negligible disparity obtained comparing very similar JFETs and resistors previously implemented in 6H-SiC [2]. As discussed in [2,7], a key basis for simplified design of SiC JFET ICs that function over an extremely broad temperature range without changes to input voltages is the fact that SiC resistors and JFETs should almost identically track in the magnitude of their conduction parameter changes with temperature. At a minimum, the larger disparities illustrated for high T in Fig. 5 are likely to undesirably increase the T dependence of simple analog inverting and differential amplifier sub-circuits. Digital logic chip functionality will be less affected than analog circuits due to the fact that logic circuit output voltages primarily rely on V_T and power supply voltages [2,7]. Further study is needed to elucidate the root physical mechanisms behind the larger than expected R value disparity with T. Until negated (perhaps) via processing changes, this R change disparity between device types at high T should be accounted for in modeling and design of extreme temperature 4H-SiC JFET ICs.

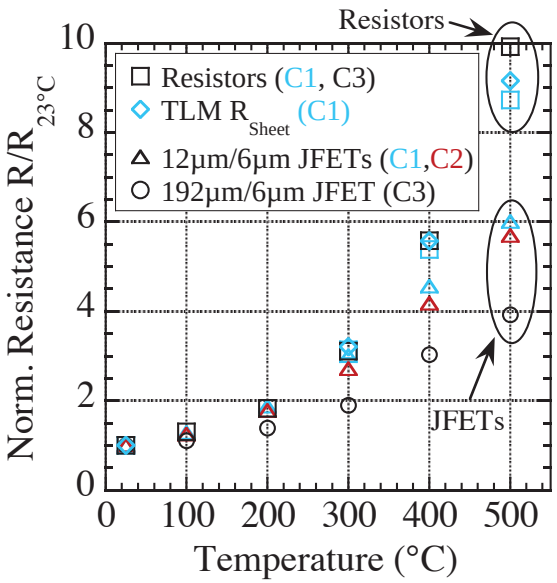

Fig. 5. Normalized resistance ($R/R_{23°C}$) of packaged devices measured vs. T with $V_{Substrate}$ = -18V. See Fig. 2 for wafer locations of chips C1, C2, and C3.

Summary

Important relative changes in DC parameters of epitaxial n-channel 4H-SiC JFETs and resistors as a function of wafer position and temperature have been measured. While parameter value spreads/changes measured in this work can be somewhat accommodated via circuit design and supply voltage adjustments, significantly reduced parameter variation would yield IC chips with more uniform electrical functionality regardless of temperature or chip location on the wafer.

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