STRS Waveform Porting for NASA's CoNNeCT Project

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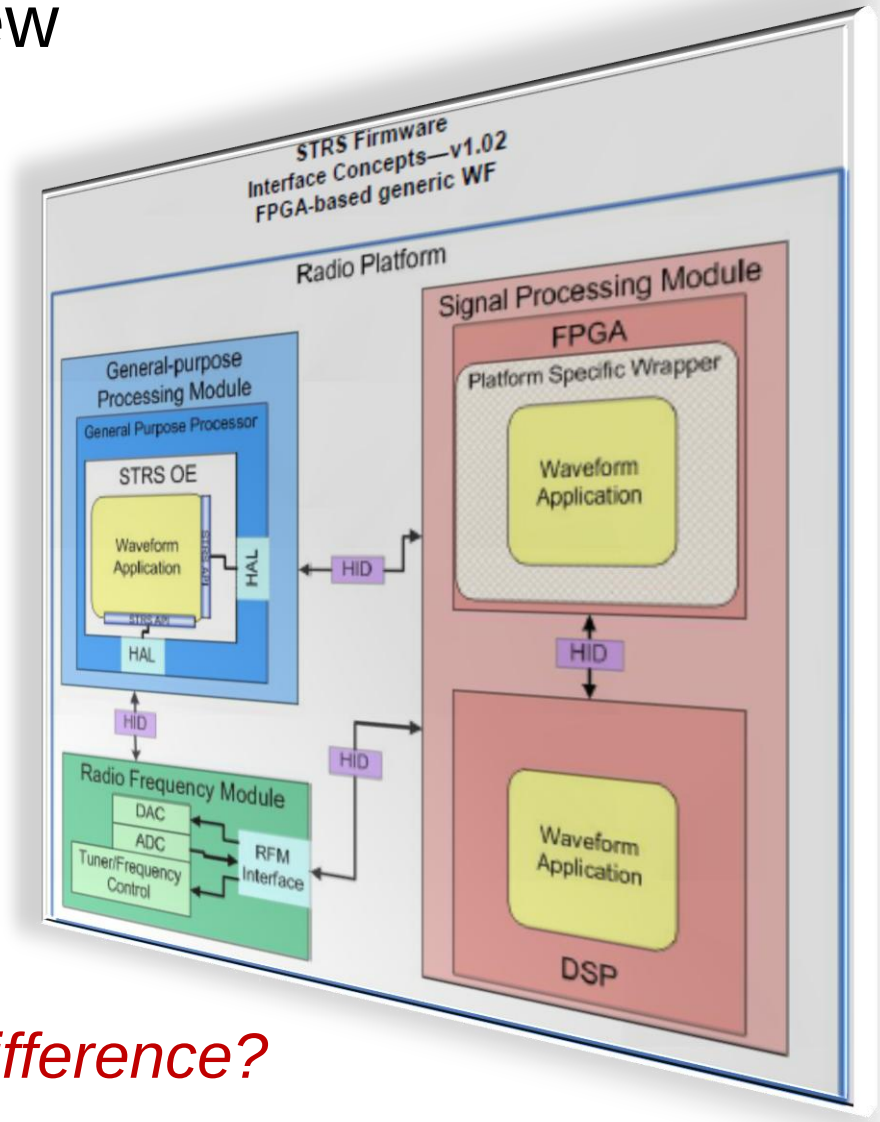
Dale Mortensen

Outline

- CoNNeCT project overview
- The Ported Waveform – TDRSS application
- "What is all this

  STRS stuff, anyhow?"
- Development approach
- Porting metrics & results



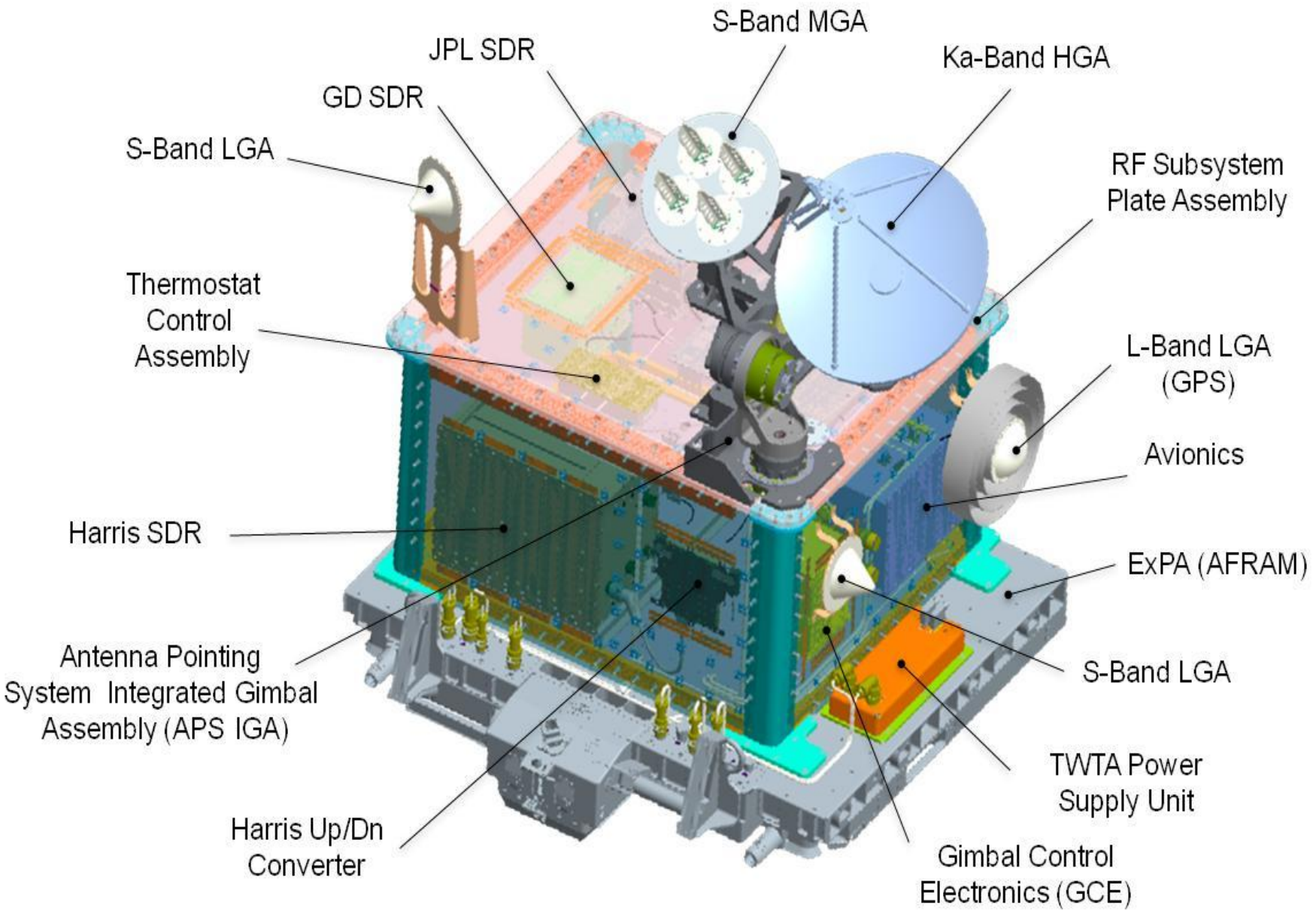
Does STRS really make a difference?

CoNNeCT Project Overview

Communications, Navigation, and Networking reConfigurable Testbed

- a.k.a. “Space Communications and Networking (SCAN) Testbed”
- International Space Station(ISS) Exterior Payload, scheduled to launch in 2012
- Investigating the application of SDRs to NASA Missions
- SDR technology development
- Validating future mission operational capabilities
- First flight for STRS

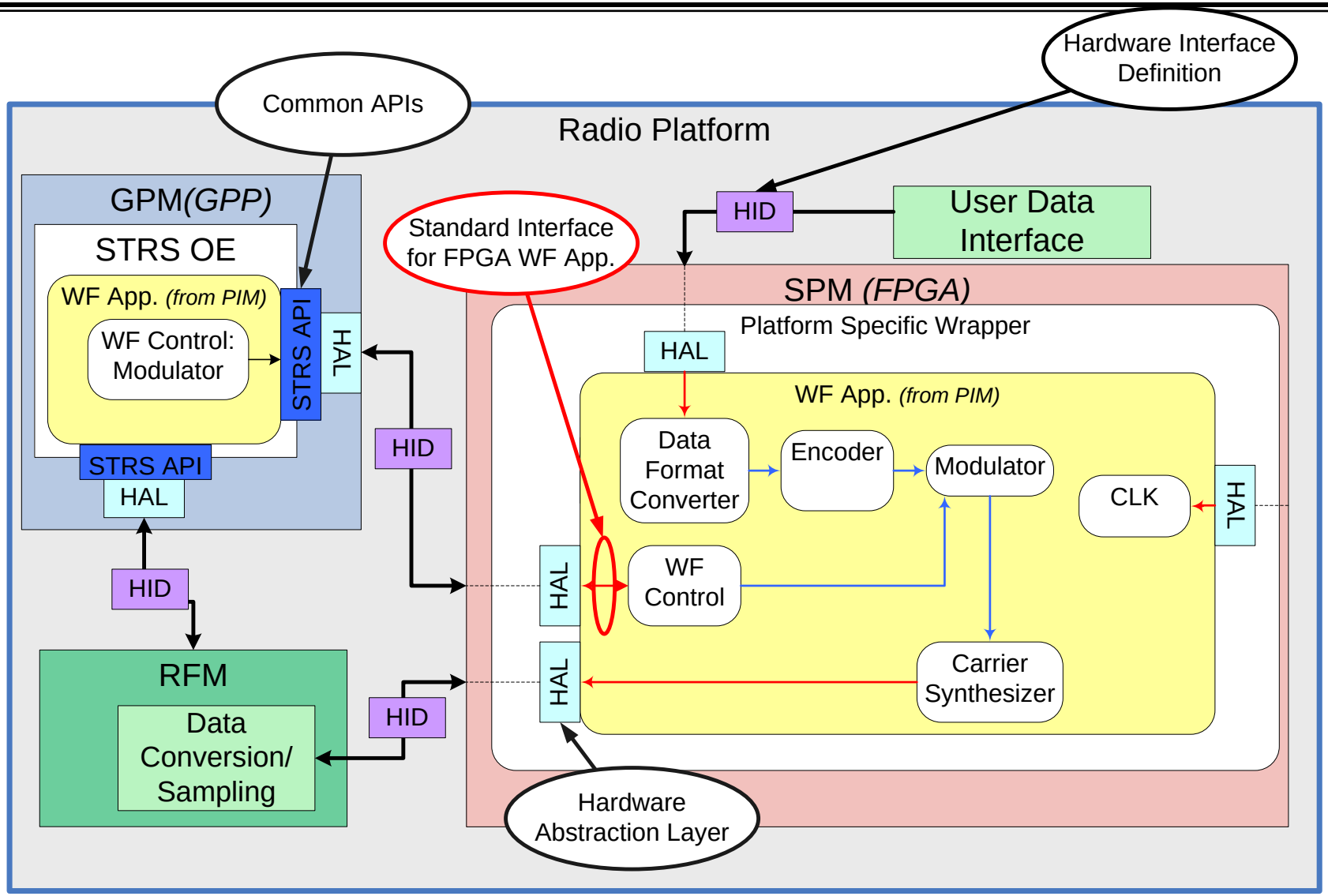
CoNNeCT Flight Payload



JPL Baseline Waveform Description

Description	**Transmit** (return link)	**Receive** (forward link)
Modulation	BPSK	
Spreading	Direct Sequence Spread Spectrum (PN Short code) (with bypass option for DG2)	
TDRSS functionality	Data Group 1, Mode 2 Data Group 2, non-coherent	
Forward Error Correction	½ rate convolutional encoding	½ rate Viterbi decoding
User Data Rates	24 kbps (spread), 192, 769 kbps (non-spread)	18 kbps (spread), 155, 769 kbps (non-spread)
Scrambling	IESS-308, V.35	
Data Formatting	NRZ-M	

Space Telecommunications Radio System



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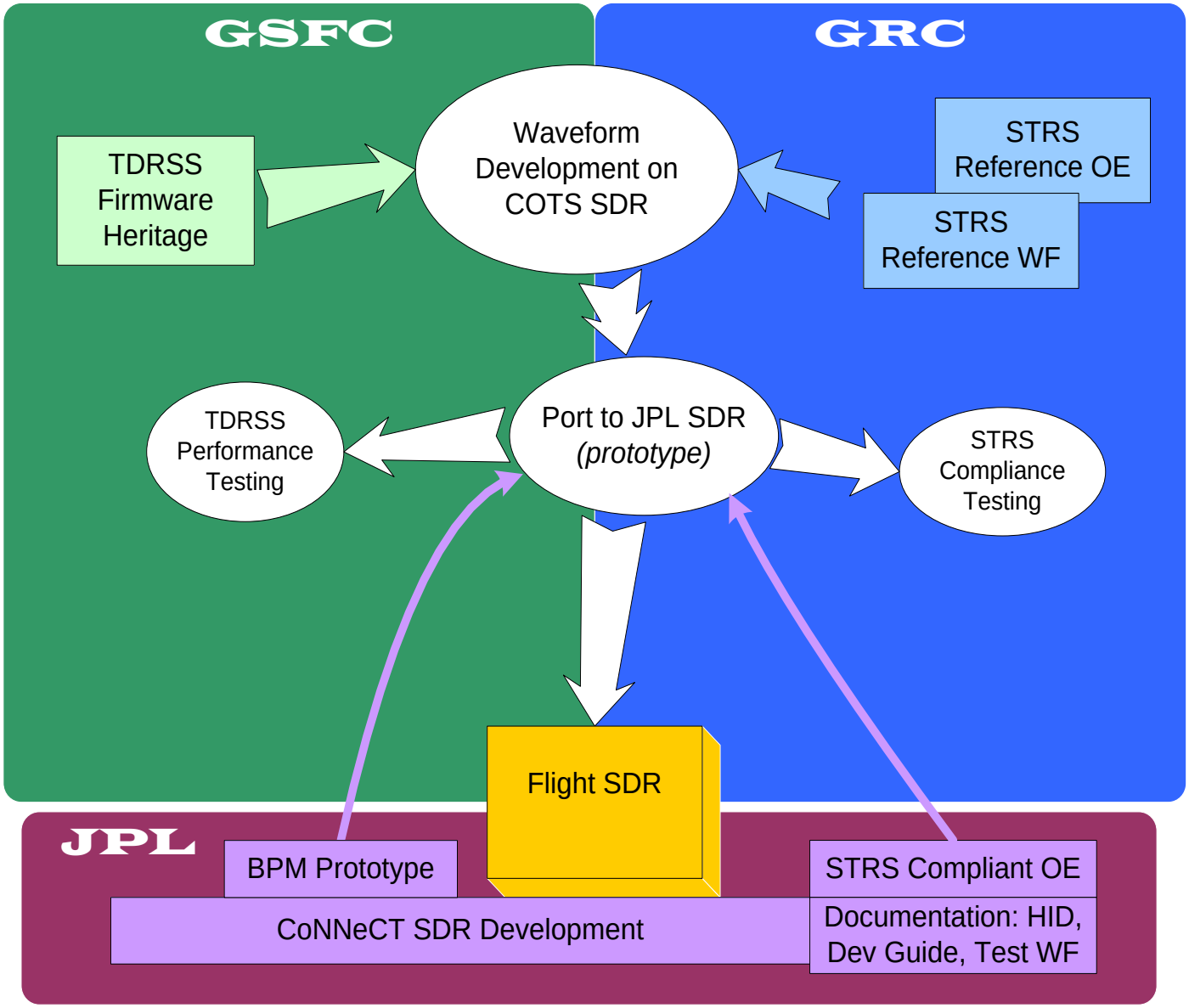
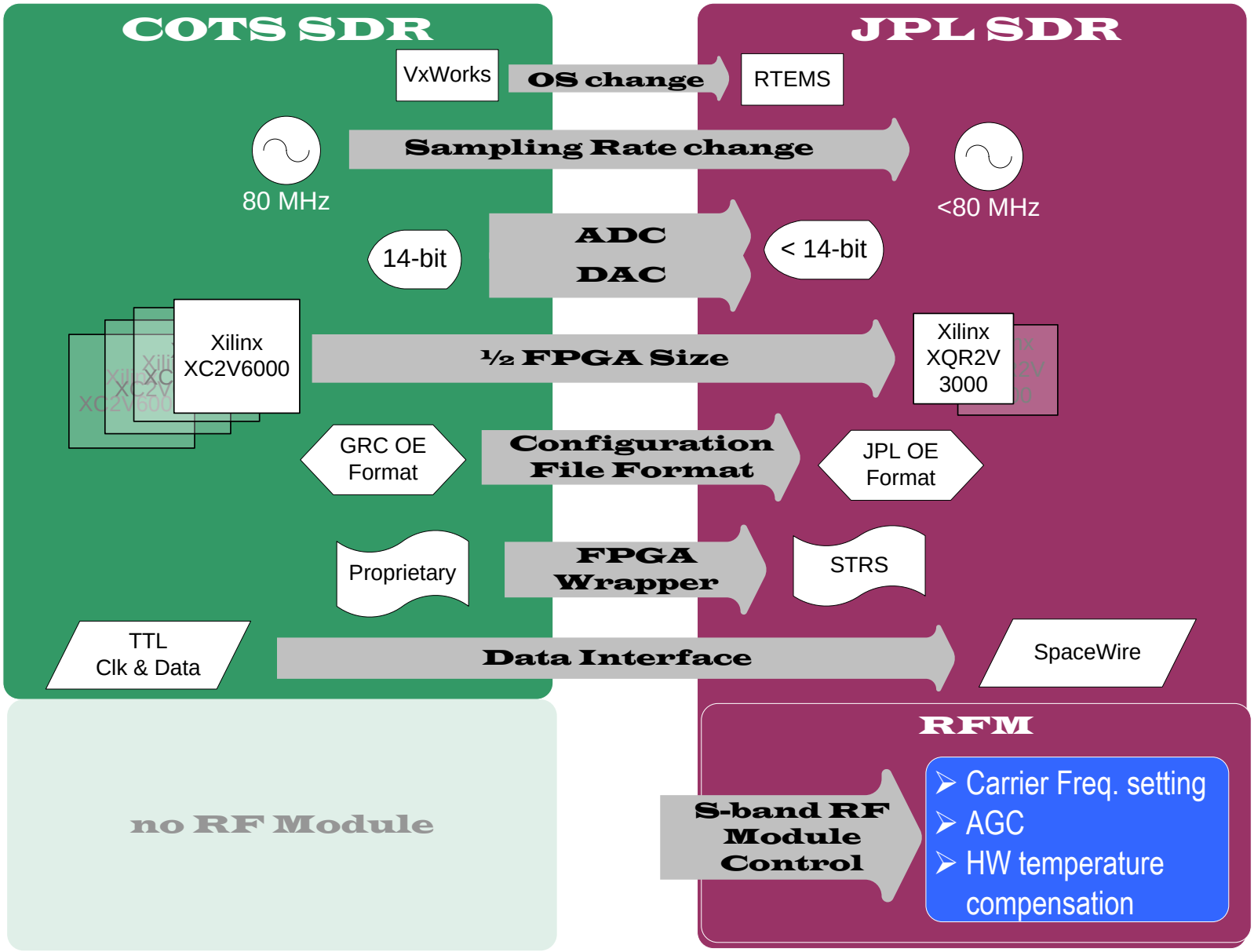
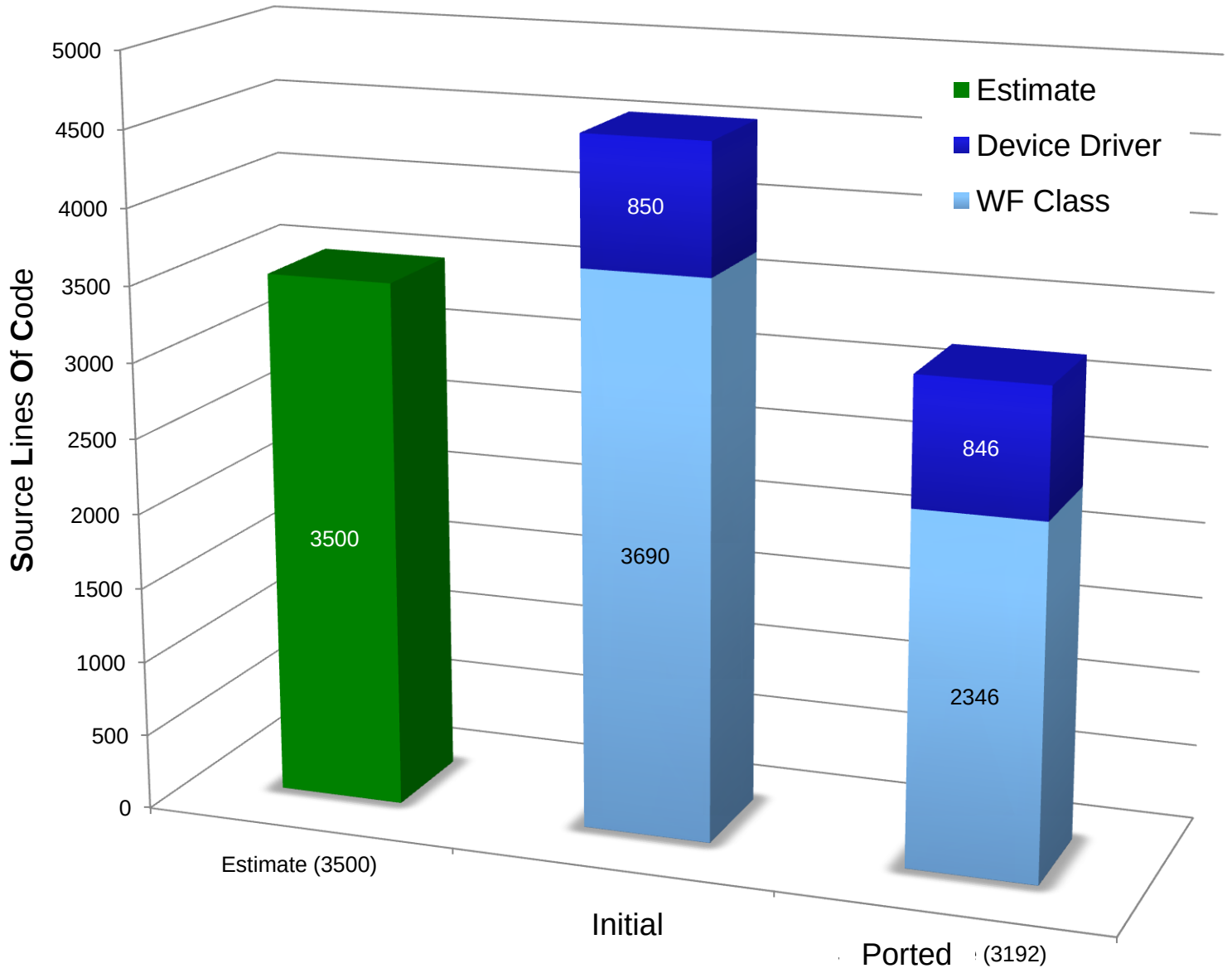
Development Approach



Porting to Target Platform



Processor Code porting - SLOC



FPGA Utilization

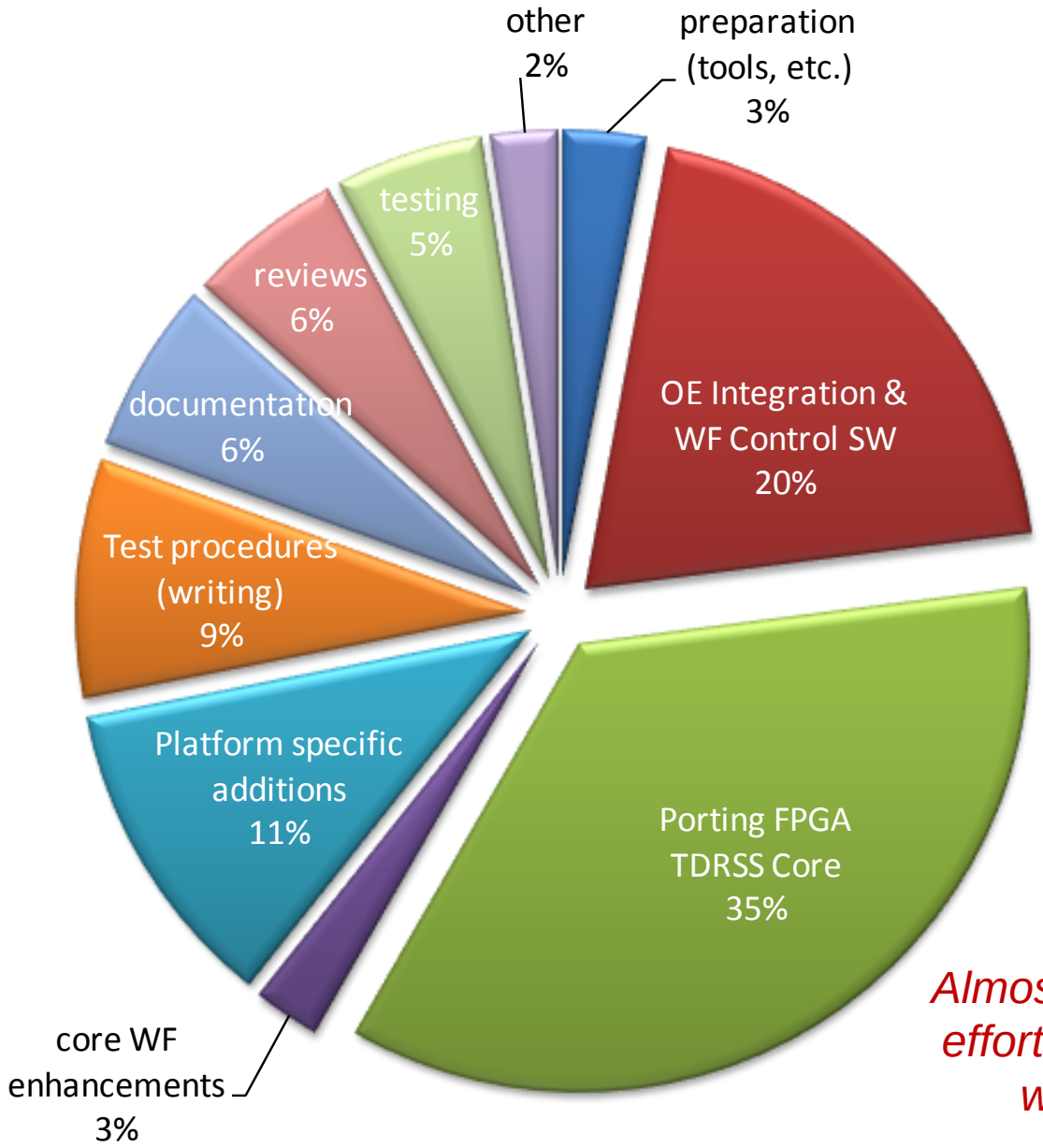
FPGA Resource	Initial Utilization	Ported Utilization
Total Slice Registers	94.5 %	59.8 %
4 input LUTs	90.0 %	70.4 %
occupied Slices	176.7 %	99.9 %
Slices containing only related logic	176.7 %	94.1 %
Slices containing unrelated logic	0 %	5.9 %
4 input LUTs	98.2 %	72.4 %
MULT18X18s	109.4 %	85.4 %

**porting of the waveform involved reducing the functionality of the original GSFC waveform so as to fit into the smaller JPL SDR FPGAs. There was also a speed reduction constraint.*

Porting Effort Overview

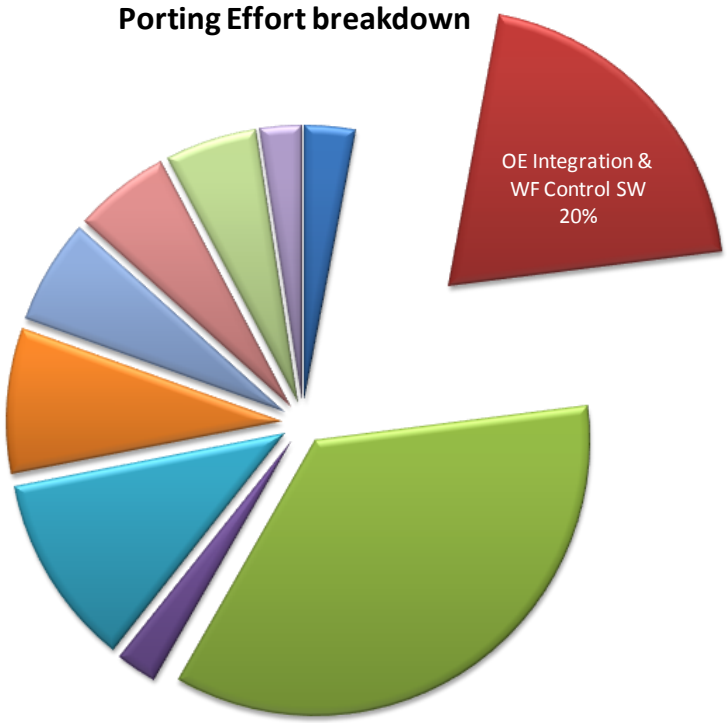
- 374 working (8 hour) days total effort divided between 3 engineers
- total calendar time 2 years
- tools used/required: Matlab/Simulink, Synplicity HDL synthesis(now Synopsis), Xilinx ISE, RTEMS development tools, Prototype BPM
- Does **not** include CoNNeCT System integration, performance, and environmental testing (vibe, thermal vacuum, EMI)
- NOTE: Porting effort blurs with system integration and flight platform specific functions. The COTS platform did not have an RF front end.

Porting Effort Breakdown



*Almost half of the porting effort was **not** related to waveform reuse*

STRS Effects



The OE integration & WF Control slice would have been significantly larger.

How did the WF port benefit with STRS?

1. Software for control was recompiled for new target processor, because of standard APIs.

2. Commanding and configuring from OE was the same, because of standard APIs.

Conclusions

1. Porting from more capable platform can be difficult:
   - Waveform design may need to change (e.g. analog I/Q mod instead of digital)
   - Reduction in features/performance.
2. SDR Platform should compensate for all temperature effects with OE and/or dedicated HW. However, some effects are waveform dependent.
3. STRS Architecture **was** helpful for this development:
   - despite the COTS to space-based platform disparity the standard APIs reduced porting effort.
   - Allowed for some parallel development, (forced by schedule constraints)
4. Better metrics could be found in a comparison of COTS to JPL Prototype, or a port of the current waveform on the JPL Flight SDR to another STRS flight SDR.

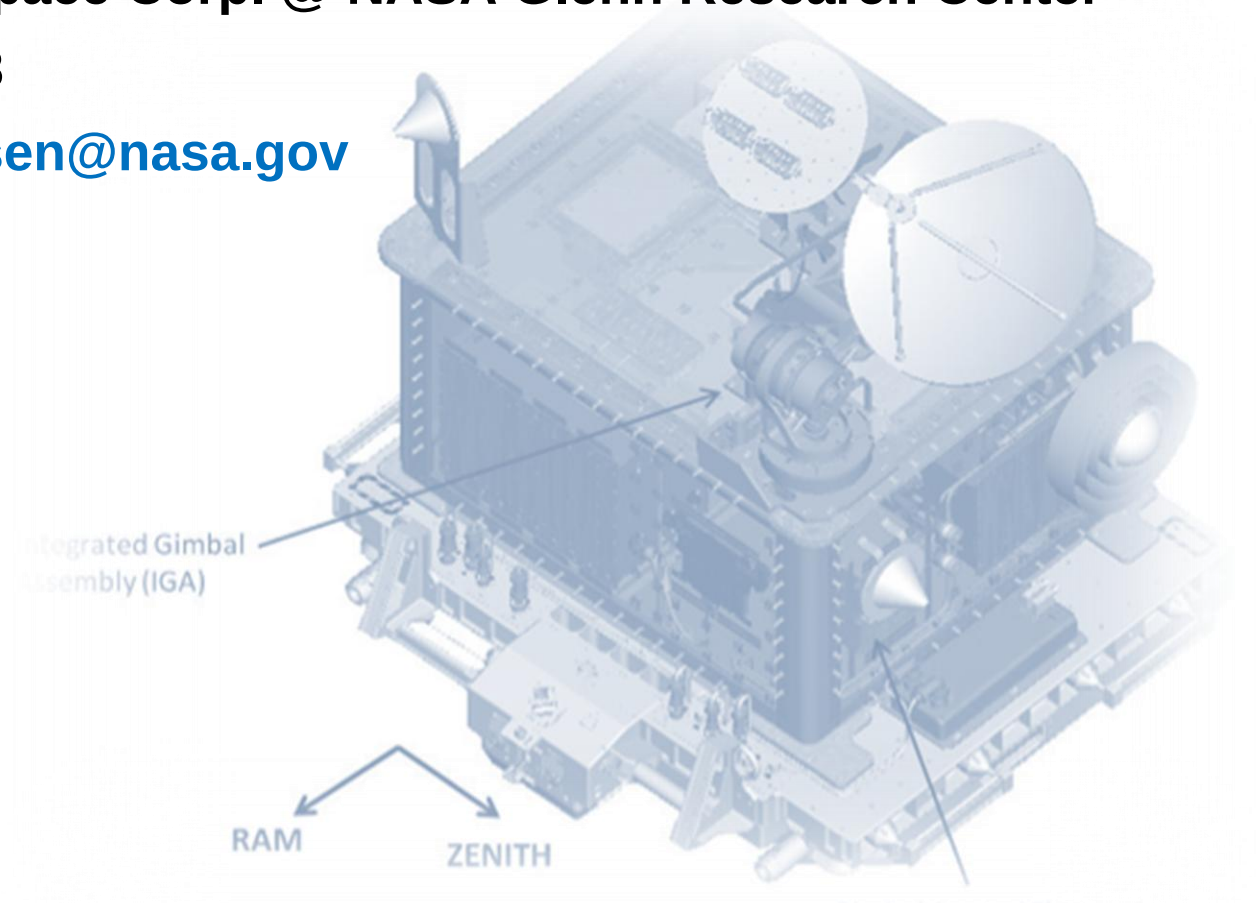
Contact Information

Dale J. Mortensen

ASRC Aerospace Corp. @ NASA Glenn Research Center

216-433-6698

dale.mortensen@nasa.gov



http://spaceflightsystems.grc.nasa.gov/SpaceOps/CoNNeCT/