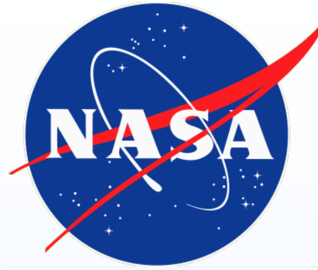

The NASA Electronic Parts and Packaging (NEPP) Program: Roadmap for FY15 and Beyond

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NASA/GSFC

http://nepp.nasa.gov

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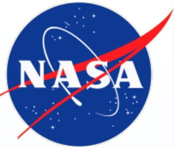
Acronyms

Acronym	Definition
AMOLED	Active Matrix Organic Light Emitting Diode
CBRAM	Conductive Bridging Random Access Memory
CGA	Column Grid Array
CIGS	Copper Indium Gallium Selenide
CMOS	Complementary Metal Oxide Semiconductor
COTS	Commercial Off The Shelf
DDR4	Double Data Rate Four
DNA	Deoxyribonucleic Acid
DoD	Department of Defense
DRAM	Dynamic Random Access Memory
EEE	Electrical, Electronic, and Electromechanical
EPC	Efficient Power Conversion
ESL	Electronic System Level
FeRAM	Ferroelectric RAM
FPGA	Field Programmable Gate Array
FY	Fiscal Year
GaN	Gallium Nitride
Gen	Generation
GSFC	Goddard Space Flight Center
HALT	Highly Accelerated Life Test
HAST	Highly Accelerated Stress Testing
HEMTs	High-electron-mobility transistors
HP Labs	Hewlett-Packard Laboratories
HW	Hardware
IC	Integrated Circuit

Acronym	Definition
IP	Intellectual Property
IR	Infrared
IR/Infineon	International Rectifier/Infineon Technologies
LCoS	Liquid-Crystal-on-Silicon
MEMS	Micro Electrical-Mechanical System
MOSFETS	Metal Oxide Semiconductor Field Effect Transistors
MRAM	Magnetoresistive Random Access Memory
NASA	National Aeronautics and Space Administration
NAVY Crane	Naval Surface Warfare Center, Crane, Indiana
NEPP	NASA Electronic Parts and Packaging
Occam	Open Conditional Content Access Management
OLED	Organic Light Emitting Diode
PBGA	Plastic Ball Grid Array
R&D	Research and Development
RERAM	Resistive Random Access Memory
RF	Radio Frequency
SEE	Single Event Effect
SERDES	Serializer/Deserializer
SiC	Silicon Carbide
SOC	Systems on a Chip
TI	Texas Instruments
TRL	Technology Readiness Level
VNAND	Vertical NAND
WBG	Wide Band Gap

Technology Selection Criteria for NEPP Investigation

- The technologies should satisfy all or most of the following criteria:
  - Wide applicability,
  - Product level or in productization, and,
  - No distinction: COTS to hi-reliability aerospace.
- Partnering arrangements with other organizations preferred.
- In general, we avoid:
  - Laboratory technologies, e.g., <TRL3,
  - Limited application devices with certain exceptions (critical application or NASA center specialization).



Technology Investigation Roadmap Discussion

- Technology assurance efforts are not explicitly included except on “Small Missions” chart.
  - *Guidelines are a product of many technology evaluation tasks.*
- Only major product categories shown.
- Technology areas not on Roadmap but under consideration include:
  - Electro-optics (fiber optics),
  - Advanced analog and mixed-signal devices,
  - Imaging sensors,
  - Modeling and simulation,
  - High-speed communication (SERDES, fast data switches), and,
  - Adjunct processors (eg., graphics, signal processing)
- Note 1: Advanced CMOS technologies not explicitly included:
  - NEPP leverages samples from ongoing DoD and/or commercial sources.
  - 14nm is current target.
- Note 2: “Reliability testing” may include product and/or package testing.

Gartner Hype Cycle Concept

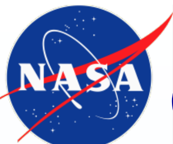
expectations

On the Rise	At the Peak	Sliding Into the Trough	Climbing the Slope	Entering the Plateau

- R&D
- Startup companies first round of venture capital funding
- First-generation products, high price, lots of customization needed
- Early adopters investigate
- Mass media hype begins
- Supplier proliferation
- Activity beyond early adopters
- Negative press begins
- Supplier consolidation and failures
- Second/thrid rounds of venture capital funding
- Less than 5 percent of the potential audience has adopted fully
- Second-generation products, some services
- Methodologies and best practices developing
- Third-generation products, out of the box, product suites
- High-growth adoption phase starts: 20% to 30% of the potential audience has adopted the innovation

Technology Trigger	Peak of Inflated Expectations	Trough of Disillusionment	Slope of Enlightenment	Plateau of Productivity

time



Gartner Hype Cycle for Electronics 2013

expectations

Wireless Power
Spin Transfer Torque Magnetic Random-Access Memory
Organic/Polymer Solar Cells
OLED Lighting
GaN Integrated Circuits
Silicon Anode Batteries
Lithium Iron Phosphate Batteries
MEMS Displays
Biochips
Memristor Memory
Instruction Set Virtualization
Resistance Polymer Memory
Terahertz Waves
Holographic Storage for Consumer Electronics
Molecular Transistors
Quantum Dot Displays
Quantum Computing
3D Photovoltaic Devices
Cognitive Radio
Photonic Crystal Displays
DNA Logic

Nanotube Electronics
Metamaterial Antennas
Printed Semiconductors
Nanomaterial Supercapacitors
450 mm Wafers
Multicore Programming
Hardware Reconfigurable Devices
Software-Defined Radio for Mobile Devices
CIGS Thin-Film Solar Cells
Occam Process
System-on-Package
FPGA in SoC
Floating Body DRAM
Silicon Photonics

Through-Silicon Vias
Network on Chip
Magnetometer
DDR4 DRAM
AMOLED
LCoS
ESL Design Tools and Methodologies
Reusable Analog IP
MEMS Gyroscopes
Electronic Paper
CMOS RF Power Amplifiers
Silicon Thin-Film Solar Cells
Resistance Phase-Change Memory
IC Subsystem Reuse
Post-193-nm Lithography
Micro Fuel Cells

As of July 2013

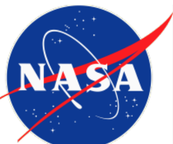
Innovation Trigger | Peak of Inflated Expectations | Trough of Disillusionment | Slope of Enlightenment | Plateau of Productivity

time

Plateau will be reached in:

○ less than 2 years ○ 2 to 5 years ● 5 to 10 years △ more than 10 years ⊗ obsolete before plateau

Source: Gartner (July 2013)



NEPP and Gartner Electronics Hype Cycle 2013

Benefit \ Years to adopt:	less than 2 years	2 to 5 years	5 to 10 years	more than 10 years
Transformational		Silicon Photonics Software-Defined Radio for Mobile Devices	Memristor Memory Nanotube Electronics	DNA Logic Molecular Transistors Organic/Polymer Solar Cells Quantum Computing Resistance Polymer Memory Terahertz Waves
High	LCoS Magnetometer Network on Chip	CIGS Thin-Film Solar Cells CMOS RF Power Amplifier ESL Design Tools and Methodologies HW Reconfigurable Devices IC Subsystem Reuse Multicore Programming Nanomaterial Supercapacitors Post-193 nm Lithography Printed Semiconductors Reusable Analog IP Silicon Anode Batteries	3D Photovoltaic Devices 450 nm Wafers Biochips GaN ICs Micro Fuel Cells Spin Transfer Torque Magnetic Random-Access Memory System on a Package	Cognitive Radio
Moderate	Resistance Phase-Change Memory Through Silicon Vias	AMOLED Electronic Paper Lithium Ion Phosphate Batteries MEMS Gyroscopes Metamaterial Antennas Wireless Power	FPGA in SOC Instruction Set Virtualization MEMS Displays Occam Process OLED Lighting Photonic Crystal Displays Quantum Dot Displays Silicon Thin-Film Solar Cells	Holographic Storage for Consumer Electronics
Low	DDR4 DRAM			

After Gartner 2013 Electronics Hype Cycle

NEPP Task Area

Future NEPP Area or Tracking Developments

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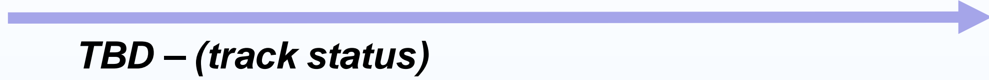
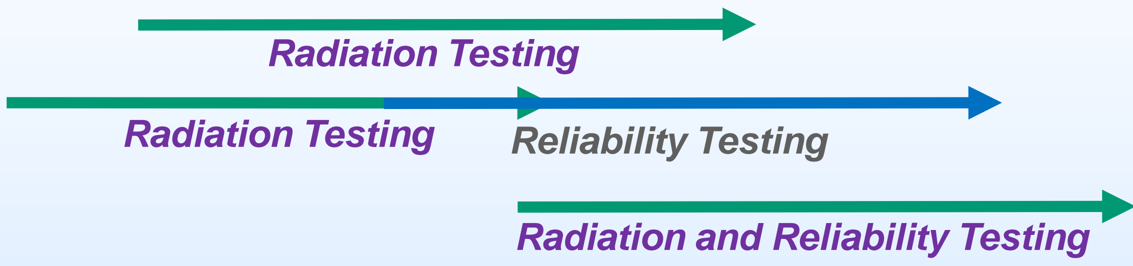
Field Programmable Gate Arrays (FPGAs)

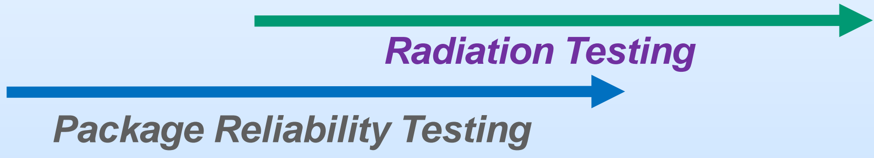
Trusted FPGA
- DoD Development



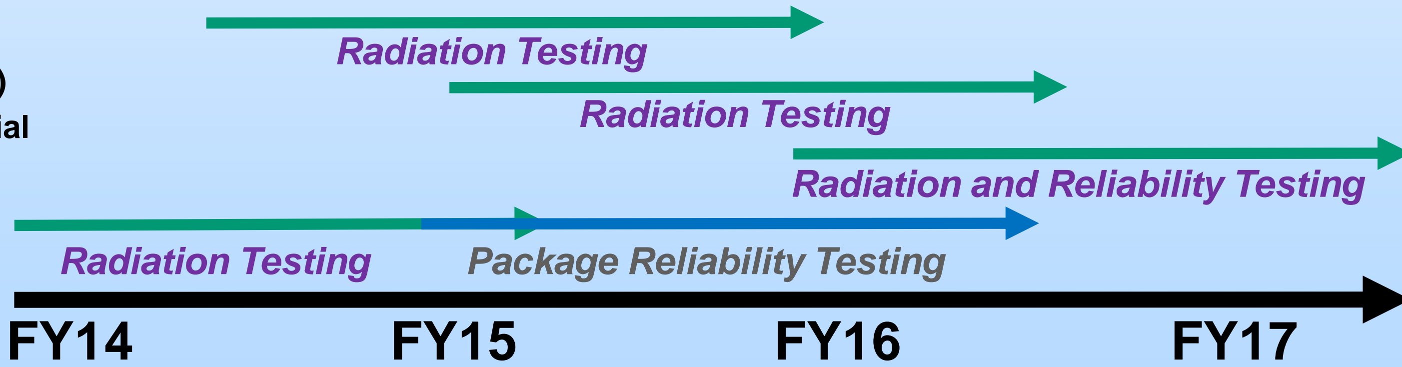
Altera
- Stratix 5 (28nm TSMC process commercial)
- Max 10 (55nm NOR based commercial – small mission candidate)
- Stratix 10 (14nm Intel process commercial)



Microsemi
- RTG4 (65nm RH)



Xilinx
- 7 series (28nm commercial)
- Ultrascale (20nm commercial – planar)
- Ultrascale+ (16nm commercial - vertical)
- Virtex 5QV (65nm RH)



Xilinx Zynq UltraScale+ Multi-Processor System on a Chip (MPSoC) family

Processing System

Application Processing Unit
Quad ARM Cortex™-A53
NEON™
Floating Point Unit
32KB I-Cache with Parity
32KB D-Cache with ECC
Memory Management Unit
SCU
GIC
CCI/SMMU
1MB L2 Cache/ECC

Graphic Processing Unit
ARM Mali™- 400 MP
Geometry Processor
2 Pixel Processors
Memory Management Unit
64KB L2 Cache

DDR Controller
DDR4/3/3L, LPDDR4/3, ECC Support
256KB OCM with ECC

High Speed
Display Port
USB 3.0
SATA 3.0
PCIe Gen2
PS-GTR

Real-Time Processing Unit
Dual ARM Cortex™-R5
Vector Floating Point Unit
Memory Protection Unit
128KB TCM with ECC
32KB I-Cache with ECC
32KB D-Cache with ECC
GIC

Security
Configuration AES Decryption, Authentification and Secure Boot
TrustZone
Voltage/Temp Monitor

Platform Management Unit
Power
System Management

System Control
DMA, Timers, WDT, Resets, Clocking and Debug

General Connectivity
Gigabit Ethernet
CAN
I2C
UART
USB 2.0
SPI
Quad SPI NOR
NAND
SD/eMMC

Programmable Logic

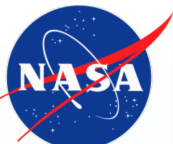
Storage and Signal Processing
Block RAM
UltraRAM
DSP

General Purpose IO
High-Performance HPIO
High Density HDIO

High Speed Connectivity
GTH
100G EMAC
GTY
PCIe Gen4
Interlaken

Video Codec
H.265/H.264
AMS

From Xilinx.com



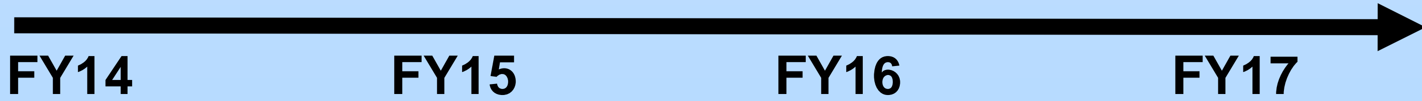
Advanced Processors

Next Generation Space Processor (NGSP)
- Joint NASA-AFRL Program for RH multi-core processor
- TBD architecture/process

RH Processor
- BAE Systems RAD5510/5545
- Replacement for RAD750

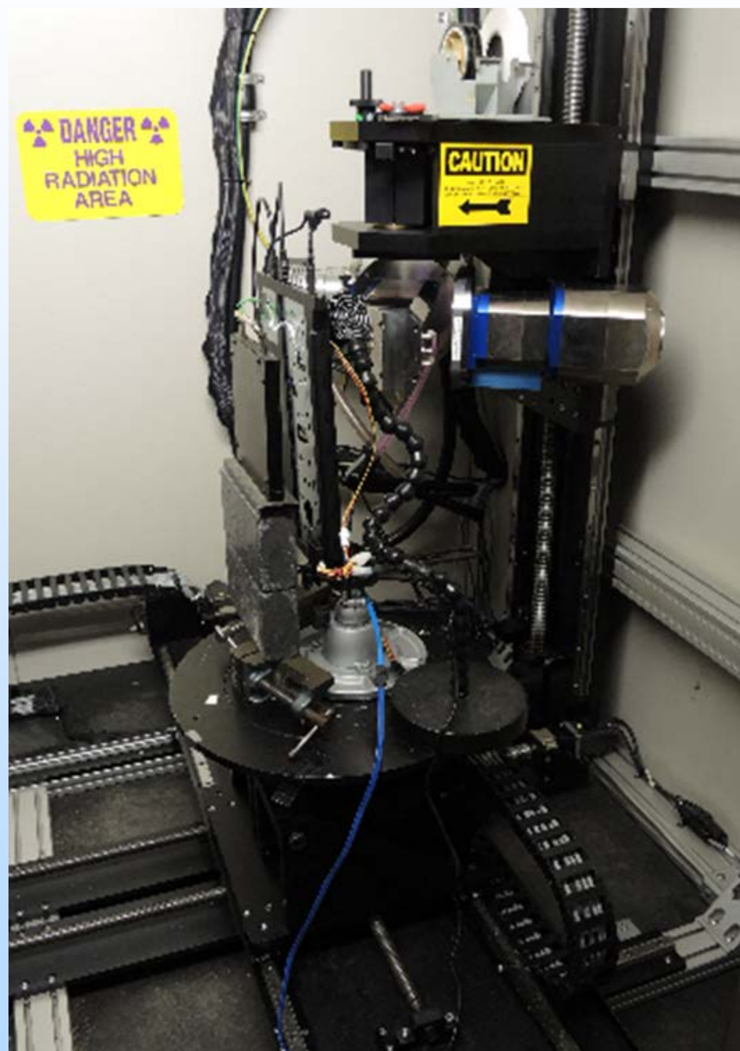
Intel Broadwell Processors
- 14nm FinFET commercial
- 1st high-performance sans heatsink (lower power for performance)

Freescale P5020/5040
- Commercial 45nm network processor
- Preparation for RH processor



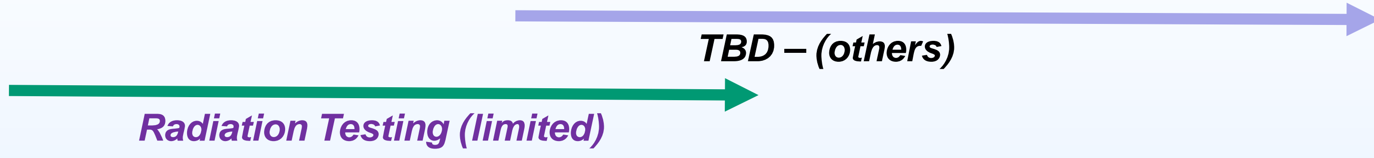
Note: Future considerations under discussion include automotive "self-driving" processor options.

Preliminary Radiation testing of 14nm Intel with Navy Crane

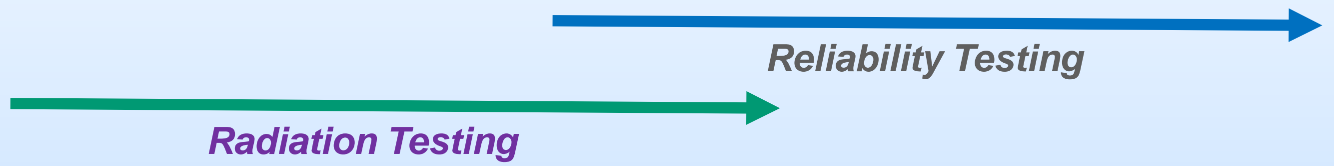


Microcontrollers and Mobile Processors (Small Missions)

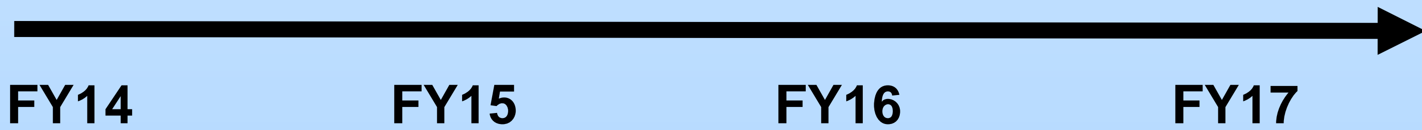
TBD – other
- Atmel AT91SAM9G20, and TI Sitara AM3703,
- ARM (Snapdragon), Intel Atom mobile



TI MSP430
- Popular CubeSat microcontroller
- Several varieties



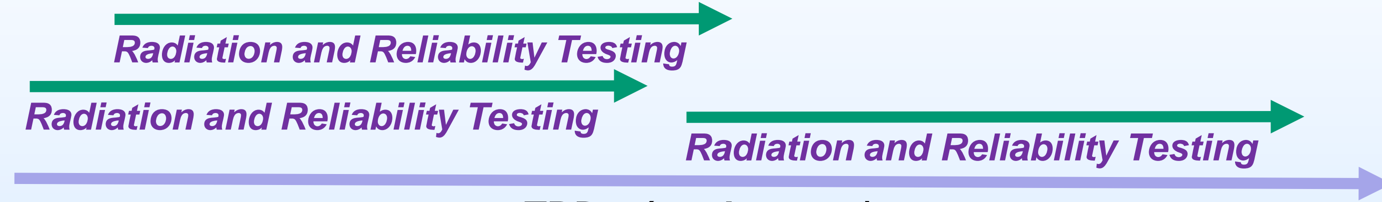
Freescale MPC56XX
- 90nm on-shore fab
- Automotive Grade
- Being used for both part and board level testing



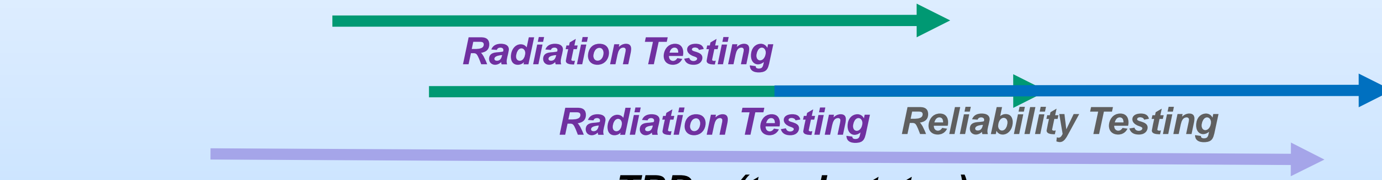
Commercial Memory Technology

Other
- MRAM
- FeRAM

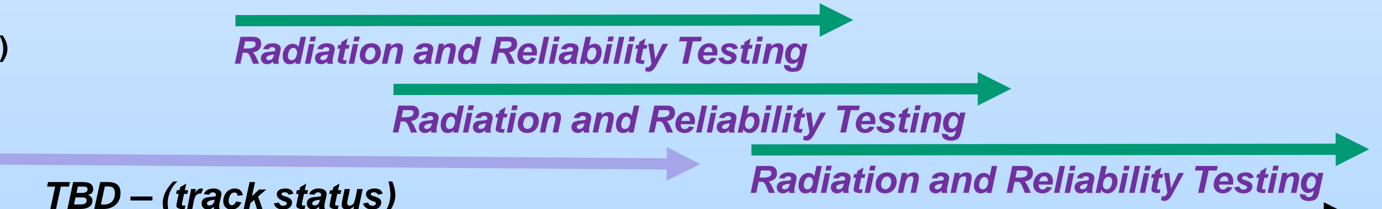
Resistive
- CBRAM (Adesto)
- ReRAM (Panasonic)
- ReRAM (Tezzaron)
- TBD (HP Labs, others)



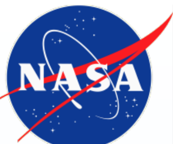
DDR 3/4
- Intelligent Memory (robust cell twinning)
- Micron 16nm DDR3
- TBD – other commercial



FLASH
- Samsung VNAND (gen 1 and 2)
- Micron 16nm planar
- Micron Hybrid memory Cube
- TBD - other commercial



FY14 FY15 FY16 FY17



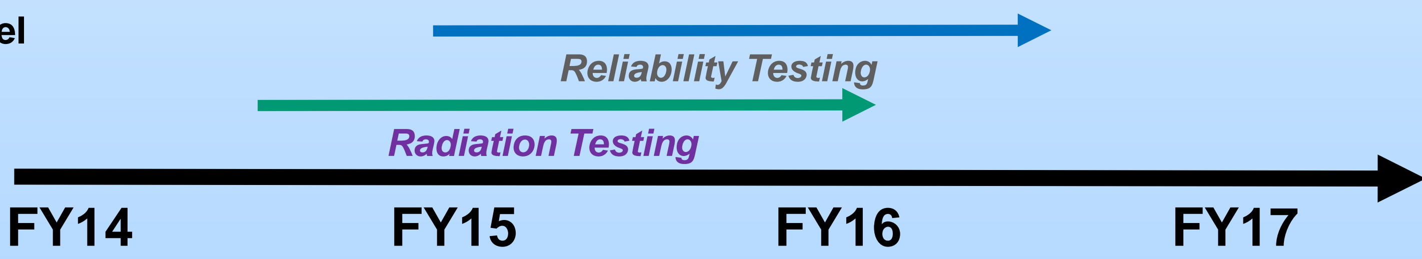
Small Missions

EEE Parts Guidelines
- Small missions (Class D, CubeSat – 2 documents)
- System on a chip (SOC) single event effects (SEE) guideline

Commodities evaluation
- See commodities roadmaps for processors, power
- CubeSat Star Tracker

Automotive grade electronics
- Multiple classes of electronics (passives, actives, ICs)
- Testing by NASA and Navy Crane

Alternate test – board level
- Freescale MPC56XX
- Automotive Grade
- Both part and board level reliability testing



Automotive Processors and Systems for Self-Driving Cars?

S32V234 Block Diagram

Image Proc. Platform
- Dual Camera Interfaces: 2 x MIPI CSI2; 2 x Parallel 16 bit
- Image Signal Processing: HDR, Color Conversion, Tone Mapping
- Image Cognition Proc.: L-mem, L-mem, 32 CU, 32 CU, Sequencer, DMA — APEX2CL

CPU Platform
- Cortex-A53: 32 KB I-cache 2 way; 32 KB D-cache 4 way; NEON
- Cortex-A53: 32 KB I-cache 2 way; 32 KB D-cache 4 way; NEON
- Cortex-M4
- SCU; L2 Cache–512 KB + ECC

Vision Platform
- Gfx & Display: 3D GPU; DCU 18/24 bits RGB
- Video Codec H.264: 8-12 bit Encoder; 8-12 bit Decoder JPEG/H.264

Internal Memory: 4 MB RAM with ECC

Security: CSE + Flashless

Fabric: Amba AXI3/ACE interconnect 128-bit with MPU

System Control & Support: FCCU & M/L BIST; T-Sensor; CRC Computing; Safe DMA; DEBUG and Trace Unit

Ext. Memory I/F: DDR Control + ECC; DDR Quad SPI

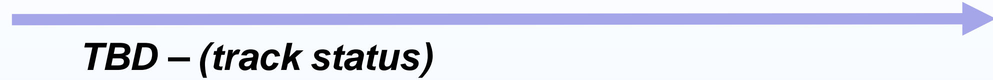
External Memory: LP-DDR2/DDR3

Connectivity
- Zipwire
- 2xCAN-FD 64 Msg
- 5 Gb/s PCIe 1 Lane
- 2x eTimers
- Dual Ch. FlexRay 128 Msg
- 2x LinFlex Control & 3x I^2C
- 1x SAR ADC 12 bits, 1.8 V
- Gigabit Ethernet Control
- 4x dSPI (4 cs)
- 1x SD-HC

From Freescale.com

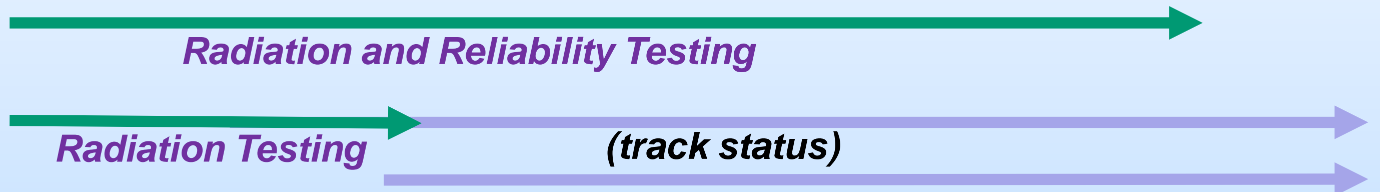
Wide Band Gap (WBG) Technology

GaN Class V development
- Microsemi with EPC



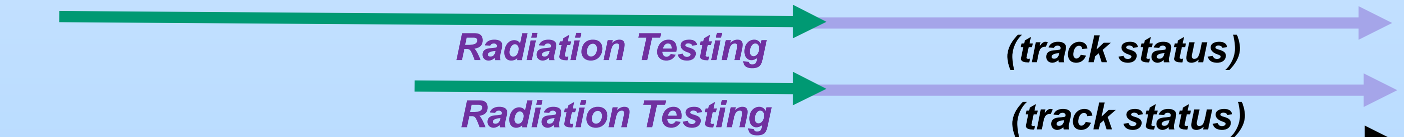
GaN Enhancement Mode HEMTs
- EPC Gen 2-3, 200 V - 600 V
- GaN Systems 100 V, 650 V
- Panasonic 600 V (target)
- IR/Infineon 600 V (target)

SiC MOSFETs
- Cree Gen 1-2 1200 V - 1700 V
  Gen 3- narrower neck
- STMicro baseline SEE test
- Rohm Trench design



SiC Diodes
- Manufacturer X SEE baseline and hardening efforts

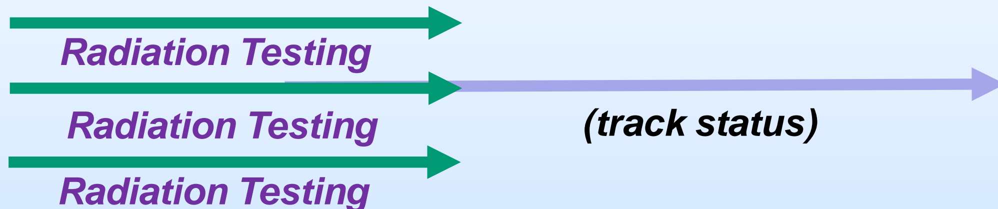
SiC ICs
- Ozark IC
- Manufacturer X



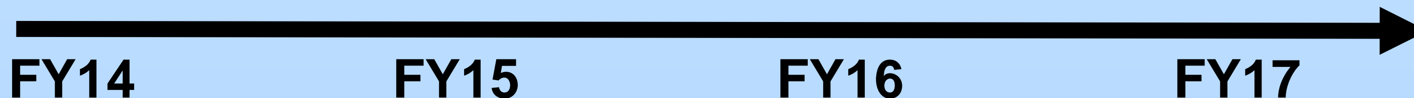
FY14 **FY15** **FY16** **FY17**

Silicon Power Devices

MOSFETs – Rad Hardened
- Microsemi i2MOS
- Infineon superjunction 100 V, 600 V (target)
- IR/Infineon R8 trench 20 V



Schottky Diodes
- Multiple vendors, reverse voltage ratings, and forward current ratings



Packaging Technologies (1 of 2)

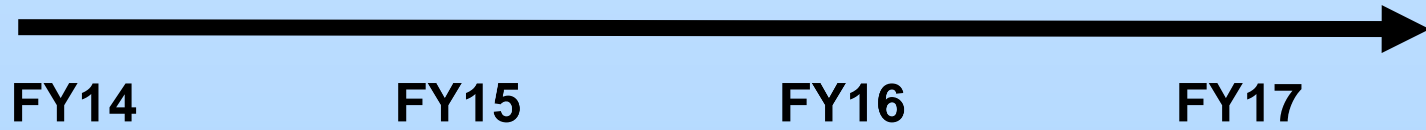
High Density, Non-hermetic Column Grid Array (CGA)
- **Xilinx CN/Kyocera Daisy Chain**
- **Microsemi Daisy Chain**
- ***Materials analysis, long term stress, root cause failure***

HALT Methodology/Qualification
- **HALT/HAST comparison**
- **Plastic BGA matrix**

Area Array Column
- **Selection guide**

Thermal Interface Materials
- **Selection guide**

PBGA Thermal Cycle Evaluation

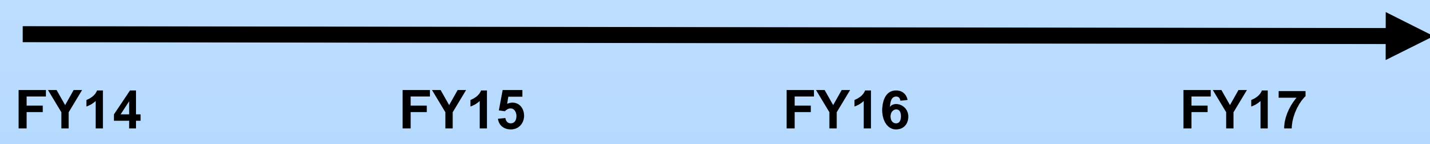


Packaging Technologies (2 of 2)

Bump Reliability
- Technology review
- Test vehicle options

3D Packaging Technologies
- Technology review
- Test vehicle options

QFN package reliability
- Reliability/Qualification metrics



And Just When You Think Your Roadmap is Set, New Parts are Released

- Examples
  - More complex processors
    - TI Multicore DSP+ARM KeyStone II System-on-Chip (SoC)
  - Integrated "instruments"
    - TI DLP2010NIR – near IR sensing and controller

Summary and Comments

- NEPP Roadmaps are constantly evolving as technology and products become available.
  - Like all technology roadmaps, NEPP's is limited to funding and resource availability.
  - Not shown are TBD passives and connector roadmaps under development.
  - NEPP is working to develop preliminary plans on interfacing to the NASA Reliability and Maintainability Program and its work on Model Based System Engineering (MBSE) approaches.
- We look forward to further opportunities to partner.

https://nepp.nasa.gov