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Preliminary Radiation Testing of a State-of-the-Art Commercial 14nm CMOS Processor / System-on-a-Chip

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Abstract: Radiation test results of Intel state-of-the-art 14nm "Broadwell" U-series processor / System-on-a-Chip (SoC) for total dose are presented, along with exploratory results from trials at a medical proton facility. Investigation builds upon previous collaborative efforts [1] by utilizing commercial laptop motherboards and software stress applications as opposed to traditional automated test equipment (ATE).

Introduction

Commercial processors provide an intense topic of interest for the space community. As technologies and manufacturing processes have advanced in response to the free market demand, the resulting innovations offer a tantalizing set of benefits to space users. These are: high-performance, low-cost, and a trend toward better radiation tolerance as feature sizes shrink.

TABLE I: EXAMPLE HISTORICAL HARDNESS OF PROCESSORS

Device	Technology*	Test Date	Result	Ref.
Intel 80386-20	1 µm CHMOS IV	1993	Failure Between 5-7.5 krad(Si)	[2]
Intel 80486DX2-66	0.8 µm CHMOS V	1995	Failure Between 20-25 krad(Si)	[3]
Intel Pentium III	0.25 µm CMOS	2000	Failure ~ 500 krad(Si)	[4]
AMD K7	0.18 µm CMOS	2002	Failure > 100 krad(Si)	[4]
AMD Llano	32 nm CMOS	2013	No Failures 1, 4, 17 Mrad(Si)	[1],[5]

* = all technologies are complementary metal-oxide semiconductor (CMOS).
The H in CHMOS stands for high-density.

With the advent of Intel's present day 14nm Tri-Gate "Broadwell" line-up, users may begin realizing another additional benefit: low-power, and with that, lower heat output. The Device Under Test (DUT) for this report is a 15-Watt design, but alternative products on this same process offer as low as 4.5-Watt Thermal Design Power (TDP). These parts are the first Core™ processor family fan-less offerings to the mainstream market.

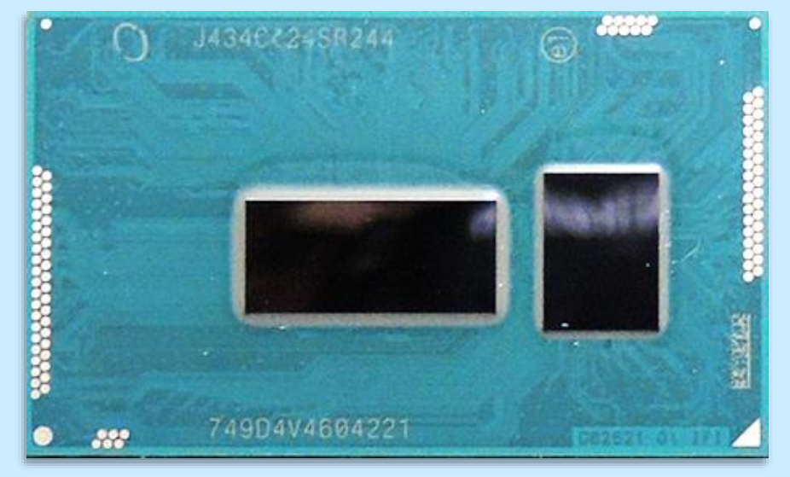
To slightly twist a quote attributed to Voltaire: "With great (low) power, comes great responsibility". How does this technology compare to the previously studied planar designs under irradiation? And, how viable is Tri-Gate design for future space applications?

The goal of this work is to identify possible areas of weakness in 14nm state-of-the-art processor technology by leveraging retail and freeware software to exercise candidate devices in the presence of radiation. The results, while performed at the system level, will hopefully aid future researchers and add to our realm of knowledge of these sophisticated devices.

Device Description

The DUT utilized is a state-of the-art 14nm processor / SoC from Intel Corporation [6]

- Part Number: FH8065801884006, also known as Core™ i3-5005U
- Single Package, Multi-Chip Design on 1168-ball micro Flip-Chip Ball Grid Array (FCBGA)
- Center Die Houses Arithmetic and Graphic Cores
- Outer Die Houses Input/Output Features
- Maximum Frequency: 2.0 GHz
- Minimum Frequency: 500 MHz
- Level 1, 2, and 3 caches
- 15 Watt Thermal Design Power (TDP)
- 10 Watt "Configurable" TDP mode
- Alternative Parts Manufactured on This Process Feature TDP as low as 4.5 Watts

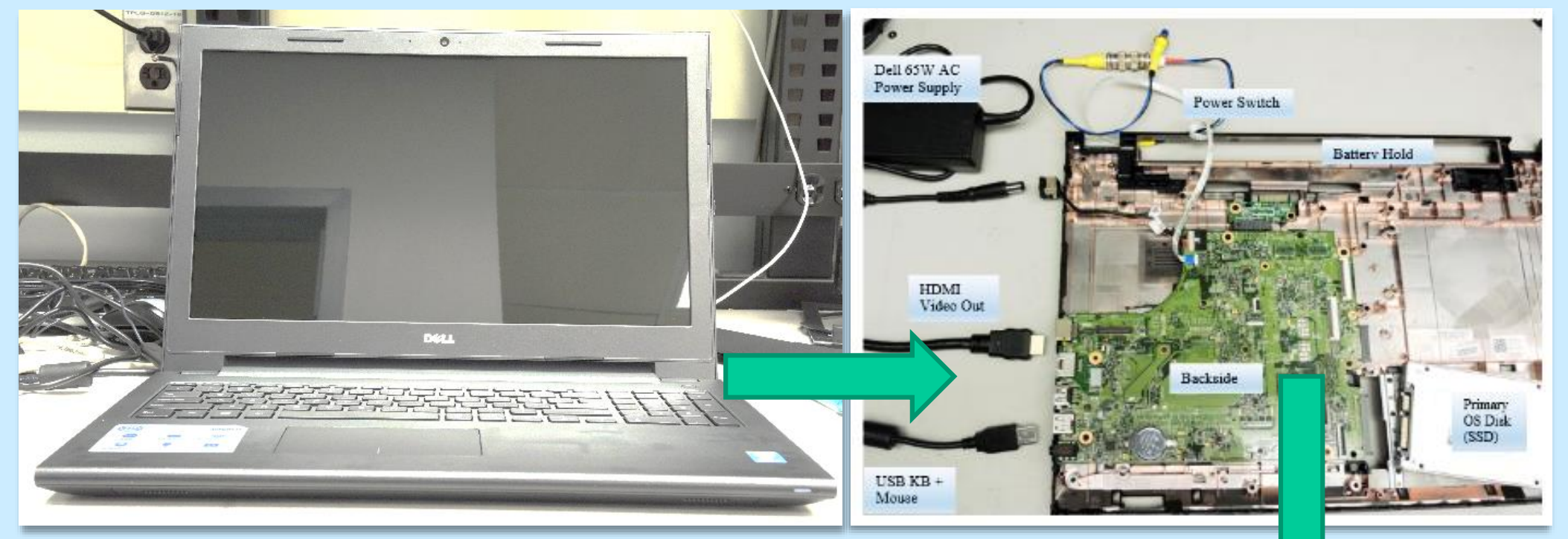

Intel Broadwell-U Series Processor

Intel maintains multiple fabrication sites

- Three sites are producing parts at the 14nm level
- It is unknown whether the chosen DUT was produced in Oregon, USA, Arizona, USA, or Leixlip, Ireland, is unknown

Test Setup – Hardware and Software

Dell Inspiron 3000 series laptops [11] were procured and partially dismantled to create a test fixture. The folding display panel, integrated touchpad device, heat-sink, fan, and other ribbon connected interfaces were removed. An externally powered server-grade 8000 Revolutions per Minute (RPM) 60mm fan was utilized to provide external cooling in lieu of the missing heat-sink. An external Solid State Disk (SSD) was connected to the internal Serial Advanced Technology Attachment (SATA) interface and also powered externally.



- Removal of integrated hardware yields power readings that more closely represent actual power needs of the processor
- Fixture may be operated via battery or Dell supplied 120V adapter
- 60mm fan provides cooling by moving air across the face of the processor.

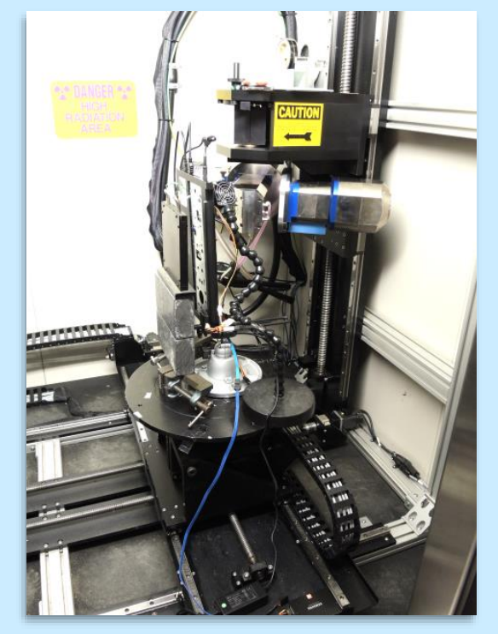
TABLE II: SUPPORTING SOFTWARE

Title	Function
Microsoft Windows Server 2012 R2	Commercially available Operating System (OS), Standard Edition, configured to be "portable". http://www.microsoft.com/en-us/server-cloud/products/windows-server-2012-r2/
HWiNFO64	Freeware hardware monitoring and on-board sensor logging tool. http://www.hwinfo.com
Intel Optimized LINPACK Library	Freely available stress computation and benchmarking software. Binaries are maintained by Intel and tailored to optimize latest features on Intel products. https://software.intel.com/en-us/articles/intel-math-kernel-library-linpack-download
Geeks3D.com "FurMark"	Freeware graphical stress tool – causes integrated graphics capabilities to consume power and dissipate heat. http://www.ozone3d.net/benchmarks/fur/
Splinterware System Scheduler	"Free Version" of the software tool was utilized to automate software steps that required interaction (i.e. key presses, custom log naming, dismissal of dialog windows) http://www.splinterware.com/products/wincron.htm
PsTools	Collection of command-line tools to facilitate system administration of OS https://technet.microsoft.com/en-us/sysinternals/bb896649.aspx

While not officially supported by Microsoft, the "Windows to Go" method was chosen for maximum flexibility of our choice of OS [12]. The latest official drivers were installed and unneeded services were disabled when possible. The remaining software was executed, either interactively, or via batch scripting, to perform hardware stress testing or statistical data logging.

Total Ionizing Dose (TID) Testing

- Performed at NAVSEA Crane using Northstar X5000 X-ray chamber
- Exposures made while executing (OS) at idle, with performance statistics logging, on 120V power adapter
- Full suite of stress tests run post-exposure, on battery


Test Fixture Mounted in X-ray Chamber

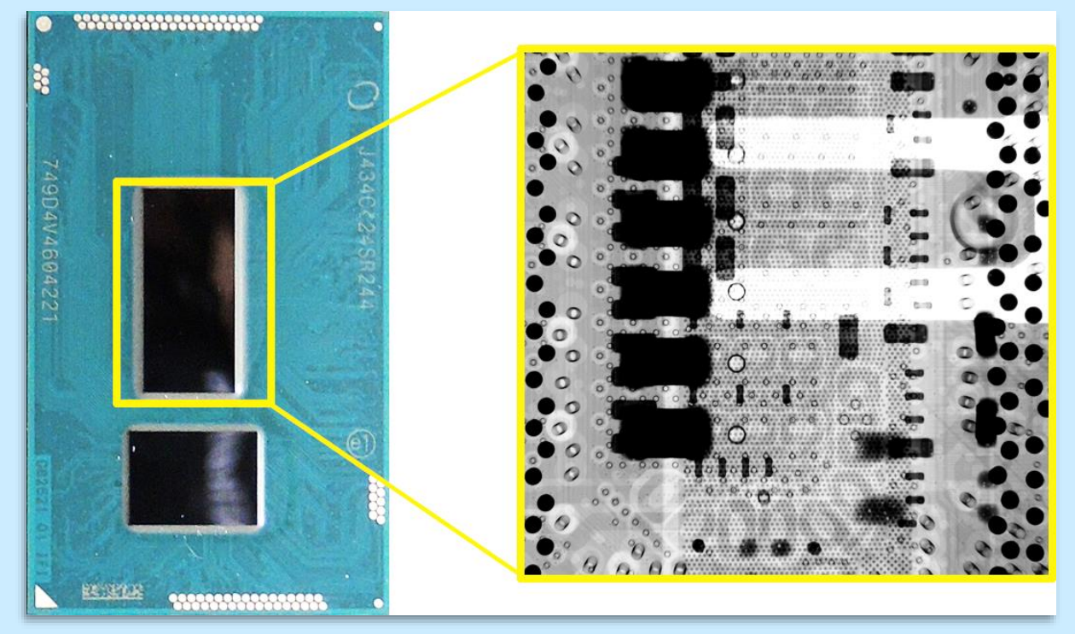
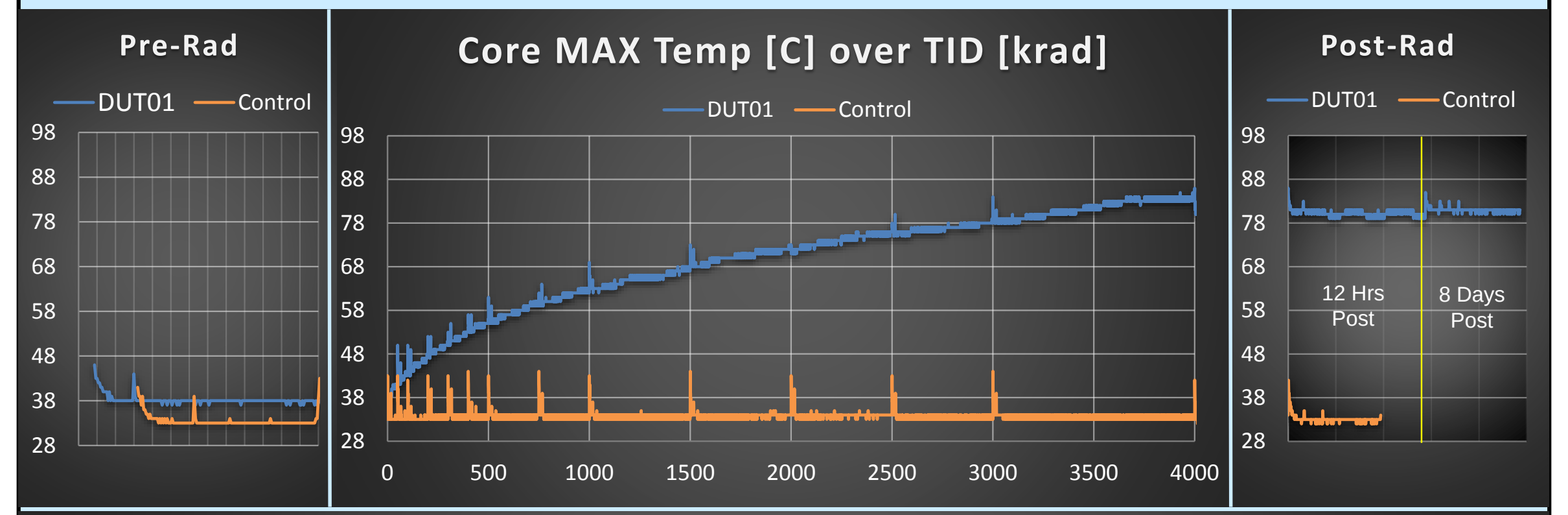


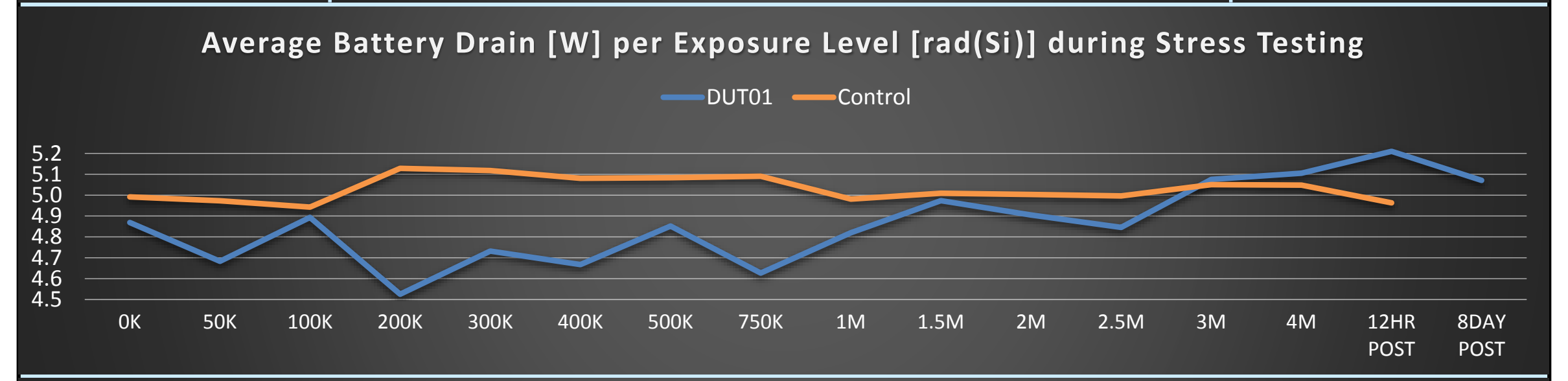
Diagram Indicating Portion of DUT Targeted by X-ray

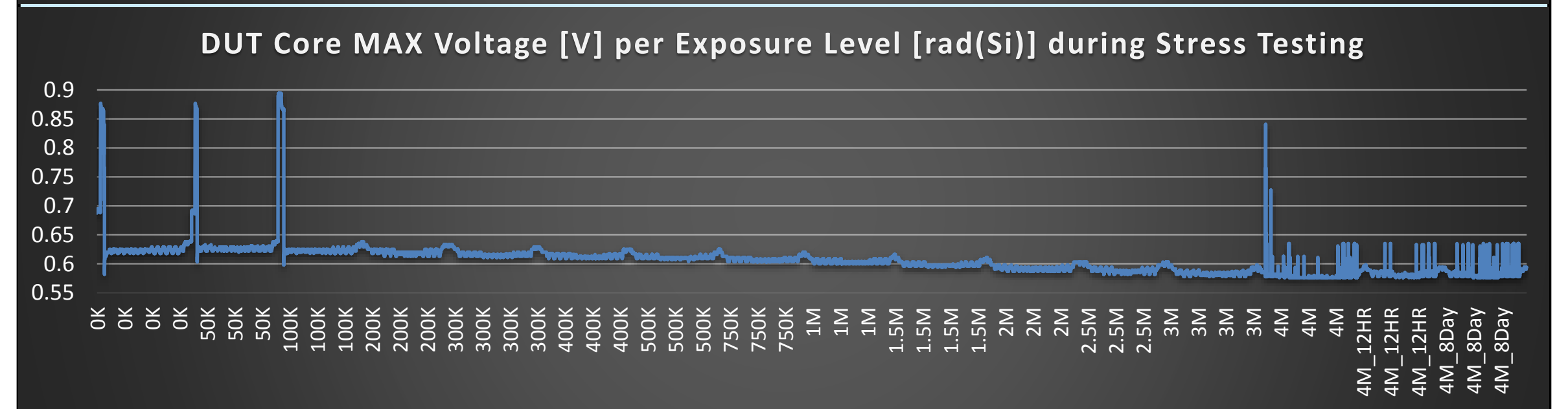
Total Dose Results

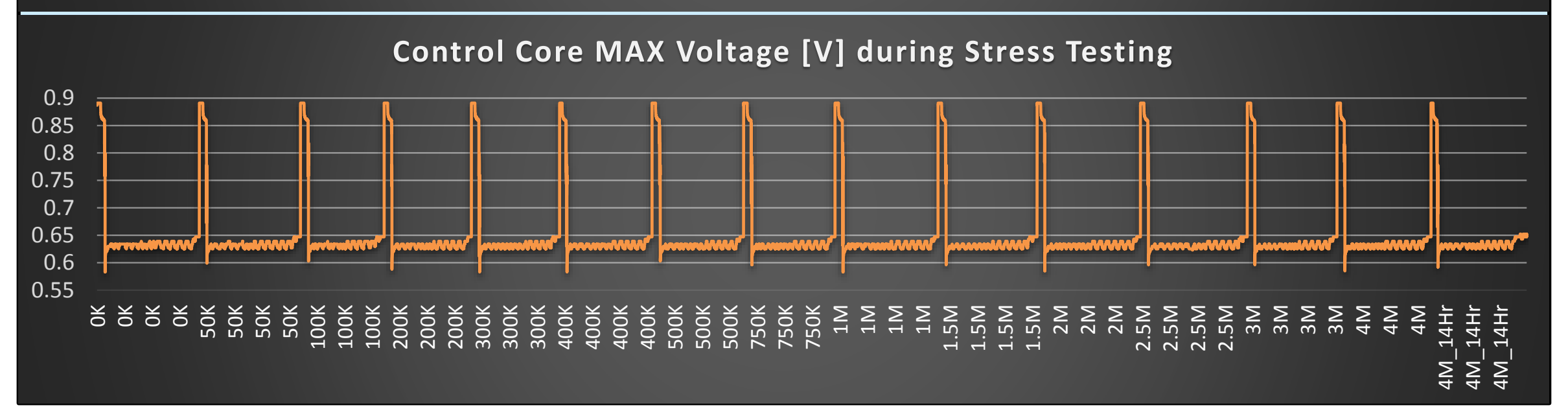
1 sample step-stress irradiated to 4 Mrad(Si); Dose rate was ~10.8 krad(Si) / Min

- No processor functional failures observed at tested levels
  However,
- Processor temperature readings degraded early into testing
- Processor reported decreasing voltage levels throughout testing, under idle and stress conditions, but required more power as exposure levels increased
- Irradiated sample generally completed LINPACK tests ***faster*** than control sample after irradiations began









Total Dose Stress Test Performance

TABLE III: STRESS, POWER, AND PERFORMANCE STATISTICS

Dose Level	DUT Avg. Batt. Drain (W)	Control Avg. Batt. Drain (W)	DUT LINPACK Time (s)	Control LINPACK Time(s)	DUT LINPACK GigaFlops	Control LINPACK GigaFlops
0K (Pre-Rad)	4.869	4.992	279.233	325.226	6.7441	5.7903
50K	4.683	4.973	287.543	294.652	6.5492	6.3912
100K	4.893	4.942	296.568	285.84	6.3498	6.5882
200K	4.525	5.129	265.096	299.36	7.1037	6.2906
300K	4.732	5.118	260.46	289.263	7.2302	6.5102
400K	4.668	5.080	264.422	284.394	7.1218	6.6217
500K	4.852	5.084	268.555	306.662	7.0122	6.1408
750K	4.627	5.091	259.631	305.746	7.2532	6.1592
1M	4.820	4.981	260.323	304.19	7.234	6.1907
1.5M	4.974	5.009	265.909	282.004	7.082	6.6778
2M	4.905	5.003	304.87	301.871	6.1769	6.2383
2.5M	4.845	4.996	234.362	315.318	8.0353	5.9723
3M	5.075	5.050	264.739	320.198	7.1133	5.8812
4M	5.105	5.048	316.455	302.024	5.9508	6.2351
4MPOST12HR (Post-Rad)	5.209	4.963	277.687	283.09	6.7816	6.6522
4MPOST8DAYS (Post-Rad)	5.071		265.058		7.1047	
Mean	4.866	5.031	273.182	299.989	6.9277	6.2893
Standard Deviation	0.190	0.059	20.097	13.574	0.4989	0.2818

Proton Facility and "Testing"

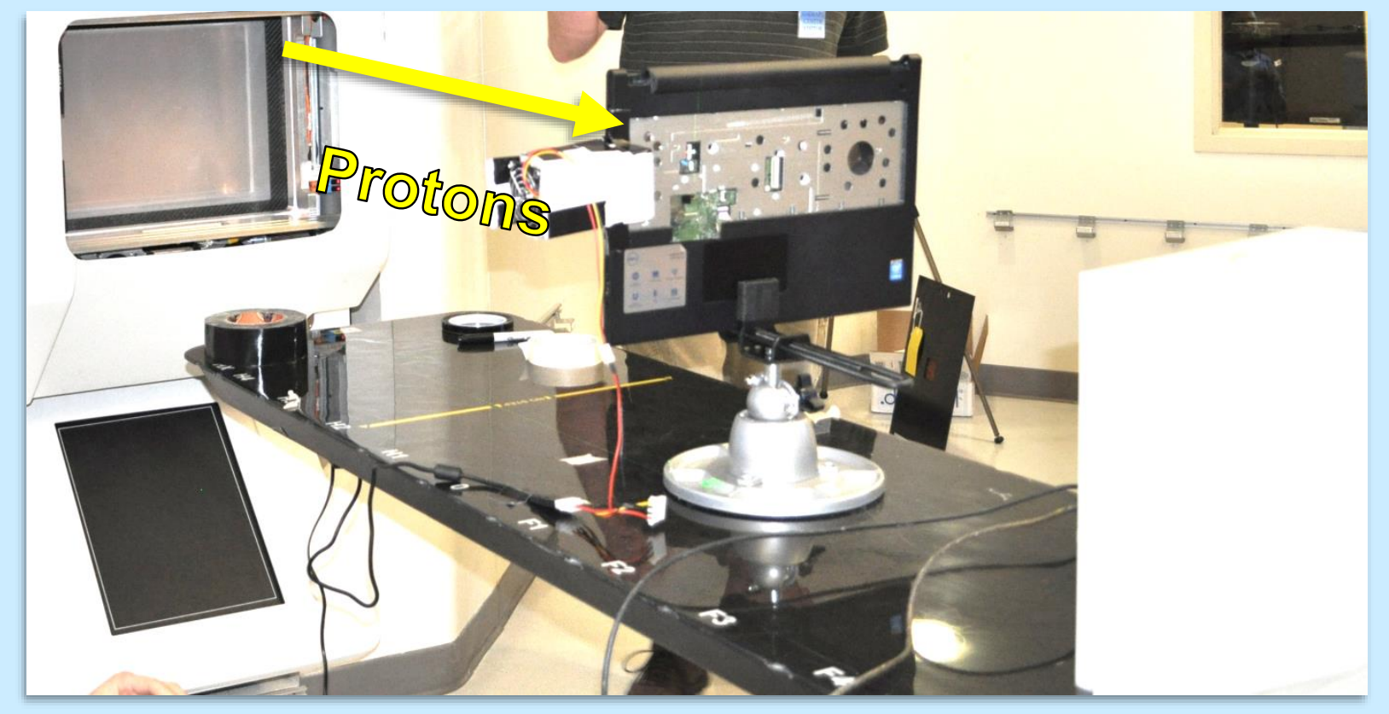
- SCRIPPS Proton Therapy Center is a medical facility located in San Diego, CA, USA
  - Facility was chosen for evaluation by NASA/U.S. government /industry collaborative effort to investigate feasibility of U.S. Proton Cancer Facilities in wake of Indiana University Cyclotron closure
  - Refer to NSREC 2015 poster, "Evaluation and Application of U.S. Medical Proton Facilities for Single Event Effects Test," by B. Wie et al., for further details on this facility study

One of the challenges of performing any single event testing of modern, complex processors is the large amount of features built-in to provide availability and resiliency (example Ref [20]). While these features provide certain soft error protection that helps the user, several items need to be considered for the single event tester:

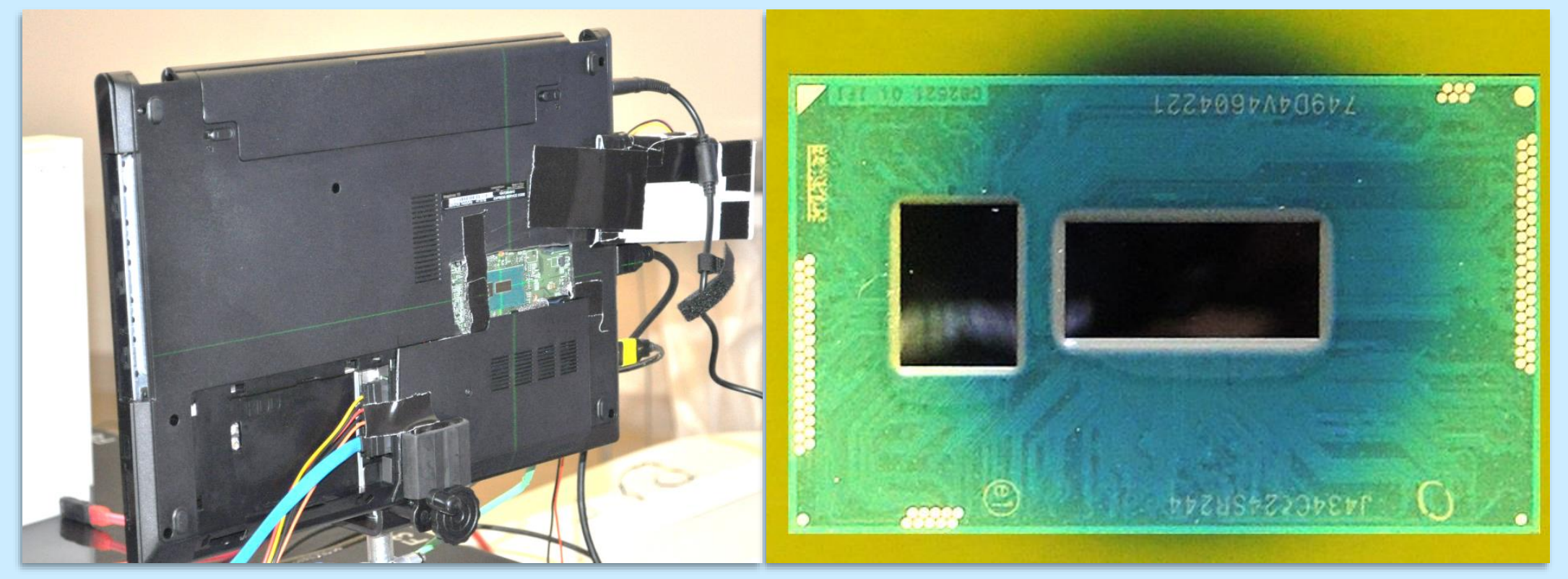
- Some single particle errors may never be seen eternally to the device due to correction of the errors limiting visibility of error occurrence for sensitivity analysis
- Some errors may be logged such as cache errors and allow the system to remain available
- Some errors may cause crashes to the system and an accompanying reboot

1 sample exposed to 200 and 220 MeV Protons

- Exposures were made while executing (OS) and collecting performance statistics: at idle (non-stress), with LINPACK only (math stress), and with LINPACK and FurMark (math and graphical stress)



Test fixture being setup on patient examination table.


Test fixture undergoing alignment (left); radiographic overlay of beam spot over sample DUT (right).

Proton Test Results

Three types of Single Event Effects (SEE) generally observed

- System Crashes (Fatal Errors (FE))
- Recoverable Errors (Non-Fatal Errors (NFE))
- *Not-Logged:* Visible Disturbances in Video (Graphical "Glitches")

Caveat: these are rough results

- Limited test time and statistics
- Test methods (and facility interactions) undergoing refinement

During non-stress (idle) testing, the DUT was least susceptible to errors

- ~ FE Cross-Section: $2x10^{-9}$ cm^2 \ ~ NFE Cross-Section: $3x10^{-9}$ cm^2

During both types of stress tests, the DUT exhibited more sensitivity

- FE Cross-Section an order of magnitude more sensitive than idle tests: $1\text{-}2x10^{-8}$ cm^2
- NFE Cross-Section $\sim 3x10^{-9}$ cm^2 for math only, up to $\sim 1x10^{-8}$ cm^2 for combined math and graphical

Regarding Non-Fatal Errors:

- *Generally appeared in conjunction with Graphical Glitches*
- *OS provides some insight via Machine Check Architecture*
- *Cache Level 1 and 2 Instruction (Pre)Fetch NFEs prevalent*

No hard device failures occurred despite encountering FE conditions in all but two test runs

Summary and Takeaway Thoughts

- NO heat-sinks were employed during evaluation of DUT and control samples
  - Air was moved across bare, unaltered, exposed die
- All devices remained operational after completion of test runs
- TID tested sample continues to read "hot" after 3 months (current time since test)
  - Unknown: how voltage and temperature readings impact these parts beyond tested level
- Positive side effect of using laptop platform:
  - Portability is a given
  - Power consumption (Battery Drain) can be recorded alongside other statistics
- Negatives:
  - Restricted laptop mainboard feature set limits access to device features and other useful performance stats found in desktop systems
- Software Test Platform:
  - Lends itself well to TID testing, where apparent hardness of these parts allows insight into various operational behaviors
  - But, requires more refinement to achieve similar level of detail in fault-rich conditions like protons and heavy ions

Note: future testing is planned to gather more data on both proton and total dose performance on additional samples of this device.

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References available in final paper.