Preliminary Radiation Testing of a State-of-the-Art Commercial 14nm CMOS Processor / System-on-a-Chip

Carl M. Szabo, Jr., Adam Duncan, Kenneth A. LaBel, Matt Kay, Pat Bruner, Mike Krzesniak, Lei Dong

Abstract— Hardness assurance test results of Intel state-of-the-art 14nm "Broadwell" U-series processor / System-on-a-Chip (SoC) for total ionizing dose (TID) are presented, along with exploratory results from trials at a medical proton facility. Test method builds upon previous efforts [1] by utilizing commercial laptop motherboards and software stress applications as opposed to more traditional automated test equipment (ATE).

***Index Terms*— radiation, total ionizing dose, 14nm, SoC, processor, proton-induced effects, commercial motherboard, software stress testing, test method.**

I. Introduction

Commercial processors are an intense topic of interest for the space community. As technologies and manufacturing processes have advanced in response to the free market demand, the resulting innovations offer a tantalizing set of benefits to space users. These are: high-performance, low-cost, and a trend toward better radiation tolerance as feature sizes shrink.

TABLE I: HISTORICAL HARDNESS OF PROCESSOR TECHNOLOGIES
modified from K. LaBel, et al. [1].

Device	Technology*	Test Date	Result	Ref.
Intel 80386-20	1 µm CHMOS IV	1993	Failure Between 5-7.5 krad(Si)	[2]
Intel 80486DX2-66	0.8 µm CHMOS V	1995	Failure Between 20-25 krad(Si)	[3]
Intel Pentium III	0.25 µm	2000	Failure ~ 500 krad(Si)	[4]
AMD K7	0.18 µm	2002	Failure > 100 krad(Si)	[4]
AMD Llano	32 nm	2013	No Failures 1, 4, 17 Mrad(Si)	[1],[5]

* = all technologies are complementary metal-oxide semiconductor (CMOS).The H in CHMOS stands for high-density.

However tantalizing these benefits may appear, there is usually a caveat that hinders the mass adoption of these products in space missions. In particular, the power and thermal consumption of the processor. A relatively trivial problem for terrestrial users, where countermeasures like air conditioning, heat-sinks and fans are plentiful, these power and heat obstacles not only can make these processors impractical for spacecraft, but also impractical to test within modern facilities without specially fabricated heat-removal options.

With the advent of Intel's present day 14nm "Broadwell" line-up, users may begin realizing a new benefit: low-power, and with that, lower heat output. The Device Under Test (DUT) for this report is a 15-Watt design, but alternative products on this same process offer as low as 4.5-Watt Thermal Design Power (TDP). These parts are the first Core™ processor family fan-less offerings to the mainstream market.

In order to achieve this benefit, the traditional, planar transistor design was abandoned in favor a "Tri-gate", or Intel's variant of Fin-Shaped Field Effect Transistor (FinFET) three-dimensional design. This technology became available in 2012 with the introduction of the 22nm "Ivy Bridge" processor line-up, and has been further refined in the current Broadwell series (second generation 14nm Tri-gate).

Unfortunately, and likely unintentionally, while one caveat may have been eliminated, a new one has spawned in its place. To slightly twist a quote attributed to Voltaire: "With great (low) power, comes great responsibility". How does this technology compare to the previously studied planar designs under irradiation? And, how viable is this FinFET design for an application that is intended to perform above and beyond the capability of a CubeSAT?

Intel stipulates that its processors are not intended for high-reliability applications, and this fact is generally understood when it comes to designing potential spacecraft. However, this major limitation does not preclude the community from characterizing the technology. The change in process from planar to three-dimensional design, on its own, warrants further study, given how relatively young it is.

The goal of this work is to elucidate possible areas of weakness by leveraging retail and freeware software to exercise the DUT in the presence of radiation. The results, while performed at the system level, will hopefully aid future researchers and add to our realm of knowledge of these sophisticated devices.

This work was supported by the NASA Electronic Parts and Packaging Program (NEPP), in collaboration with Naval Surface Warfare Center Crane.

Carl M. Szabo, Jr. is with AS&D, Inc. (ASRC Federal Space and Defense), 7515 Mission Drive, Suite 200, Seabrook, MD 20706, work performed for NASA Goddard Space Flight Center (GSFC), Greenbelt, MD 20771 (USA), phone: 301-286-8890, email: carl.m.szabo@nasa.gov.

Adam Duncan, Matt Kay, Pat Bruner, and Mike Krzesniak are with NSWC Crane, Crane, IN, 47522 (USA), emails: adam.duncan@navy.mil, matthew.kay@navy.mil, patrick.bruner@navy.mil, and michael.krzesniak@navy.mil.

Kenneth A. LaBel, is with NASA/GSFC, Code 561.4, Greenbelt, MD 20771 (USA), phone: 301-286-9936, email: kenneth.a.label@nasa.gov

Lei Dong is with Scripps Proton Therapy Center, San Diego, CA 92121 (USA), email: dong.lei@scrippshealth.org.

Submitted to the Institute of Electrical and Electronics Engineers (IEEE) Nuclear and Space Radiation Effects Conference (NSREC), Radiation Effects Data Workshop, Boston, Massachusetts, July 15, 2015.

II. Device Under Test

The DUT utilized is a modern state-of the-art SoC with the codename Broadwell-U from Intel Corporation [6]. The device part number is: FH8065801884006, also known as Core™ i3-5005U. This is a 2.0 GHz dual-core, dual-thread processor with 3 MB of shared cache, integrated floating point, graphics and input/output control via Platform Controller Hub (PCH). The processor is packaged in a non-lidded 1168-ball micro Flip-Chip Ball Grid Array with distinct dies for the PCH functions and the combined arithmetic/logic and graphical functions. The device utilizes Intel's 2nd generation Tri-gate technology by way of a 14nm process and has nominally a 15 Watt thermal design power. Maximum operating temperature is 105 degrees Celsius.

On-chip peripherals include a dual-channel Dual Data Rate Generation 3 Low Voltage (DDR3L) memory controller, a 12-lane PCI Express 2.0 controller and high definition graphics controller with support for up to 3 displays, all in a 40 mm x 24 mm x 1.284 mm package.

The size of the processor and graphics die is 13.4 mm x 6.0 mm, while the PCH die is 6.1 mm x 8.4 mm [7].

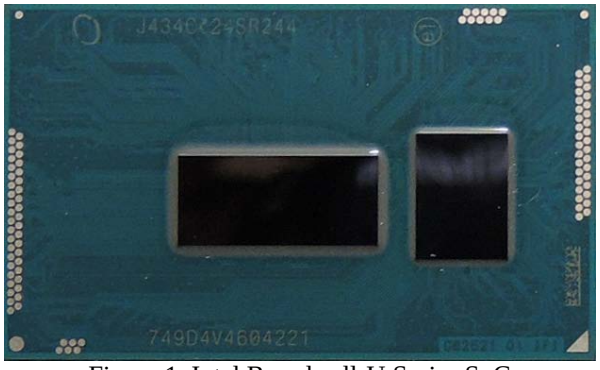


Figure 1. Intel Broadwell-U Series SoC

Intel maintains many fabrication sites. At this time, three such sites are producing parts at the 14nm level. Whether the chosen DUT was produced in Oregon, USA, Arizona USA, or Leixlip, Ireland, is unknown.

III. Facilities Utilized

A Northstar X5000 [8] Computed Tomography (CT) 225 KeV X-ray chamber located at NAVSEA Crane [9] was used to perform TID testing.

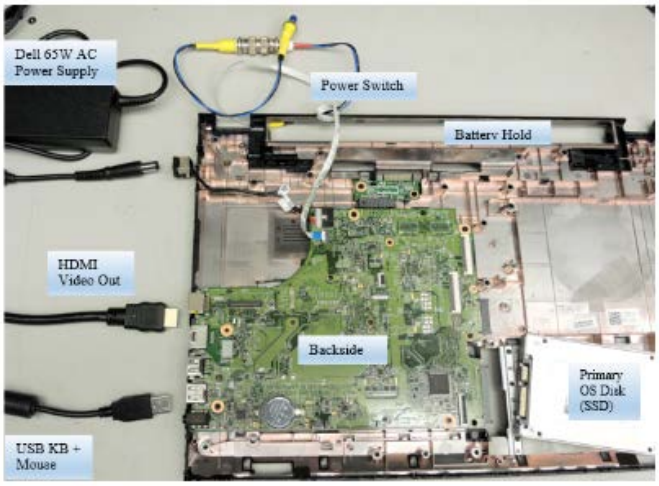
Proton testing was performed at SCRIPPS Medical Proton Facility, in San Diego, CA. This site was chosen for evaluation by a NASA / U.S. government / industry collaborative effort to investigate feasibility of U.S. Proton Cancer Facilities in wake of the Indiana University Cyclotron closure in late 2014 [21]. SCRIPPS features a 90-ton cyclotron whose beamline can be directed to provide a range of 70-245 MeV Protons to 5 treatment rooms via computer console [10].

IV. Test Setup

A. General Test Setup

Commercially available Inspiron 3000 series laptops [11] were procured from Dell. These units were partially dismantled to serve as test fixtures. The folding display panel, touch pad device, heat-sink, fan, and other externally connected ribbon interfaces were removed, while the motherboard, power connector, factory installed 4GB DDR3L memory, and battery were retained. Video was sent via onboard High-Definition Multimedia Interface (HDMI) port and control was maintained via available soldered-on Universal Serial Bus (USB) connector.

Excess thermal compound was removed from the dies and a server-grade 8000RPM external 60mm fan was utilized to provide cooling in lieu of the missing heat-sink. Power was supplied from an external source providing a basic 12V Molex connector. Neither the processor nor PCH die was thinned.



(a)

(b)

Figure 2. Partially Assembled Test Fixture and Block Diagram, Back Side (a) and Assembled Fixture, Front Side (b)

An Operating System (OS), based on the "Windows to Go" concept [12] introduced by Microsoft with the Windows 8 product, was installed onto a 512GB Samsung 850 PRO series Solid State Disk (SSD). Windows Server 2012R2 was selected for its error reporting capabilities instead of Windows 8.1. The advantage of this setup was to be able to run natively from the onboard Serial Advanced Technology Attachment (SATA) interface AND/OR the USB 2.0 or 3.0 ports, if needed.

Various supporting software was executed, either interactively, or via batch scripting, to perform hardware stress testing or statistical logging.

TABLE II: SUPPORTING SOFTWARE

Title	Function
Microsoft Windows Server 2012 R2 [13]	Commercially available OS, Standard Edition, configured to be "portable".
HWiNFO64 [14]	Freeware hardware monitoring and on-board sensor logging tool.
Intel Optimized LINPACK Library [15]	Freely available stress computation and benchmarking software. Binaries are maintained by Intel and tailored to optimize the latest features on Intel products.
Geeks3D.com "FurMark" [16]	Freeware graphical stress tool – causes integrated graphics capabilities to consume power and dissipate heat.
Splinterware System Scheduler [17]	"Free Version" of the software tool was utilized to automate software steps that required interaction (i.e. key presses, custom log naming, dismissal of dialog windows)
PsTools [18]	Collection of command-line tools to facilitate system administration of OS

During testing, the systems were supplied power from the Dell-provided power adapter or battery.

B. Total Dose Test Setup

For total dose testing, the test fixture, as shown in figure 2, was mounted into the X-ray test chamber. Cabling for keyboard/mouse, video, power switch, and Dell power source were fed to a user area.

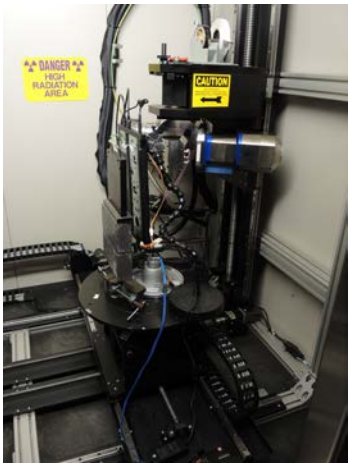
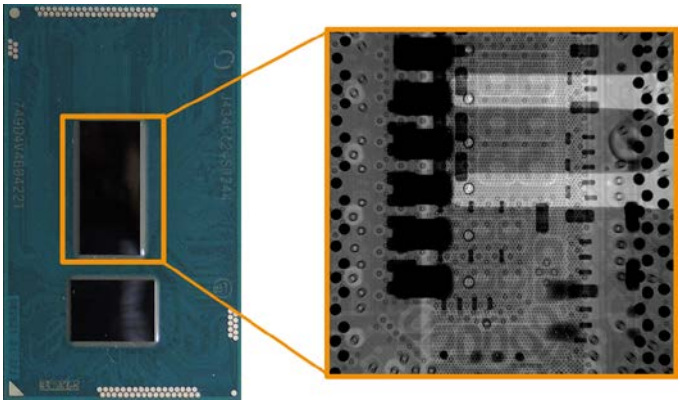


Figure 3. Test Fixture Mounted in X-Ray Chamber

Upon setup of the test fixture, thermo-luminescent dosimeters (TLDs) were placed around the DUT package so that the amount of radiation could be calculated. The goal was to achieve a rate of at least 10 krad(Si) per minute, so the beam was focused on the computational and graphical die instead of the entire package. Calculation of the TLD readings confirmed that the DUT target was receiving ~10.8 krad(Si) per minute.

(a)



(b)

Figure 4. TLDs Placed on DUT (a) and Actual X-ray Targeted Area of Package (b)

During in-situ exposure, the system was powered by the provided Dell power source and booted to Windows. HWiNFO64 was utilized to record DUT performance statistics during the irradiation, logging readings every 2 seconds.

When the desired dose step was reached, the X-ray source was stopped, HWiNFO64 was stopped, and the system was gracefully shut down. After a brief 2-3 second delay, the Dell power source was unplugged, and the system was started under battery power. When Windows was restarted, a series of batch files invoked HWiNFO64 again, and spawned the LINPACK stress test. Unlike the exposure step, the battery drain in Watts was recorded to provide insight into the actual energy needs of the motherboard, which should almost exclusively be that of the processor. A graphical stress test using the FurMark tool would loop on and off periodically as the LINPACK stress test

exercised the DUT. Logging continued until the stress test calculation was completed.

If the LINPACK result remained consistent, the system was gracefully shut down again. The power source was plugged in, and the system was restarted to repeat in-situ logging until the next exposure step.

This process repeated for as long as time and labor would allow.

C. Proton Facility Test Setup

At SCRIPPS, the test fixture was placed on a patient examination table, with necessary power, video, and USB cables connected to a user control area. A cooling fan running at 8000 revolutions per minute (RPM) was affixed to the side, utilizing an existing exhaust pathway to provide cool air across the face of the DUT.

Once the fixture was secured, the DUT was aligned by laser to be properly targeted by the proton beam. After acquiring the target, the control room could prepare parameters for beam requests.

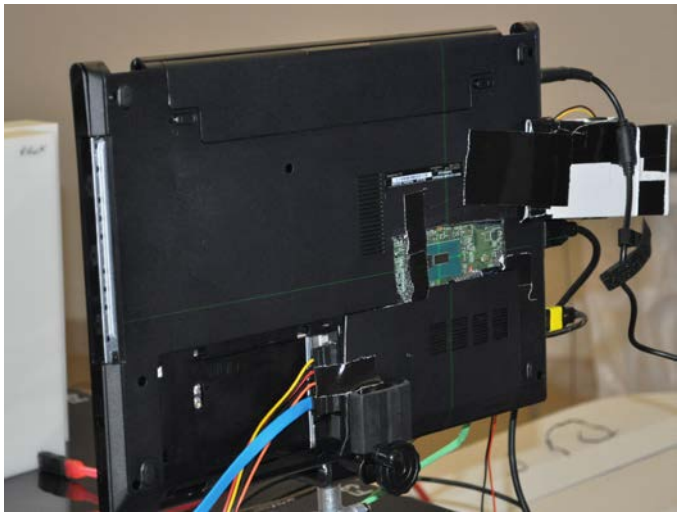


Figure 5. Test Fixture Undergoing Laser Alignment

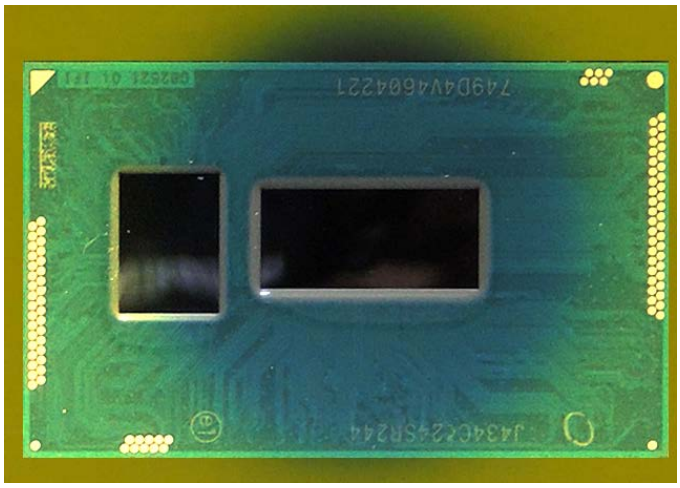


Figure 6. Radiographic Film Overlay on Example DUT Showing Non-Scattered Beam Signature

During exposure to the proton beam, three test methods were implemented:

Method 1: With the test fixture running the OS at idle, record performance statistics with HWiNFO64.

Method 2: With the test fixture running only the LINPACK executable, record performance statistics with HWiNFO64.

Method 3: With the test fixture running LINPACK and periodically cycling FurMark (akin to the stress test that was utilized during previous Total Dose testing), record performance statistics with HWiNFO64.

Under all methods, the objective was to complete the test and record whether the system remained operational throughout the duration of exposure to the beam. If the test fixture experienced a crash, encountered an unexpected reset, or ceased to respond to operator control, the test run was halted and the delivered dose was recorded.

After all tests were performed, the OS system-level log files were scoured for details about crashes, memory dumps, or other notable behaviors.

V. RESULTS

A. Total Dose Test Results

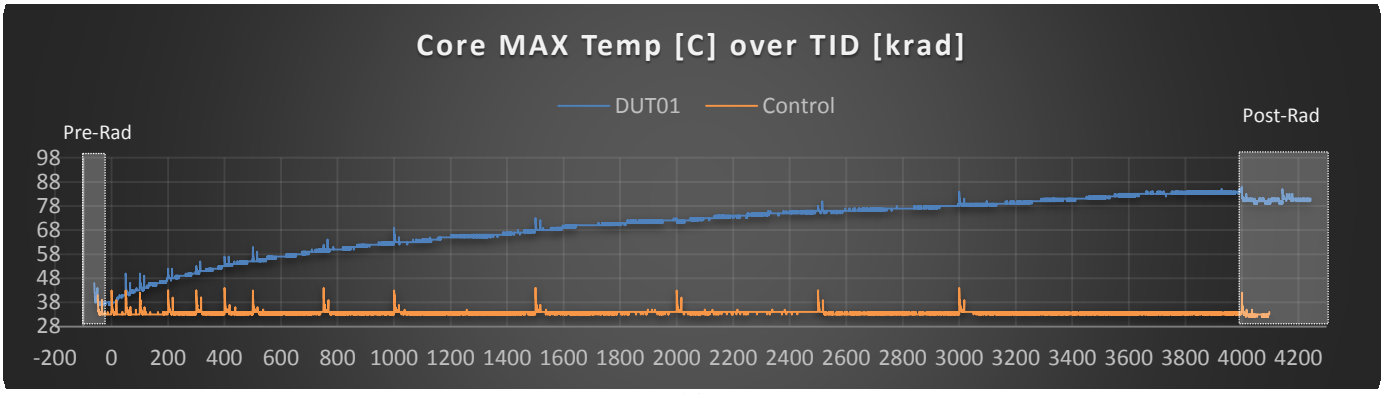
Initial results from total dose testing revealed a behavior observed previously on the earlier planar device designs [1],[5]. Specifically, the DUT's on-die thermal sensor began to report incorrectly high temperatures early into the non-stress exposure steps (figure 7a). The sensor continued to report progressively higher temperatures, while, paradoxically, the DUT reported decreasing voltage levels as exposure levels increased (figure 8a). The control part behaves consistently under non-stress, conditions, save for one anomaly, which is believed to be the result of a high duty spike during the boot process, causing the Adaptive Thermal Monitor [19] to limit the operating frequency.

When graphed, the contrast of behaviors from the DUT and control sample is glaring. Prior to exposure, the DUT and control parts behave in similar fashion (figures 7b and 8b), whereas post exposure, the DUT continues to report that its temperature is elevated (figure 7c). Meanwhile, the control part reflects the expected response to operation in a "room temperature" environment.

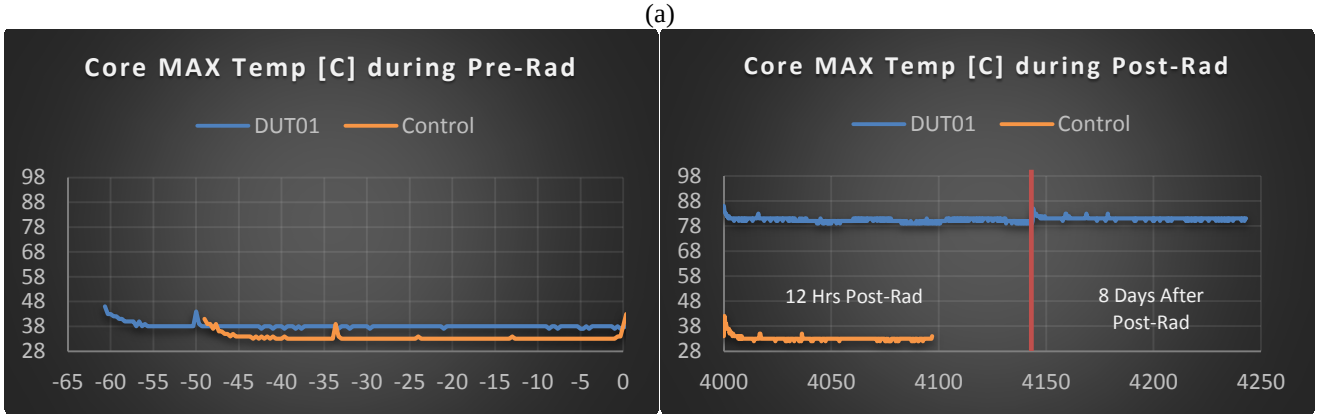
Nonetheless, the DUT continued to pass the LINPACK stress test consistently to highest tested dose levels.

Rather unexpectedly, the LINPACK stress tests completed faster on the irradiated DUT in comparison to the control. Overall, the DUT outperformed the control device on all but 3 iterations of the stress test, with a series of quicker completion times occurring from the 200k – 1.5 Mrad(Si) exposure levels, followed by another streak at the 2.5 – 3 Mrad(Si) levels.

Additionally, the DUT showed decreases in voltage over the course of stress testing (figures 9a and 9b), while demonstrating increased battery drain, as shown in figure 10.

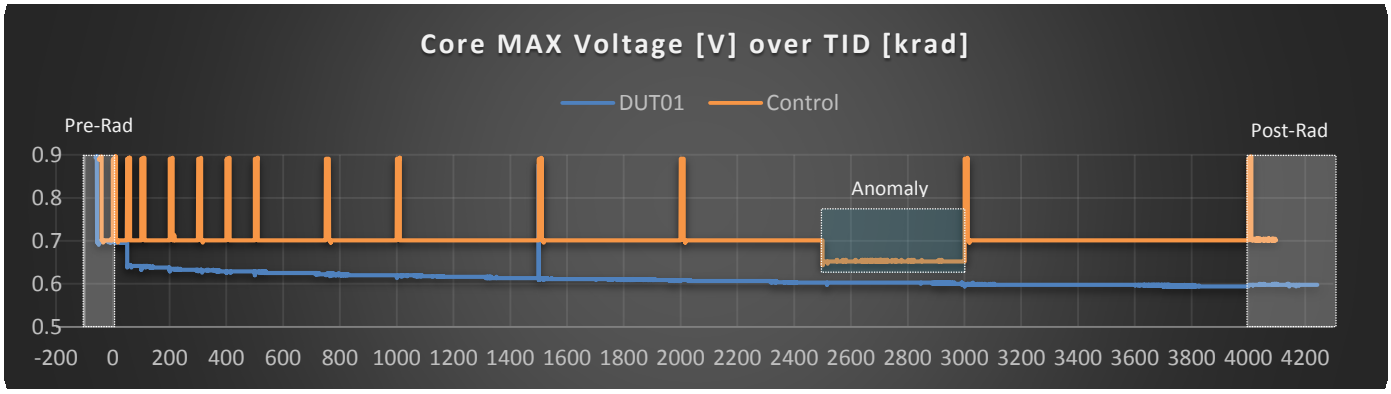


(a)

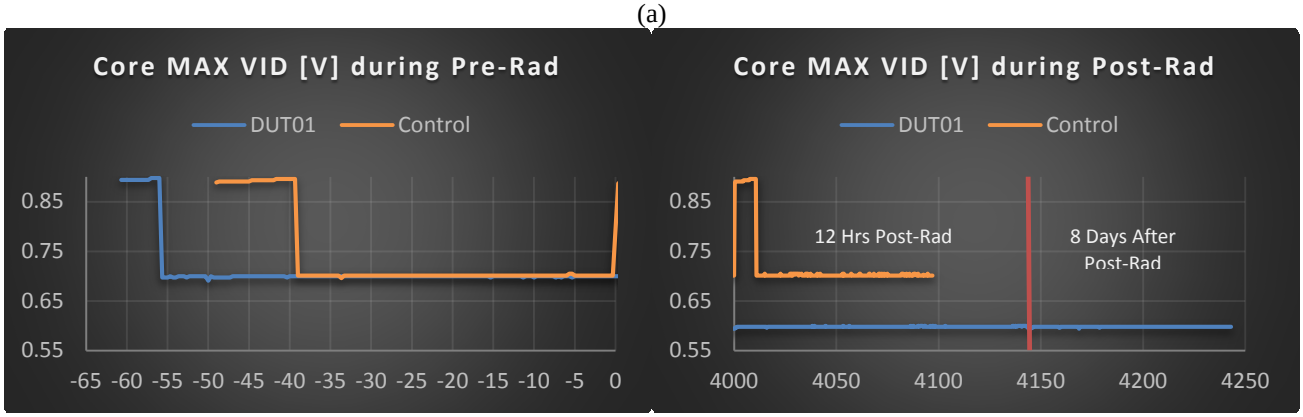


(b) (c)

Figure 7. Comparison of Reported Maximum Temperature Readings of DUT and Control during non-Stress irradiation (a), with Zoomed-In results isolating pre-exposure behavior (b) and post-exposure behavior (c)



(a)



(b) (c)

Figure 8. Comparison of Reported Maximum Voltage Identifier Readings of DUT and Control during non-Stress irradiation (a), with Zoomed-In results isolating pre-exposure behavior (b) and post-exposure behavior (c)

TABLE III: DOSE LEVELS WITH BATTERY DRAIN AND LINPACK PERFORMANCE

Dose Level	DUT Avg. Batt. Drain (W)	Control Avg. Batt. Drain (W)	DUT LINPACK Time (s)	Control LINPACK Time(s)	DUT LINPACK GFlops	Control LINPACK GFlops
0K (Pre-Rad)	4.869	4.992	279.233	325.226	6.7441	5.7903
50K	4.683	4.973	287.543	294.652	6.5492	6.3912
100K	4.893	4.942	296.568	285.84	6.3498	6.5882
200K	4.525	5.129	265.096	299.36	7.1037	6.2906
300K	4.732	5.118	260.46	289.263	7.2302	6.5102
400K	4.668	5.080	264.422	284.394	7.1218	6.6217
500K	4.852	5.084	268.555	306.662	7.0122	6.1408
750K	4.627	5.091	259.631	305.746	7.2532	6.1592
1M	4.820	4.981	260.323	304.19	7.234	6.1907
1.5M	4.974	5.009	265.909	282.004	7.082	6.6778
2M	4.905	5.003	304.87	301.871	6.1769	6.2383
2.5M	4.845	4.996	234.362	315.318	8.0353	5.9723
3M	5.075	5.050	264.739	320.198	7.1133	5.8812
4M	5.105	5.048	316.455	302.024	5.9508	6.2351
4MPOST12HR (Post-Rad)	5.209	4.963	277.687	283.09	6.7816	6.6522
4MPOST8DAYS (Post-Rad)	5.071		265.058		7.1047	
Mean	4.866	5.031	273.182	299.989	6.9277	6.2893
Standard Deviation	0.190	0.059	20.097	13.574	0.4989	0.2818

(a)

(b)

Figure 9. Reported Maximum Voltage Identifier Readings of DUT (a) contrasting those reported by Control sample (b) during post-irradiation Stress Testing

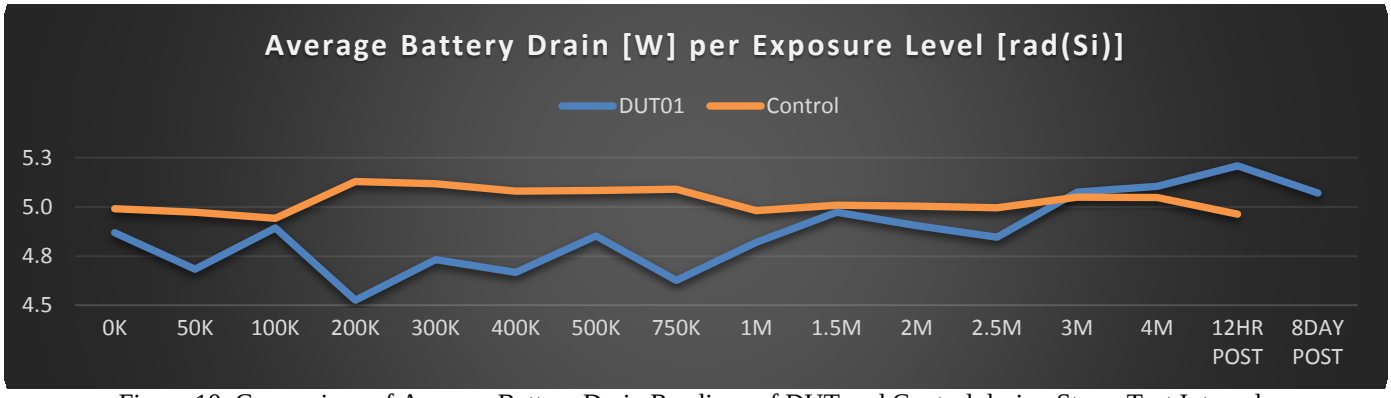


Figure 10. Comparison of Average Battery Drain Readings of DUT and Control during Stress Test Intervals

Due to time constraints at the facility, we were unable to achieve a total dose beyond 4 Mrad(Si). The authors plan to reconvene and test additional DUTs beyond 4 Mrad(Si) to observe more behaviors and/or until a failure is achieved.

No failures with the DUT or control samples were encountered, and no failures occurred on any supporting hardware, such as the DDR3L memory, SSD, power supply, or battery.

The test data suggests that this device, at least up to 4 Mrad(Si) TID, is able to perform computations accurately despite incorrect thermal die readings and paradoxically decreasing voltage alongside increasing power consumption levels.

B. Proton Facility Test Results

As time allowed, a series of test runs were performed, mostly with 200 MeV protons and no scattering. Two final runs used 220MeV protons with a 7mm lead scatter.

During these test runs, three types of events were observed: System Crashes (Fatal Errors (FE)), Recoverable (Non-Fatal Errors (NFE), and Video Output Disruptions (Graphical "Glitches"). The occurrence of events in the last category, Graphical Glitches, was observed on-screen and noted, as they could not be accurately counted.

The possibility exists that other events may have appeared while escaping detection, such as FEs or NFEs occurring in conjunction with an immediate reset of the system. Unfortunately, the OS cannot record events when it is not allowed a sufficient opportunity to do so.

Lastly, to reemphasize the preliminary nature of these results: limited test time, coupled with limited statistics, forces us to provide somewhat simplistic proton see test data.

As one would expect, when the test fixture was operating the DUT at idle (non-stress), when there is little to no activity taking place within the processor, this part is least susceptible to proton exposure, giving a FE cross section of around $10^{-9}cm^2$. By contrast, both stress test types revealed about an order of magnitude higher sensitivity cross sections bordering on 1 to $2x10^{-8}cm^2$.

NFE cross-sections for idle and math-only tests were approximately $3x10^{-9}cm^2$ with the combined math and graphics stress test results approximately $1x10^{-8}cm^2$.

At the end of testing, despite the DUT (and test platform) encountering many FE conditions, no hard device failures occurred. Environment and performance statistics suggested no tendency toward unusual thermal, voltage, or power readings. Surprisingly, the supporting hardware (DDR3L, SSD, power supplies, and fan) also continued to function nominally.

Worth noting is the ability of the CPU to recover from certain types of cache error conditions. Most of the NFEs encountered were Level 1 and Level 2 instruction fetch operations of the processor cache. Meanwhile, many of the FEs were revealed to be Level 0 data eviction errors.

VI. DISCUSSION

One of the challenges with respect to performing single event testing of modern, SOTA processors, is the large collection of features integrated into the device. In fact, it may be slightly misleading to call these devices "processors", as this no longer describes what the device ***is***. Nowadays, the processor itself has become one of those integrated capabilities, situated alongside whatever else the chipmaker is compelled to include, thanks to the market shift toward SoCs. The processor just happens to be the element of the SoC whose characteristics we care about most.

While the inclusion of processing, graphics, input and output controllers, and data busses has provided some level of convenience to the consumer, products aimed toward the enterprise users must provide some measure of availability and resiliency [20] by means of soft error protection. The single event tester must be cognizant of these enhancements and be aware that certain problems may arise:

- The processor may internally correct errors caused by single particles; evidence of the correction may not be visible externally to the device,
- Other errors may be logged, such as cache or ECC memory errors, allowing the system to remain stable,
- Some errors may cause crashes to the system and cause a reboot before the problem can be recorded, and,

- The tester may be unable to disable one, many, or any of these protection mechanisms.

The methodology used for this testing represents a "best effort" approach to replace traditional custom bias boards and expensive ATE, but the tradeoff is that error visibility is only as good as the detail provided by the SoC, OS, stress, and test tools. The wildcard is whether or not the tester is able to procure, and thoroughly evaluate, a fully-featured, enthusiast motherboard that allows the tailoring of all or most device-level parameters.

The SoC manufacturer is able to afford both the ATE equipment and the labor required to develop test vectors due to commercial sales volumes (i.e., free market economics). However, being a commercial entity, the manufacturer also is not compelled to disseminate any hint of radiation hardness or related capability, other than, by way of legal (author-paraphrased) disclaimer: "We're not liable if you irradiate our products."

This approach, nonetheless, enables the community to investigate newly available products, using commonly available means to leverage integrated features. The fact that chip makers are catering to modern tastes in ultra-portable and tablet computers – while addressing the community's desire for low-power, low-heat, and high-performance – compels us to investigate these parts further. After all, if the products satisfy the needs of today's earthlings, perhaps they will, in turn, take interest in seeing our efforts succeed beyond Earth.

•••

Meanwhile, despite 3 months' time having passed since TID testing ceased, our sample DUT continued to report elevated temperatures. These readings ***did not change*** after the application of a heat-sink and thermally-conductive compound to the die surfaces.

•••

Follow-up tests are planned for further TID, Protons, and Heavy Ions. Continued trials will help determine limitations and advantages of software based system-level testing on state-of-the-art processors.

VII. SUMMARY

We have performed a series of total dose and exploratory proton irradiations on a 14nm commercial Intel processor, utilizing system-level tests that are conducted with commercial and free software tools. This work is a continuation of previous efforts supported by the NEPP Program and builds upon successful collaborations with NSWC Crane and other entities. The authors look forward to future tests on these and other parts.

VIII. ACKNOWLEDGMENTS

The authors would like to thank the NASA Electronic Parts and Packaging Program and Naval Surface Warfare Center Crane for their support.

IX. REFERENCES

[1] Kenneth A. LaBel, Robert A. Gigliuto, Carl M. Szabo, Jr., Martin A. Carts, Matthew Kay, Timothy Sinclair, Matthew Gadlage, Adam Duncan, and Dave Ingalls," Hardness Assurance for Total Dose and Dose Rate Testing of a State-Of-The-Art Off-Shore 32 nm CMOS Processor," https://nepp.nasa.gov/files/24951/NSREC2013_LaBel_W40L.pdf, Jul. 2013.

[2] K. Sahu, "Radiation Report on TRMM/GPEP Part No. MQ80386-20, PPM-93-062," http://radhome.gsfc.nasa.gov/radhome/papers/tid/PPM-93-062.pdf, Jun. 1993.

[3] Donald R. Johnson, "Total Dose Test Report on the Intel 80486DX2-66 Microprocessor tested 8/29-9/8/95," http://radhome.gsfc.nasa.gov/radhome/papers/td80486.htm, Sept. 1995.

[4] Jim Howard, Ken LaBel, Marty Carts, Ron Stattel, Charlie Rogers, Tim Irwin, and Zoran Kahric, "Total Ionizing Dose Testing of the Intel Pentium III (P3) and AMD K7 Microprocessors," http://radhome.gsfc.nasa.gov/radhome/papers/tid/G020802_P3_TID.pdf, Feb. 2002.

[5] Kenneth A. LaBel, Martin A. Carts, Robert A. Gigliuto, Carl M. Szabo, Jr., Matt Kay, Tim Sinclair, Matt Gadlage, Adam Duncan, and Dave Ingalls, "Advanced Micro Devices (AMD) Processor: Radiation Test Results," presented at NEPP Electronics Technology Workshop, June 11-12, 2013.

[6] Intel® Core™ i3-5005U Processor (3M Cache, 2.00 GHz) http://ark.intel.com/products/84695/Intel-Core-i3-5005U-Processor-3M-Cache-2_00-GHz, 2015.

[7] 5th Generation Intel® Core™ Processor Family Mobile Thermal Mechanical Design Guide for Embedded Applications, http://www.intel.com/content/www/us/en/embedded/products/broadwell-u/5th-gen-core-mobile-embedded-thermal-mech-guide.html, Jan. 2015.

[8] X5000 | North Star Imaging, http://4nsi.com/systems/x5000, Jun. 2015.

[9] Federal Laboratory Consortium, Naval Surface Warfare Center – Crane Division, Laboratory Information, http://www.federallabs.org/labs/profile/?id=1374, Jun. 2015.

[10] Lei Dong, Luis Perles, "Proton Beam Test for Electronics and Aerospace Programs," presented at 2015 Single Event Effects (SEE) and Military and Aerospace Programmable Logic Devices (MAPLD) Special Proton Session, May 20, 2015.

[11] Inspiron 15 3543 Specifications, http://downloads.dell.com/Manuals/all-products/esuprt_laptop/esuprt_inspiron_laptop/inspiron-15-3543-laptop_Reference%20Guide_en-us.pdf, Mar. 2015.

[12] Chris Hoffman, "How to Create a Windows To Go USB Drive Without the Enterprise Edition," http://www.howtogeek.com/196817/how-to-create-a-windows-to-go-usb-drive-without-the-enterprise-edition/, Sept. 2014.

[13] Windows Server 2012 R2 overview, http://www.microsoft.com/en-us/server-cloud/products/windows-server-2012-r2/, Jun. 2015.

[14] Professional System Information and Diagnostics, HWiNFO32™ / HWiNFO64™ - Powerful system information tools for Windows, http://www.hwinfo.com, Jun. 2015.

[15] Intel® Math Kernel Library – LINPACK Download, https://software.intel.com/en-us/articles/intel-math-kernel-library-linpack-download, Jun. 2015.

[16] FurMark: VGA Stress Test, Graphics Card and GPU Stability Test, Burn-in Test, OpenGL Benchmark and GPU Temperature, http://www.ozone3d.net/benchmarks/fur/, Jun. 2015.

[17] FREE - System Scheduler, task scheduler alternative for Microsoft Windows, http://www.splinterware.com/products/wincron.htm, Jun. 2015

[18] TechNet (TN) PsTools, https://technet.microsoft.com/en-us/sysinternals/bb896649.aspx, Jun. 2015

[19] 5th Generation Intel® Core™ Processor Family Datasheet Vol. 1, http://www.intel.com/content/www/us/en/processors/core/5th-gen-core-family-datasheet-vol-1.html, p. 66, Jun. 2015.

[20] Intel® Xeon® Processor D Product Family Technical Overview | Intel® Developer Zone, https://software.intel.com/en-us/articles/intel-xeon-processor-d-product-family-technical-overview#_Toc419802873, Jun. 2015

[21] B. S. Wie, K. A. Label, T. L. Turflinger, A. D. Kostic, R. A. Reed, C. C. Foster, J. L. Wert, J. S. George, "Evaluation and Application of U.S. Medical Proton Facilities for Single Event Effects Test", to be presented at IEEE Nuclear and Space Radiation Effects Conference (NSREC), Jul. 2015.