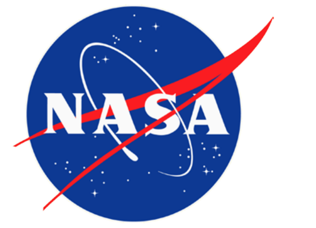
Martha O'Bryan

Compendium of Current Single Event Effects for Candidate Spacecraft Electronics for NASA

Martha V. O'Bryan[1], Kenneth A. LaBel[2], Dakai Chen[2], Michael J. Campola[2], Megan C. Casey[2], Jean-Marie Lauenstein[2], Jonathan A. Pellish[2], Raymond L. Ladbury[2], Melanie D. Berg[1]

1. AS&D, Inc.; 2. NASA GSFC

National Aeronautics and Space Administration



Abstract: We present the results of single event effects (SEE) testing and analysis investigating the effects of radiation on electronics. This paper is a summary of test results.

Introduction

NASA spacecraft are subjected to a harsh space environment that includes exposure to various types of ionizing radiation. The performance of electronic devices in a space radiation environment are often limited by their susceptibility to single event effects (SEE). Ground-based testing is used to evaluate candidate spacecraft electronics to determine risk to spaceflight applications. Interpreting the results of radiation testing of complex devices is challenging. Given the rapidly changing nature of technology, radiation test data are most often application-specific and adequate understanding of the test conditions is critical [1].

Studies discussed herein were undertaken to establish the application-specific sensitivities of candidate spacecraft and emerging electronic devices to single-event upset (SEU), single-event latchup (SEL), single-event gate rupture (SEGR), single-event burnout (SEB), and single-event transient (SET).

For total ionizing dose (TID) and displacement damage dose (DDD) results, see a companion paper submitted to the 2015 Institute of Electrical and Electronics Engineers (IEEE) Nuclear and Space Radiation Effects Conference (NSREC) Radiation Effects Data Workshop (REDW) entitled "Compendium of Current Total Ionizing Dose and Displacement Damage for Candidate Spacecraft Electronics for NASA" by M. Campola, et al. [2].

Test Techniques and Setup

A. Test Facilities

All tests were performed between February 2014 and February 2015. Heavy ion experiments were conducted at the Lawrence Berkeley National Laboratory (LBNL) [3], and at the Texas A&M University Cyclotron (TAMU) [4]. Both of these facilities provide a variety of ions over a range of energies for testing. Each device under test (DUT) was irradiated with heavy ions having linear energy transfer (LET) ranging from 0.6 to 120 MeV•cm^2/mg. Fluxes ranged from 1x10^2 to 1x10^5 particles/cm^2/s, depending on device sensitivity. Representative ions used are listed in Table I and II. LETs in addition to the values listed were obtained by changing the angle of incidence of the ion beam with respect to the DUT, thus changing the path length of the ion through the DUT and the "effective LET" of the ion [5]. Energies and LETs available varied slightly from one test date to another.

Laser SEE tests were performed at the pulsed laser facility at the Naval Research Laboratory (NRL) [6], [7]. Single photon absorption method was used with the laser light having a wavelength of 590 nm resulting in a skin depth (depth at which the light intensity decreased to 1/e – or about 37% – of its intensity at the surface) of 2 μm. A nominal pulse rate of 1 kHz was utilized. Pulse width was 1 ps, beam spot size ~1.2 μm.

Table I: LBNL Test Heavy Ions

Ion	Energy (MeV)	Surface LET in Si (MeV•cm^2/mg) (Normal Incidence)	Range in Si (μm)
^{18}O	183	2.2	226
^{22}Ne	216	3.5	175
^{40}Ar	400	9.7	130
^{23}V	508	14.6	113
^{65}Cu	660	21.2	108
^{84}Kr	906	30.2	113
^{107}Ag	1039	48.2	90
^{124}Xe	1233	58.8	90
LBNL 10 MeV per amu tune			

Table I: TAMU Test Heavy Ions

Ion	Energy (MeV)	Surface LET in Si (MeV•cm^2/mg) (Normal Incidence)	Range in Si (μm)
^{14}N	210	1.3	428
^{20}Ne	300	2.5	316
^{40}Ar	599	7.7	229
^{63}Cu	944	17.8	172
^{84}Kr	1259	25.4	170
^{109}Ag	1634	38.5	156
^{129}Xe	1934	47.3	156
^{197}Au	2954	80.2	155
TAMU 15 MeV per amu tune			
^{84}Kr	2081	19.8	332
^{139}Xe	3197	38.9	286
TAMU 25 MeV per amu tune			

amu = atomic mass unit

B. Test Method

Unless otherwise noted, all tests were performed at room temperature and with nominal power supply voltages. We recognize that for device qualification, high temperature and worst-case maximum operating voltage are recommended for SEL testing, whereas high temperature and worst-case minimum operating voltage are recommended for SEU/SET testing. Unless otherwise noted, SEE testing was performed in accordance with JESD57 test procedures where applicable [8].

1) SEE Testing - Heavy Ion:

Depending on the DUT and the test objectives, one or more of three SEE test approaches were typically used:

Dynamic – the DUT was continually exercised while being exposed to the beam. The events and/or bit errors were counted, generally by comparing the DUT output to an unirradiated reference device or with an expected output (Golden chip or virtual Golden chip methods) [9]. In some cases, the effects of clock speed or device operating modes were investigated. *Results of such tests should be applied with caution due to their application-specific nature.*

Static – the DUT was configured prior to irradiation; data were retrieved and errors were counted after irradiation.

Biased – the DUT was biased and clocked while power consumption was monitored for SEL or other destructive effects. In most SEL tests, functionality was also monitored.

DUTs were monitored for soft errors, such as SEUs and for hard failures, such as SEGR. Detailed descriptions of the types of errors observed are noted in the individual test reports [10], [11].

SET testing was performed using high-speed oscilloscopes controlled via LabVIEW®. Individual criteria for SETs are specific to the device and application being tested. Please see the individual test reports for details [10], [11].

Heavy ion SEE sensitivity experiments include measurement of the linear energy transfer threshold (LET_{th}) and cross section at the maximum measured LET. The LET_{th} is defined as the maximum LET value at which no effect was observed at an effective fluence of 1×10^7 particles/cm^2. In the case where events are observed at the smallest LET tested, LET_{th} will either be reported as less than the lowest measured LET or determined approximately as the LET_{th} parameter from a Weibull fit. In the case of SEGR experiments, measurements are made of the SEGR threshold V_{ds} (drain-to-source voltage) as a function of LET and ion energy at a fixed V_{gs} (gate-to-source voltage).

2) SEE Testing - Pulsed Laser Facility Testing

The DUT was mounted on an X-Y-Z stage in front of a 100x lens that produces a spot diameter of approximately 1 μm at full-width half-maximum (FWHM). The X-Y-Z stage can be moved in steps of 0.1 μm for accurate determination of SEU sensitive regions in front of the focused beam. An illuminator, together with a charge coupled device (CCD) camera and monitor were used to image the area of interest, thereby facilitating accurate positioning of the device in the beam. The pulse energy was varied in a continuous manner using a polarizer/half-waveplate combination and the energy was monitored by splitting off a portion of the beam and directing it at a calibrated energy meter.

Test Results Overview

Principal investigators are listed in Table III. Abbreviations and conventions are listed in Table IV. SEE results are summarized in Table V. Unless otherwise noted, all LETs are in MeV•cm^2/mg and all cross sections are in cm^2/device. All SEL tests are performed to a fluence of 1×10^7 particles/cm^2 unless otherwise noted.

Table III: List of Principal Investigators

Principal Investigator (PI)	Abbreviation
Melanie D. Berg	MB
Megan C. Casey	MCC
Michael J. Campola	MiC
Dakai Chen	DC
Raymond L. Ladbury	RL
Jean-Marie Lauenstein	JML
Jonathan A. Pellish	JP

Table IV: Abbreviations and Conventions

LET = linear energy transfer (MeV•cm^2/mg)
LET_{th} = linear energy transfer threshold (the maximum LET value at which no effect was observed at an effective fluence of 1x10^7 particles/cm^2 – in MeV•cm^2/mg)
< = SEE observed at lowest tested LET
> = no SEE observed at highest tested LET
σ = cross section (cm^2/device, unless specified as cm^2/bit)
σ_{maxm} = cross section at maximum measured LET (cm^2/device, unless specified as cm^2/bit)
ADC = analog to digital converter
BiCMOS = bipolar complementary metal oxide semiconductor
CMOS = complementary metal oxide semiconductor
DUT = device under test
ECC = error correcting code
eng samples = engineering samples
GPIB = general purpose interface bus
H = heavy ion test
ID# = identification number
I_{dss} = drain-source leakage current
I_{out} = output current
L = laser test
LBNL = Lawrence Berkeley National Laboratory
LDC = lot date code
min = minimum
MLC = multiple-level cell
MOSFET = metal-oxide-semiconductor field-effect transistor
NAND = Negated AND or NOT AND
NRL = Naval Research Laboratory
PCB = printed circuit board
PECL = positive emitter coupled logic
PI = principal investigator
PIGS = post-irradiation gate stress
PNP = positive-negative-positive
REAG = radiation effects and analysis group
SBU = single-bit upset
SEB = single event burnout
SEE = single event effect
SEFI = single-event functional interrupt
SEGR = single event gate rupture
SEL = single event latchup
SET = single event transient
SEU = single event upset
SiC = silicon carbide
SiGe = silicon germanium
SMART = self-monitoring, analysis and reporting technology
SSD = solid state drive
SSR = solid state relay
TAMU = Texas A&M University Cyclotron Facility
VCC = power supply voltage
VDMOS = vertical double diffused MOSFET
VDS = drain-to-source voltage
VGS = gate-to-source voltage
VNAND = vertical-NAND
Xe = Xenon

Table V: Summary of SEE Test Results

Part Number	Manufacturer	LDC, Wafer # or pkg markings	Device Function	Technology	Particle: (Facility/Year/Month) P.I.	Test Results: LET in MeV•cm^2/mg, σ in cm^2/device, unless otherwise specified	Supply Voltage	Sample Size (Number Tested)
Memory Devices:								
RM24	Adesto	No LDC	CBRAM	NonVolatile Memory	H: (LBNL14May; LBNL14Sep) DC L: (NRL14Jun) DC	H: SEL LET_{th} >83; 10 < SEU LET_{th} < 20; SEFI LET_{th} < 7.3; SEFI σ=5.9x10^{-7} cm^2 at LET 83; SEFIs can be recovered via power cycle in most cases, rewrite was required in some cases. Bit upsets were only observed in write/read mode. L: Laser test identified areas on the die that are sensitive to SEFI: bandgap reference, voltage regulator, SRAM, and logic circuits.	2.7 to 3.6 V	4
850 PRO series MZ7KE256HMHA	Samsung	No LDC	SSD	VNAND Flash Memory	H: (TAMU14Oct) DC	SEL LET_{th} >40; SEU LET_{th} < 1.8 SEFI LET_{th} < 1.8 SEFIs occurred during static and dynamic cycling test modes. Most SEFIs recoverable with power cycle. Some SEFIs caused data corruption, and required rewrite. Heavy ion-induced cell upsets were evident from reallocated sectors via ECC.	5 V	4
MN101L AM13L-STK2	Panasonic	No LDC	Microcontroller with Embedded Resistive Memory	ReRAM, 180 nm CMOS	H: (LBNL14May) DC; L: (NRL14Mar) DC	H: SEL LET_{th} > 70; 3.1 < SEFI LET_{th} < 4.4, σ = 4 × 10^{-5} cm^2/device at LET of 70. L: Pulsed-laser testing confirmed the SEU tolerance of the resistive memory array, and identified the sense amplifier as a sensitive component for SEFIs.	3.3V	3 at LBNL; 1 at NRL
Linear/Mixed Signal Devices:								
LM6172	Texas Instruments	1208A	Operational Amplifier	Bipolar	H: (TAMU13Dec; TAMU14Apr) MCC	SET 0.14< LET_{th} <0.87; σ_{maxm}=1×10^{-3} cm^2.	±5 V	2 (2013): 3 (2014)
AD7984	Analog Devices	C60	ADC	Bipolar	H: (TAMU14Oct) MiC	SEL LETth > 75.1; SET of 60 μs at LET >28.8 for given application.	2.5 V	4
MAX4595DVBR	Texas Instruments	pkg info SOT-23 6SB	Analog Switch	CMOS	H: (TAMU14Oct) MiC	SEL LET_{th} > 85; negative transients were observed ~2.5 μs long and -750 mV in amplitude; worst transient observed was 10 μs long and had negative going amplitudes of less than 1.5 V at LET 27.8	3.3V, 5V, 6V	3
MAX308ESE	Maxim	1108	Analog Multiplexer	CMOS	H: (TAMU14Oct) MiC	SEL LET_{th} > 89 [20]]	+/-15V	1
TLV5618	Texas Instruments	0801A	ADC	CMOS	H: (TAMU14Oct) RL	8.1< SEL LET_{th} <11.4 σ_{maxm}~6×10^{-5} cm^2; SET LET_{th} <1.8, σ_{maxm} ~2×10^{-4} cm^2; 3.6< SEU LET_{th}<5.5, σ_{maxm} ~1.5×10^{-5} cm^2.	5 V; 6 V	2
ADP3330	Analog Devices	1238	Voltage Regulator	BiCMOS	H: (TAMU14Oct) RL	SEL LET_{th} >53.1; 28.8< SET LET_{th} <53.1, σ_{maxm} ~1.5×10^{-5} cm^2; packaging precluded testing at angle.	3.3 V	2
LMV7219	Texas Instruments	1249	Comparator	BiCMOS	H: (TAMU14Oct) RL	SEL LET_{th} >53.1; SET LET_{th} < 2.8, σ not saturated at LET=53.1; LET and cross section depend on input voltage ΔV_{in}; transients can last up to several microseconds.	5 V	3
AZ88923	Arizona Microtek	0146	Integrated Circuit	SiGe PECL	H: (TAMU15Oct) RL	SETs with durations up to 10 microseconds were observed at LET ~17. SET LET_{th} <1.8; SET σ_{maxm} 1.1x10^{-4} cm^2.	3.3 V	3
Power Device:								
SMHF2812	Crane Interpoint	1021, 1214	DC-DC Converter	Hybrid	H: (TAMU14Jul) MCC	No destructive SEEs observed at 44 MeV-cm^2/mg in either LDC. [25]	28 V, 35 V	6
CMF10120D	CREE	W52812	MOSFET	SiC VDMOS	H: (LBNL14Sept) JML; MCC	966-MeV Xe (LET=65 in SiC): min evaluated Vds=182 V: Failed Idss and PIGS tests; at higher V_{DS}, primary failure mode SEB.	0 V_{GS}	11
SCT30N120	STMicroelectronics	No LDC (eng samples)	SiC MOSFETs	SiC VDMOS	H: (LBNL14June) JML	Contact PI for test results.	0 V_{GS}	24
Diodes – Pass at 100% of Reverse Voltage:								
FYPF2010DN	Fairchild Semiconductor	14-032; E13AA wafer	Diode	Si	H: (LBNL14June) MCC	No failures observed at 100% of reverse voltage when irradiated with 1233 MeV Xe (LET = 58.8).	100 V	3
MBR4045WT	ON Semiconductor	14-040; NFB19G wafer	Diode	Si	H: (LBNL14June) MCC	No failures observed at 100% of reverse voltage when irradiated with 1233 MeV Xe (LET = 58.8).	45 V	3
RB205T-60	Rohm Semiconductor	14-023; No LDC	Diode	Si	H: (LBNL14June) MCC	No failures observed at 100% of reverse voltage when irradiated with 1233 MeV Xe (LET = 58.8).	60 V	3
MBR4045CT	Vishay	14-025; P350X wafer	Diode	Si	H: (LBNL14June) MCC	No failures observed at 100% of reverse voltage when irradiated with 1233 MeV Xe (LET = 58.8).	45 V	3
Diodes – Degradation and Pass at 100% of Reverse Voltage:								
MBR2080CT	ON Semiconductor	14-043; NF914 wafer	Diode	Si	H: (LBNL14June) MCC	Degradation observed during beam run while biased at 100% of reverse voltage, but all parameters remained within specification when irradiated with 1233 MeV Xe (LET = 58.8).	80 V	3
Diodes – Degradation and Failure at 100% of Reverse Voltage:								
MBRF2045CT	ON Semiconductor	14-039; SPB17 wafer	Diode	Si	H: (LBNL14June) MCC	Degradation observed during beam run while biased at 75% of reverse voltage, but all parameters remained within specification when irradiated with 1233 MeV Xe (LET = 58.8). Degradation was also observed during beam run when biased at 100% of reverse voltage, but parameters exceeded specification.	45 V	4
MBR6045WT	ON Semiconductor	14-041; NFE04G wafer	Diode	Si	H: (LBNL14June) MCC	Degradation observed during beam run while biased at 75% of reverse voltage, but all parameters remained within specification when irradiated with 1233 MeV Xe (LET = 58.8). Degradation was also observed during beam run when biased at 100% of reverse voltage, but parameters exceeded specification.	45 V	4
Diodes – Catastrophic Failure at 100% of Reverse Voltage:								
MBRF20100CT	ON Semiconductor	14-044; SPB16 wafer	Diode	Si	H: (LBNL14June) MCC	No failures observed at 75% of reverse voltage when irradiated with 1233 MeV Xe (LET = 58.8). Catastrophic failure was observed at 100% of reverse voltage.	100 V	3
STPS20200C	STMicroelectronics	14-037; 640DN wafer	Diode	Si	H: (LBNL14June) MCC	No failures observed at 75% of reverse voltage when irradiated with 1233 MeV Xe (LET = 58.8). Catastrophic failure was observed at 100% of reverse voltage.	200 V	4
MBR20100CT	Fairchild Semiconductor	14-031; A1250 wafer	Diode	Si	H: (LBNL14June) MCC	Degradation observed during beam run while biased at 75% of reverse voltage, but all parameters remained within specification when irradiated with 1233 MeV Xe (LET = 58.8). Catastrophic failures observed when biased at 100% of reverse voltage	100 V	3
MBR20200CT	Fairchild Semiconductor	14-033; A1034 wafer	Diode	Si	H: (LBNL14June) MCC	Degradation observed during beam run while biased at 75% of reverse voltage, but all parameters remained within specification when irradiated with 1233 MeV Xe (LET = 58.8). Catastrophic failures observed when biased at 100% of reverse voltage.	200 V	3
NXPS20H100CX	NXP Semiconductor	14-022; 1310	Diode	Si	H: (LBNL14June) MCC	Degradation observed during beam run while biased at 75% of reverse voltage, but all parameters remained within specification when irradiated with 1233 MeV Xe (LET = 58.8). Catastrophic failures observed when biased at 100% of reverse voltage.	100 V	3
MBR2060CT	ON Semiconductor	14-042; NF031 wafer	Diode	Si	H: (LBNL14June) MCC	Degradation observed during beam run while biased at 75% of reverse voltage, but all parameters remained within specification when irradiated with 1233 MeV Xe (LET = 58.8). Catastrophic failures observed when biased at 100% of reverse voltage.	60 V	3
STPS30H100C	STMicroelectronics	14-036; 7SAGG wafer	Diode	Si	H: (LBNL14June) MCC	Degradation observed during beam run while biased at 75% of reverse voltage, but all parameters remained within specification when irradiated with 1233 MeV Xe (LET = 58.8). Catastrophic failures observed when biased at 100% of reverse voltage.	100 V	3
STPS60SM200C	STMicroelectronics	14-038; G406X wafer	Diode	Si	H: (LBNL14June) MCC	Degradation observed during beam run while biased at 75% of reverse voltage, but all parameters remained within specification when irradiated with 1233 MeV Xe (LET = 58.8). Catastrophic failures observed when biased at 100% of reverse voltage.	200 V	3
MBR20100CT	Vishay	14-026; 1411G wafer	Diode	Si	H: (LBNL14June) MCC	Degradation observed during beam run while biased at 75% of reverse voltage, but all parameters remained within specification when irradiated with 1233 MeV Xe (LET = 58.8). Catastrophic failures observed when biased at 100% of reverse voltage.	100 V	3
MBR60100	Vishay	14-027; 1335S wafer	Diode	Si	H: (LBNL14June) MCC	Degradation observed during beam run while biased at 75% of reverse voltage, but all parameters remained within specification when irradiated with 1233 MeV Xe (LET = 58.8). Catastrophic failures observed when biased at 100% of reverse voltage.	100 V	3
STPS40M60C	STMicroelectronics	14-035; 64OBY wafer	Diode	Si	H: (LBNL14June) MCC	No failures observed at 50% of reverse voltage when irradiated with 1233 MeV Xe (LET = 58.8). Degradation observed during beam run while biased at 75% of reverse voltage. Post-rad electrical parameter measurements were out of specification. Catastrophic failure was observed at 100% of reverse voltage.	60 V	4
MBR20H200CT	Vishay	14-028; 1330S wafer	Diode	Si	H: (LBNL14June) MCC	No failures observed at 50% of reverse voltage when irradiated with 1233 MeV Xe (LET = 58.8). Degradation observed during beam run while biased at 75% of reverse voltage. Post-rad electrical parameter measurements were out of specification. Catastrophic failure was observed at 100% of reverse voltage.	200 V	3
MBRC20200CT	ON Semiconductor	12-034; CH803691S1 WFR#3	Diode	Si	H: (LBNL14June; Sept) MCC	Catastrophic failure was observed at 100% of reverse voltage when irradiated with 1233 MeV Xe (LET = 58.8). Elevated temperature does not appear to change part susceptibility.	200 V	3
STPS4045C	STMicroelectronics	14-034; 6K1F1 wafer	Diode	Si	H: (LBNL14June) MCC	No failures observed at 50% of reverse voltage when irradiated with 1233 MeV Xe (LET = 58.8). Catastrophic failure was observed at 75% and 100% of reverse voltage.	45 V	4
MBR3045PT	Fairchild Semiconductor	14-029; AC33 wafer	Diode	Si	H: (LBNL14June) MCC	Catastrophic failure was observed at 100% of reverse voltage when irradiated with 1233 MeV Xe (LET = 58.8). Additional testing is required.	45 V	4
FPGAs:								
A3PE3000L-PQ208 ProASIC	Microsemi	12-052; 1108	ProASIC FPGA	CMOS	H and P: (LBNL14May) MB	Ongoing research investigating different mitigation strategies.	1.5; 2.5; and 3.3 V	2
XC7K325T Kintex7	Xilinx	14-001; 1349	FPGA	CMOS	H: (TAMU14Apr/Oct/Dec) MB	SEU LET_{th} < 0.07 (configurable memory)	Varies w/data sheet	5
XQV5FX70T	Xilinx	14-015; 1774118	Virtex 5 FPGA	CMOS	H: (TAMU14Apr/Oct) MB	Contact PI for test results.	4.5 V	2
Test Chips:								
32 nm SOI (Deneb)	IBM	13-067; 14-013	SET Pulse Width Measurement	32 nm SOI CMOS	H: (LBNL14May) JP w/Rodbell	Contact Kenneth P. Rodbell	0.9, nominal	1
Miscellaneous Devices:								
RDHA710	International Rectifier	14-008; 1340	Solid State Relay	Hybrid	H: (TAMU14Apr) MCC	SET LET_{th} < 87.1 MeV-cm^2/mg. No SEEs observed.	28 V, 35 V	2
RDHA701	International Rectifier	14-009; 1340	Solid State Relay	Hybrid	H: (TAMU14Apr) MCC	SET LET_{th} < 87.1 MeV-cm^2/mg. No SEEs observed.	28 V, 35 V	2

Test Results and Discussion

As in our past workshop compendia of NASA Goddard Space Flight Center (GSFC) test results, each DUT has a detailed test report available online at http://radhome.gsfc.nasa.gov [10] describing the test method, SEE conditions/parameters, test results, and graphs of data.

This section contains summaries of testing performed on a selection of featured parts.

Samsung 256 GB 850 Pro Solid State Drive

We evaluated the heavy ion single-event effect (SEE) susceptibility of the Samsung 850 PRO solid state drive (SSD). Their datasheets can be found on Samsung's websites [13], [14]. The 850 PRO drives consist of multiple-level cell (MLC) VNAND. The 256 GB SSD comprises 4 VNAND chips. Each chip consists of multiple stacked VNAND die. The other active components on the SSD, including the DDR3 memory and controller, were shielded during the beam exposure.

Fig. 1 shows a schematic of the test setup. The desktop PC for accessing the SSD is positioned in the irradiation chamber in close proximity to the device-under-test (DUT). The power supply is also positioned in the irradiation chamber. We remotely control the power supply via GPIB or USB interface. We utilized an open source software called "Caine" as the diagnostic tool to perform read and write operations to the SSD [13]. The program interface also allows us to examine the Self-Monitoring, Analysis and Reporting Technology (SMART) attributes, which includes a list of reliability parameters for the SSD.

Fig. 2 shows a photograph of the test setup. The SSD operated in the static or dynamic test mode. In the static mode, we programmed the SSD with a pattern (00, FF, checkerboard), irradiated the device, read and recorded the bad addresses. In dynamic mode, we actively cycled in read or write/read mode and recorded errors during the exposure. In the event of a functional interrupt, we allowed the SSD to self-clear the error. If functionality did not recover, we cycled power to the SSD.

Single-event functional interrupt (SEFI) dominated the SEE response. The SEFI LET threshold is less than 1.8 MeV·cm^2/mg. The SSD recovered functionality by power reset in most cases, and the errors self-cleared on the second read in other cases. In addition, the SMART attributes revealed errors due to ion-induced cell corruption which were corrected by ECC.

Fig. 3 shows the SEFI cross section as a function of effective LET. The cross-section data have significant Poisson error, due to the low error count. We irradiated four parts with 25 MeV/amu Kr, Ar, and Ne, at various angles. The heavy ions likely penetrated multiple dies for some ion species (particularly Ne). Therefore, SEFI due to signal contention is possible. However, with that consideration, we carried out comparative runs with degraded beams, which reduced the ion penetration range to within one die, but still observed SEFIs with similar characteristics. Table VI categorizes the functional interrupt errors according to the device response, recovery method, and test mode. We note that the errors during read/write tests occurred during the read cycle only. We did not detect write errors during the test.

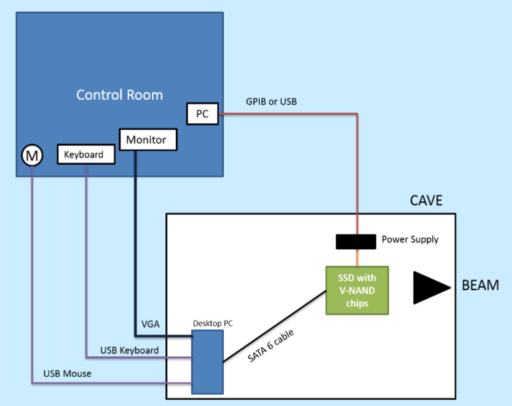


Fig. 1. Schematic diagram of the test setup.

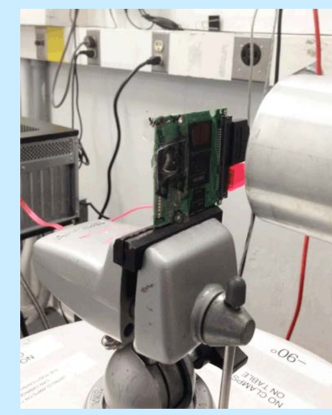


Fig. 2. Shows a photograph of the test setup.

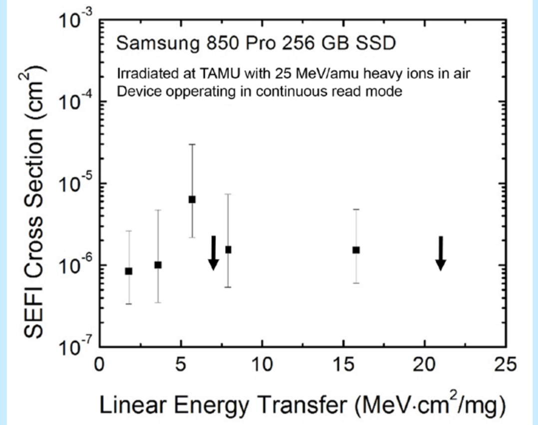


Fig. 3. SEFI cross section vs. LET for the 256 GB Samsung SSD irradiated with 25 MeV/amu heavy ions in air. Device was continuously read during irradiation. Arrows indicate maximum fluence levels without any observed error.

Table VI:
SEFIs categorized according to the test mode, event characteristics, and recovery method.

Test Mode	Description	Recovery Method
Static on, Static off	SSD not responsive	Power cycle
Static on, Dynamic read	Read access errors	Power cycle, Self-cleared in one case
Dynamic read	Corrupt data errors with entire memory showing errors	Rewritten (Did not power cycle)
Dynamic read	Corrupt data errors with 8 continuous sectors showing errors	Self-cleared on next read

Static on/off tests are representative of typical application conditions for storage flash devices. All of the SEEs that occurred during static mode testing caused the SSD to become nonresponsive. A power cycle was required to recover functionality following such an event. Critically, the SEFI occurred even when the SSD was unpowered during irradiation. The stored data were unaffected. We were able to successfully read the programmed data after a SEFI.

The program categorized the errors as either access errors or data corruption errors. The access errors meant that the SSD could not carry out the read successfully. The corrupt errors could represent radiation-induced corrupt cells. However, in some cases, the corrupt error could be cleared on a subsequent read. Thus they are likely caused by SEUs in the data buffers. However, cell corruption was evident in other cases. The SMART attribute, "reallocated sector count," indicated the number of sectors which were removed and replaced due to cell corruption. The error count increased due to SEE even though the errors were not visible during read, since ECC detected and corrected the errant data by replacing the bad sectors.

Both read access errors and data corruption errors affected 8 continuous sectors (4 KB) at a time. The errors repeated every 128 sectors in most cases. The trend may reflect the data organization of the SSD, which we are not yet familiar with at the time of this writing. The 256 GB SSD consists of two 8 die chips and two 4 die chips. We irradiated the 8 die chip during the test. Assuming that the controller reads 4 KB from one die at a time, once the SSD encounters a SEFI, it skips the other dies in that chip and attempts to read from the next chip. Therefore, the total number of sectors from the other unirradiated chips should be 8×(4+4+8) = 128 sectors. Consequently, we repeatedly observed the patterns of 8 continuous bad sectors followed by 128 error-free sectors. [15], [16]

Texas Instruments LM6172 Operational Amplifier

The LM6172 is a matched pair of high speed, low power, low distortion voltage feedback amplifiers. It offers 100 MHz unity-gain bandwidth, 3000 V/μs slew rate and 50 mA of output current per channel, while consuming 2.3 mA of supply current per channel. The device can operate at ±5 V or ±15 V power supply. The LM6172 is built with Texas Instruments' advanced VIP III (Vertically Integrated PNP).

Three parts were mechanically delidded. The parts were then soldered to small printed circuit boards (PCBs) that were designed specifically for this testing. The test circuits for one side of each device was configured as an inverter, while the other side was configured as a voltage follower. The inverter configuration was application specific for the instrument. Schematics of these circuit configurations are shown in the full test report [17].

While these parts showed no destructive SEEs, the LM6172 is highly susceptible to SETs. Fig. 4 shows the single-event transient cross section for transients with amplitude greater than 20 mV plotted on a log-linear scale. The blue data points show the application-specific inverter configuration, while the red points show the data from the voltage follower. The errors bars were calculated using Poisson statistics at the 90% confidence level. No transients were observed when irradiated with He, and these data points are indicated on the cross-section figures by a straight line with a downward-pointing arrow. Figs. 5 and 6 show the amplitudes and pulsewidths generated when irradiated with each ion in the inverter and voltage follower configurations, respectively. It should be noted that He is not shown on these figures because no transients were observed. Each ion is shown in a different color, while the different shapes indicate the angle of incidence used. The inverter configuration appears to very slightly lengthen the pulsewidth while reducing the transient amplitude. This is most likely due to the capacitance and resistance in the feedback loop which create an RC time constant that is not present in the voltage follower.

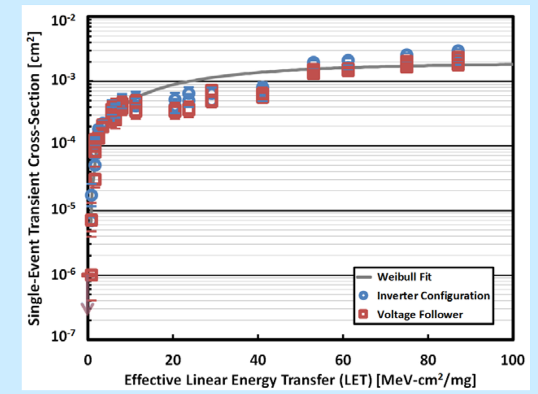


Fig. 4. Single-event transient cross-section as a function of effective LET for two LM6172 circuit configurations.

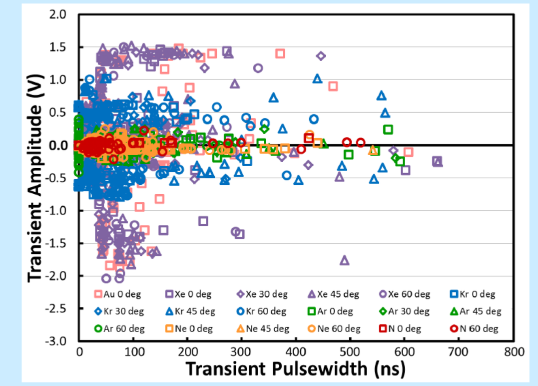


Fig. 5. Amplitude and pulsewidth scatterplot for transients generated on the LM6172 in the voltage follower configuration.

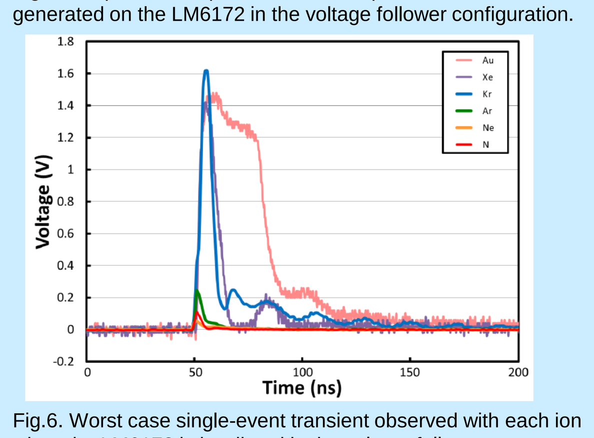


Fig.6. Worst case single-event transient observed with each ion when the LM6172 is irradiated in the voltage follower configuration and biased with 0 V on the input.

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Summary

We have presented current data from SEE testing on a variety of mainly commercial devices. It is the authors' recommendation that these data be used with caution. We also highly recommend that lot testing be performed on any suspect or commercial device.

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