Stable Electrical Operation of 6H–SiC JFETs and ICs for Thousands of Hours at 500 °C

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***Abstract*—The fabrication and testing of the first semiconductor transistors and small-scale integrated circuits (ICs) to achieve up to 3000 h of stable electrical operation at 500 °C in air ambient is reported. These devices are based on an epitaxial 6H–SiC junction field-effect transistor process that successfully integrated high-temperature ohmic contacts, dielectric passivation, and ceramic packaging. Important device and circuit parameters exhibited less than 10% of change over the course of the 500 °C operational testing. These results establish a new technology foundation for realizing durable 500 °C ICs for combustion-engine sensing and control, deep-well drilling, and other harsh-environment applications.**

***Index Terms*—High-temperature techniques, integrated circuit (IC) reliability, JFET ICs, junction field-effect transistors (JFETs), silicon compounds.**

I. Introduction

THE EXTENSION of the operating temperature envelope of useful transistor integrated circuits (ICs) well above the effective 300 °C limit of silicon-on-insulator technology is expected to enable important improvements to aerospace, automotive, energy production, and other industrial systems [1]. The emergence of wide bandgap semiconductors has enabled brief (on the order of a few hours or less) transistor and IC demonstrations at ambient temperatures of 500 °C or higher [2]–[6]. However, most envisioned applications require stable IC operation over much longer time periods at high temperature, which are on the order of thousands of hours or more. Although SiC is well known to be chemically near inert and diffusion resistant compared with silicon and III–V semiconductors, thermally activated degradation mechanisms at interfaces (such as metal–SiC and/or SiC–insulator interfaces) or materials outside the semiconductor (such as metals, insulators, and/or packaging) have limited extreme-temperature (i.e., $\geq$ 500 °C) stability/durability [1], [4]–[9]. This letter reports the first semiconductor transistors and small ICs to achieve as many as 3000 h of stable electrical operation at 500 °C. This establishes a new technology foundation for realizing usefully durable extreme-temperature ICs to benefit important harsh-environment applications.

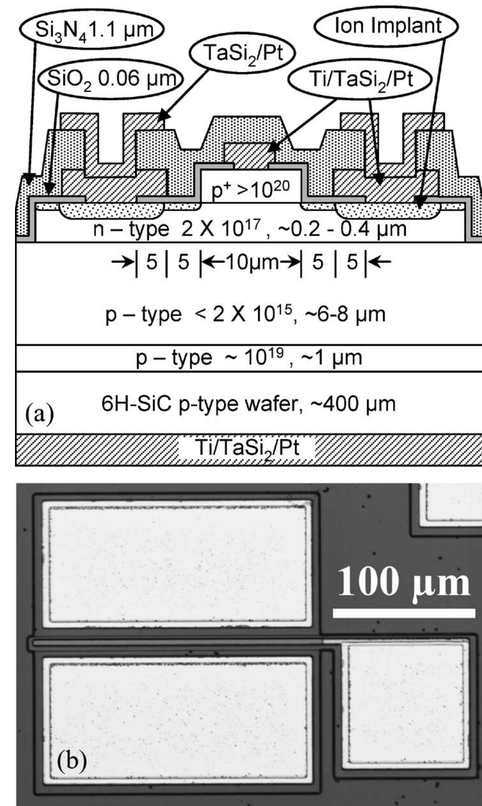

Fig. 1. (a) Simplified cross-sectional schematic of 6H–SiC JFET. The following lateral design dimensions are shown: gate length (10 μm), gate edge to n^+ contact edge spacing (5 μm), and n^+ contact edge to insulator via edge spacing (5 μm). (b) Optical micrograph showing the linear mesa layout of the 200 μm/10 μm 6H–SiC JFET. Wire-bond pads reside directly on the device mesa.

II. Experimental

A quarter wafer of small-signal 6H–SiC junction field-effect transistors (JFETs) and simple ICs (configured using a single metal-interconnect layer) was fabricated starting from commercially purchased [10] epilayered substrates. Fig. 1(a) shows the simplified cross-sectional schematic of the depletion-mode epitaxial JFET device structure, whereas the optical micrograph of Fig. 1(b) shows the layout of a test JFET with a gate width of 200 μm and a gate length of 10 μm. Fabrication process

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TABLE I
ELECTRICAL PARAMETERS OF DEVICES AND CIRCUITS RECORDED AT SELECTED TIMES DURING THE 500 °C OPERATIONAL TESTING OF PACKAGED 6H–SiC CHIPS. NOTE THAT ALL LARGE (> 2-FOLD) PARAMETER CHANGES CORRESPOND TO IMPROVED DEVICE LEAKAGE PERFORMANCE. "ITT" ENTRIES STAND FOR "INSUFFICIENT TESTING TIME" ACCUMULATED AT 500 °C TO DATE

Device	Parameter	Note	1 h	~100 h	~2000 h	3007 h	Change
Cap. #1	J_R (μA/cm^2)	1	604	218	90.9	104	-5.8X
Cap. #2	J_R (μA/cm^2)	1	301	116	ITT	ITT	-2.5X
JFET #1 200μm/10μm	V_T (V)	2	-11.8	-11.8	-11.8	-11.8	< 1%
	I_{DSS} (mA)	3	1.36	1.34	1.32	1.31	-3.7%
	g_{m0} (μS)	4	214	209	207	205	-4.2%
	R_{DS} (kΩ)	5	4.64	4.74	4.79	4.83	+4.1%
	I_{OFF} (μA)	6	37.1	1.04	0.09	0.19	-195X
JFET #2 100μm/10μm	I_{DSS} (mA)	3	0.690	0.676	0.653	0.647	-6.2%
	g_{m0} (μS)	4	107	105	101	101	-5.6%
	R_{DS} (kΩ)	5	10.3	10.8	11.2	11.3	+9.7%
Differential Amplifier IC	A_V @ 100 Hz	7	2.91	2.99	2.95	2.91	< 1%
	A_V @ 1 kHz	7	2.86	2.90	2.90	2.88	< 1%
	A_V @ 10 kHz	7	2.18	2.06	2.21	2.19	< 1%
	f_T (kHz)	8	32	30	33	33	3%
NOR Gate IC	V_{OH}	9	-1.47	-1.23	-1.67	ITT	-13.6%
	V_{OL}	10	-8.12	-8.03	-8.14	ITT	< 1%

Note 1: J_R = Capacitor leakage current density under continuous applied stress of 50 V.
Note 2: V_T = Threshold voltage from extrapolated x-intercept of $\sqrt{I_D}$ vs. V_G plot at V_D = 50 V.
Note 3: I_{DSS} = Measured drain current I_D with V_G = 0 V, V_D = 20 V.
Note 4: g_{m0} = Transconductance measured at V_D = 20 V from V_G = 0 V and V_G = -2 V steps.
Note 5: R_{DS} = Drain-to-source resistance for V_G = 0 V.
Note 6: I_{OFF} = Off-state drain leakage current measured at V_D = 50 V, V_G = -15 V.
Note 7: A_V = Differential amplifier voltage gain.
Note 8: f_T = Unity voltage gain frequency.
Note 9: V_{OH} = NOR output high voltage with both inputs low at -7.5 V.
Note 10: V_{OL} = NOR output low voltage with one input high at -2.5 V, other input low at -7.5 V.

details are described elsewhere [7]–[9], [11]–[13]. The highly durable metallization scheme of Ti/$TaSi_2$/Pt that was previously reported [12] contacted the n-type source–drain nitrogen implants and heavily p-type (Al-doped) gate epilayer. The Si_3N_4 layer was reactive sputter deposited at 200 W pulsed dc using a high-purity silicon target at 7 mtorr chamber pressure in 25 sccm N_2 (injected near the middle of the chamber) and 25 sccm Ar (injected at sputter gun) flows [13]. Following the patterned nitride via dry etching, the wafer was annealed in a N_2 tube furnace for 30 min at 600 °C. On-chip resistors were formed from the JFET n-channel layer and implants/contacts with the overlying p^+ gate layer removed. Interconnects and wire-bond pads were simultaneously formed by patterning $TaSi_2$/Pt on top of the reactive-sputtered Si_3N_4 dielectric. A differential-amplifier (diff-amp) IC consisting of three resistors and two source-coupled 20 μm gate-width/10 μm gate-length JFETs operates with a 40 V supply [11]. Logic ICs operate with negative logic voltages ($V_{\mathrm{High}} = -2.5$ V, and $V_{\mathrm{Low}} = -7.5$ V), with the NOR gate reported here consisting of three 40 μm/10 μm JFETs and three resistors powered by +20 V and −24 V supplies.

Almost all JFETs and circuits probe tested on the quarter wafer operated well at room temperature. However, probe-tip degradation effectively prohibits long-term 500 °C probe testing. Several SiC chips from the saw-diced quarter wafer were custom packaged without any lids (i.e., exposed to air) and mounted onto two custom high-temperature circuit boards [8]. The two boards were placed in two laboratory ovens with unshielded Au wires running outside the ovens to nearby terminal strips connected to computer-controlled test instruments. The devices and circuits continuously operated under electrical bias throughout the 500 °C test duration, with measurement data periodically (hourly at first then expanding to every 20 h later) stored onto a computer. The atmosphere inside the oven was ordinary room air (∼21% O_2). Back-side substrate contacts were grounded except for the −24 V bias applied to the NOR IC chip substrate.

III. RESULTS

As of this writing, two JFETs and one diff-amp IC have achieved more than 3000 h of continuous 500 °C electrical operation in air. A digital NOR-gate IC that started testing later has operated for over 2000 h at 500 °C. Table I quantitatively summarizes the measurements of important electrical parameters recorded during the 1st, ∼100th (100th for one oven and 103rd for another oven), ∼2000th (2000th or 2015th), and ∼3000th (3007th) hours of 500 °C testing.

Fig. 2 shows the comparison of the drain current I_D versus voltage (I–V) characteristics of a 200 μm/10 μm JFET (#1) measured by source-measure instruments during the 1st, 100th, and 3007th hours of the 500 °C operation under the dc stress of drain bias $V_D = 50$ V and gate bias $V_G = -6$ V. The ON-state I–V characteristics in Fig. 2(a) change by less than 10%,

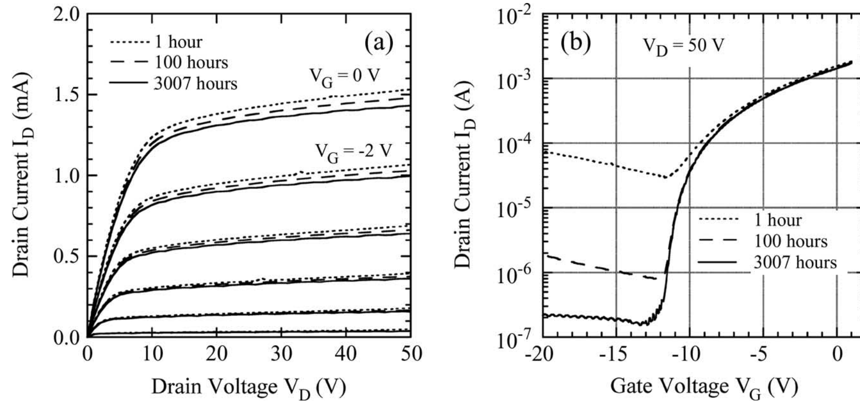

Fig. 2. Drain I–V characteristics of packaged 200 μm/10 μm 6H–SiC JFET measured during the 1st, 100th, and 3007th hour of continuous electrical operation at 500 °C. (a) Linear scale I_D versus V_D for -2 V gate steps. (b) Log scale I_D versus V_G for $V_D = 50$ V. The most circuit-critical I–V parameters degrade less than 10% throughout the test, whereas the OFF-state leakage current I_{OFF} improves (decreases) over two orders of magnitude.

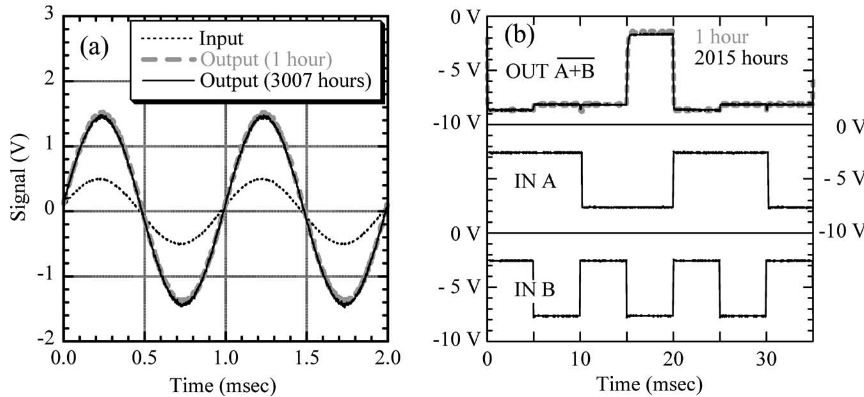

Fig. 3. Operational waveforms recorded during the 500 °C IC durability testing. (a) Diff-amp 1 kHz sine-wave test demonstrating a stable voltage gain near three during the 1st and 3007th hour of the 500 °C operation. (b) NOR-gate IC test waveforms showing stable desired output signals recorded during the 1st and 2015th hour of the 500 °C operation. For this logic family, V_{High} is -2.5 V, and V_{Low} is -7.5 V.

with over half of the small change occurring during the first 100 h of the 500 °C operation. Similar results were obtained for a 100 μm/10 μm JFET (#2 in Table I) measured by a digitizing 60 Hz curve tracer that continuously operated with 50 V drain-bias sweeps and -2 V gate steps from $V_G = 0$ V to $V_G = -16$ V. As shown in Fig. 2(b), the I_D versus V_G turnoff characteristics of JFET #1 considerably improved ($>$ 30-fold reduction in the OFF-state current I_{OFF}) during the first 100 h of the 500 °C operation. The measurements of two packaged $Pt/TaSi_2/Si_3N_4$/p-SiC test capacitors (Cap. #1 and Cap. #2 in Table I) biased at 50 V also exhibited substantial leakage-current drop over the same time period. We surmise that the JFET I_{OFF} was initially dominated by leakage across the Si_3N_4 layer, which greatly reduced (for reasons not yet studied) during the first 100 h of the 500 °C anneal time. Further studies of the JFET and nitride leakage behavior, which are well beyond the scope of this letter, are warranted.

Fig. 3 shows the 500 °C operational waveforms recorded from the ICs near the start and end of the presently reported testing. Considering that the primary goal of the experiment was the initial demonstration of the 500 °C IC durability, no effort was made to optimize the gain and/or frequency performance of the circuits. The outputs of both circuits drove 10 MΩ oscilloscope probes (11.1 pF and ac coupled for the diff-amp and 7.5 pF and dc coupled for the NOR). Fig. 3(a) shows the output waveforms of the diff-amp during the 1st and 3007th hours of the 500 °C operation, which are in response to a 1 kHz 1 V peak-to-peak amplitude sine-wave input. After 3000 h of 500 °C operation, the gain of the diff-amp changed less than 3% from its initial value. Fig. 3(b) shows the NOR-gate output recorded during the 1st and 2015th hours of the 500 °C testing, which are in response to the -2.5 V to -7.5 V logic-test input waveforms. The NOR-gate IC was subjected to a 144 h unbiased 500 °C soak (i.e., a "burn-in" suggested by the aforementioned JFET and capacitor results) prior to the initiation of the first hour of the 500 °C electrical testing. The desired stable operation with noise margins greater than 0.5 V were observed throughout the test.

IV. Summary Discussion

The increased 500 °C IC durability and stability demonstrated in this letter is now sufficient for beneficial sensor signal-conditioning circuits to survive most jet-engine ground-test programs. The durability testing of additional ICs at 500 °C is also under way and more will be initiated as additional testing equipment and high-temperature packaged ICs become available. Future work will also report on the measurement and modeling at other temperatures, including the characterization and modeling of operating-frequency limitations.

Although only a small number of devices have been packaged and tested for thousands of hours at high temperature, this demonstration establishes the feasibility of producing SiC integrated circuitry which is capable of prolonged 500 °C operation. This result was achieved through the integration of fundamental materials and/or processing advancements, including the development of high-temperature n-type ohmic contacts [12] and high-temperature packaging technology [8]. We speculate that the choice of epitaxial JFET technology and its designed operation at relatively low electric fields and low current densities are also important to the demonstrated 500 °C durability. For many envisioned applications, far greater circuit complexities than the few-transistor ICs demonstrated in this letter will be needed. The shrinkage of device dimensions and operating biases and the implementation of multilayer interconnects are obvious important further steps toward realizing durable 500 °C SiC integrated circuitry with greater complexity, higher frequency performance, and increased functionality.

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