Silicon Carbide Technology

Philip G. Neudeck
NASA Glenn Research Center

5.1 Introduction

Silicon carbide (SiC)-based semiconductor electronic devices and circuits are presently being developed for use in high-temperature, high-power, and high-radiation conditions under which conventional semiconductors cannot adequately perform. Silicon carbide's ability to function under such extreme conditions is expected to enable significant improvements to a far-ranging variety of applications and systems. These range from greatly improved high-voltage switching for energy savings in public electric power distribution and electric motor drives to more powerful microwave electronics for radar and communications to sensors and controls for cleaner-burning more fuel-efficient jet aircraft and automobile engines [1–7]. In the particular area of power devices, theoretical appraisals have indicated that SiC power MOSFET's and diode rectifiers would operate over higher voltage and temperature ranges, have superior switching characteristics, and yet have die sizes nearly 20 times smaller than correspondingly rated silicon-based devices [8]. However, these tremendous theoretical advantages have yet to be widely realized in commercially available SiC devices, primarily owing to the fact that SiC's relatively immature crystal growth and device fabrication technologies are not yet sufficiently developed to the degree required for reliable incorporation into most electronic systems.

This chapter briefly surveys the SiC semiconductor electronics technology. In particular, the differences (both good and bad) between SiC electronics technology and the well-known silicon VLSI technology are highlighted. Projected performance benefits of SiC electronics are highlighted for several large-scale applications. Key crystal growth and device-fabrication issues that presently limit the performance and capability of high-temperature and high-power SiC electronics are identified.

5.2 Fundamental SiC Material Properties

5.2.1 SiC Crystallography: Important Polytypes and Definitions

Silicon carbide occurs in many different crystal structures, called polytypes. A more comprehensive introduction to SiC crystallography and polytypism can be found in Reference 9. Despite the fact that all SiC polytypes chemically consist of 50% carbon atoms covalently bonded with 50% silicon atoms, each SiC polytype has its own distinct set of electrical semiconductor properties. While there are over 100 known polytypes of SiC, only a few are commonly grown in a reproducible form acceptable for use as an electronic semiconductor. The most common polytypes of SiC presently being developed for electronics are 3C-SiC, 4H-SiC, and 6H-SiC. The atomic crystal structure of the two most common polytypes is shown in the schematic cross section in Figure 5.1. As discussed much more thoroughly in References 9 and 10, the different polytypes of SiC are actually composed of different stacking sequences of Si–C bilayers (also called Si–C double layers), where each single Si–C bilayer is denoted by the dotted boxes in Figure 5.1. Each atom within a bilayer has three covalent chemical bonds with other atoms in the same (its own) bilayer, and only one bond to an atom in an adjacent bilayer. Figure 5.1a shows the bilayer of the stacking sequence of 4H-SiC polytype, which requires four Si–C bilayers to define the unit cell repeat distance along the *c*-axis stacking direction (denoted by $\langle 0\,0\,0\,1 \rangle$ Miller indices). Similarly, the 6H-SiC polytype illustrated in Figure 5.1b repeats its stacking sequence every six bilayers throughout the crystal along the stacking direction. The $\langle 1\bar{1}00 \rangle$ direction depicted in Figure 5.1 is often referred to as one of (along with $\langle 11\bar{2}0 \rangle$) the *a*-axis directions. SiC is a polar semiconductor across the *c*-axis, in that one surface normal to the *c*-axis is terminated with silicon atoms while the opposite normal *c*-axis surface is terminated with carbon atoms. As shown in Figure 5.1a, these surfaces are typically referred to as "silicon face" and "carbon face" surfaces, respectively. Atoms along the left-or right-side edge of Figure 5.1a would reside on ($\langle 1\bar{1}00 \rangle$) "a-face" crystal surface plane normal to the $\langle 1\bar{1}00 \rangle$ direction. 3C-SiC, also referred to as β-SiC, is the only form of SiC with a cubic crystal lattice structure. The noncubic polytypes of SiC are sometimes ambiguously referred to as α-SiC. 4H-SiC and 6H-SiC are only two of the many

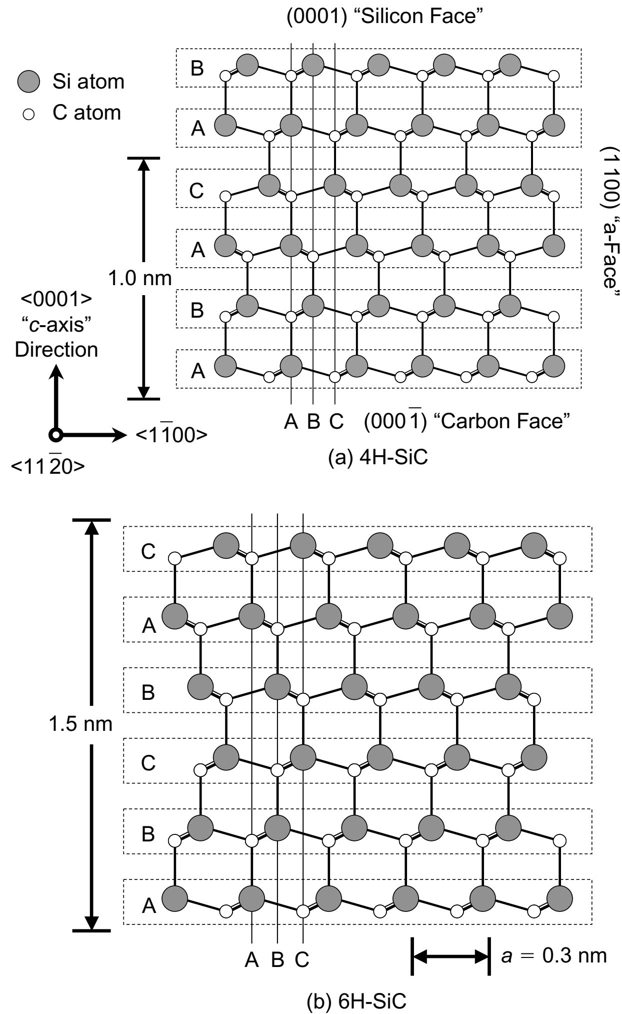

FIGURE 5.1 Schematic cross-sectional depictions of (a) 4H-SiC and (b) 6H-SiC atomic crystal structure, showing important crystallographic directions and surfaces (see text).

possible SiC polytypes with hexagonal crystal structure. Similarly, 15R-SiC is the most common of the many possible SiC polytypes with a rhombohedral crystal structure.

5.2.2 SiC Semiconductor Electrical Properties

Owing to the differing arrangement of Si and C atoms within the SiC crystal lattice, each SiC polytype exhibits unique fundamental electrical and optical properties. Some of the more important semiconductor electrical properties of the 3C, 4H, and 6H SiC polytypes are given in Table 5.1. Much more detailed electrical properties can be found in References 11–13 and references therein. Even within a given polytype, some important electrical properties are nonisotropic, in that they are strong functions of crystallographic direction of current flow and applied electric field (for example, electron mobility for 6H-SiC). Dopant impurities in SiC can incorporate into energetically inequivalent sites. While all dopant ionization energies associated with various dopant incorporation sites should normally be considered for utmost accuracy, Table 5.1 lists only the shallowest reported ionization energies of each impurity.

TABLE 5.1 Comparison of Selected Important Semiconductor Electronic Properties of Major SiC Polytypes with Silicon, GaAs, and 2H-GaN at 300 K

Property	Silicon	GaAs	4H-SiC	6H-SiC	3C-SiC	2H-GaN
Bandgap (eV)	1.1	1.42	3.2	3.0	2.3	3.4
Relative dielectric constant	11.9	13.1	9.7	9.7	9.7	9.5
Breakdown field $N_D = 10^{17}$ cm^{-3} (MVcm^{-1})	0.6	0.6	//c-axis: 3.0 $\perp c$-axis: 2.5	//c-axis: 3.2 $\perp c$-axis: > 1	1.8	2–3
Thermal Conductivity (W/cm-K)	1.5	0.5	3–5	3–5	3–5	1.3
Intrinsic carrier concentration (cm^{-3})	10^{10}	1.8×10^6	$\sim 10^{-7}$	$\sim 10^{-5}$	~10	$\sim 10^{-10}$
Electron mobility at $N_D = 10^{16}$ cm^{-3} (cm^{2}V^{-1}s^{-1})	1200	6500	//c-axis: 800 $\perp c$-axis: 800	//c-axis: 60 $\perp c$-axis: 400	750	900
Hole mobility at $N_A = 10^{16}$ cm^{-3} (cm^{2}V^{-1}s^{-1})	420	320	115	90	40	200
Saturated electron velocity (10^7 cms^{-1})	1.0	1.2	2	2	2.5	2.5
Donor dopants and shallowest ionization energy (meV)	P: 45 As: 54	Si: 5.8	N: 45 P: 80	N: 85 P: 80	N: 50	Si: 20
Acceptor dopants and shallowest ionization energy (meV)	B: 45	Be, Mg, C: 28	Al: 200 B: 300	Al: 200 B: 300	Al: 270	Mg: 140
2005 Commercial wafer diameter (cm)	30	15	7.6	7.6	15	None

Source: Data compiled from references [6,11,13,15,186,196–199] and references therein.

For comparison, Table 5.1 also includes comparable properties of silicon, GaAs, and GaN. Because silicon is the semiconductor employed in most commercial solid-state electronics, it is the standard against which other semiconductor materials must be evaluated. To varying degrees the major SiC polytypes exhibit advantages and disadvantages in basic material properties compared to silicon. The most beneficial inherent material superiorities of SiC over silicon listed in Table 5.1 are its exceptionally high breakdown electric field, wide bandgap energy, high thermal conductivity, and high carrier saturation velocity. The electrical device performance benefits that each of these properties enables are discussed in the next section, as are system-level benefits enabled by improved SiC devices.

5.3 Applications and Benefits of SiC Electronics

Two of the most beneficial advantages that SiC-based electronics offer are in the areas of high-temperature and high-power device operation. The specific SiC device physics that enables high-temperature and high-power capabilities will be examined first, followed by several examples of revolutionary system-level performance improvements these enhanced capabilities enable.

5.3.1 High-Temperature Device Operation

The wide bandgap energy and low intrinsic carrier concentration of SiC allow SiC to maintain semiconductor behavior at much higher temperatures than silicon, which in turn permits SiC semiconductor device functionality at much higher temperatures than silicon [7]. As discussed in basic semiconductor electronic device physics textbooks [14,15], semiconductor electronic devices function in the temperature range where intrinsic carriers are negligible so that conductivity is controlled by intentionally introduced dopant impurities. Furthermore, the intrinsic carrier concentration n_i is a fundamental prefactor to well-known equations governing undesired junction reverse-bias leakage currents. As temperature increases, intrinsic carriers increase exponentially so that undesired leakage

currents grow unacceptably large, and eventually at still higher temperatures, the semiconductor device operation is overcome by uncontrolled conductivity as intrinsic carriers exceed intentional device dopings. Depending upon specific device design, the intrinsic carrier concentration of silicon generally confines silicon device operation to junction temperatures <300°C. SiC's much smaller intrinsic carrier concentration theoretically permits device operation at junction temperatures exceeding 800°C. 600°C SiC device operation has been experimentally demonstrated on a variety of SiC devices (Section 5.6.3).

The ability to place uncooled high-temperature semiconductor electronics directly into hot environments would enable important benefits to automotive, aerospace, and deep-well drilling industries [7,16]. In the case of automotive and aerospace engines, improved electronic telemetry and control from high-temperature engine regions are necessary to more precisely control the combustion process to improve fuel efficiency while reducing polluting emissions. High-temperature capability eliminates performance, reliability, and weight penalties associated with liquid cooling, fans, thermal shielding, and longer wire runs needed to realize similar functionality in engines using conventional silicon semiconductor electronics.

5.3.2 High-Power Device Operation

The high breakdown field and high thermal conductivity of SiC coupled with high operational junction temperatures theoretically permit extremely high-power densities and efficiencies to be realized in SiC devices. The high breakdown field of SiC relative to silicon enables the blocking voltage region of a power device to be roughly 10× thinner and 10× heavier doped, permitting a roughly 100-fold beneficial decrease in the blocking region resistance at the same voltage rating [8]. Significant energy losses in many silicon high-power system circuits, particularly hard-switching motor drive and power conversion circuits, arise from semiconductor switching energy loss [1,3,17]. While the physics of semiconductor device switching loss are discussed in detail elsewhere [18], switching energy loss is often a function of the turn-off time of the semiconductor switching device, generally defined as the time lapse between application of a turn-off bias and the time when the device actually cuts off most of the current flow. In general, the faster a device turns off, the smaller its energy loss in a switched power conversion circuit. For device-topology reasons discussed in References 3,8, and 19–21, SiC's high breakdown field and wide energy bandgap enable much faster power switching than is possible in comparably volt–ampere-rated silicon power-switching devices. The fact that high-voltage operation is achieved with much thinner blocking regions using SiC enables much faster switching (for comparable voltage rating) in both unipolar and bipolar power device structures. Therefore, SiC-based power converters could operate at higher switching frequencies with much greater efficiency (i.e., less switching energy loss) [1,22]. Higher switching frequency in power converters is highly desirable because it permits use of smaller capacitors, inductors, and transformers, which in turn can greatly reduce overall power converter size, weight, and cost [3,22,23].

While SiC's smaller on-resistance and faster switching helps minimize energy loss and heat generation, SiC's higher thermal conductivity enables more efficient removal of waste heat energy from the active device. Because heat energy radiation efficiency increases greatly with increasing temperature difference between the device and the cooling ambient, SiC's ability to operate at high junction temperatures permits much more efficient cooling to take place, so that heat sinks and other device-cooling hardware (i.e., fan cooling, liquid cooling, air conditioning, heat radiators, etc.) typically needed to keep high-power devices from overheating can be made much smaller or even eliminated.

While the preceding discussion focused on high-power switching for power conversion, many of the same arguments can be applied to devices used to generate and amplify RF signals used in radar and communications applications. In particular, the high breakdown voltage and high thermal conductivity coupled with high carrier saturation velocity allow SiC microwave devices to handle much higher power densities than their silicon or GaAs RF counterparts, despite SiC's disadvantage in low-field carrier mobility [5,6,24–26].

5.3.3 System Benefits of High-Power High-Temperature SiC Devices

Uncooled operation of high-temperature and high-power SiC electronics would enable revolutionary improvements to aerospace systems. Replacement of hydraulic controls and auxiliary power units with distributed "smart" electromechanical controls capable of harsh ambient operation will enable substantial jet-aircraft weight savings, reduced maintenance, reduced pollution, higher fuel efficiency, and increased operational reliability [7]. SiC high-power solid-state switches will also enable large efficiency gains in electric power management and control [1,4,27–31]. Performance gains from SiC electronics could enable the public power grid to provide increased consumer electricity demand without building additional generation plants, and improve power quality and operational reliability through "smart" power management. More efficient electric motor drives enabled by SiC will also benefit industrial production systems as well as transportation systems such as diesel-electric railroad locomotives, electric mass-transit systems, nuclear-powered ships, and electric automobiles and buses.

From the above discussions it should be apparent that SiC high-power and high-temperature solid-state electronics promise tremendous advantages that could significantly impact transportation systems and power usage on a global scale. By improving the way in which electricity is distributed and used, improving electric vehicles so that they become more viable replacements for internal combustion-engine vehicles, and improving the fuel efficiency and reducing pollution of the remaining fuel-burning engines and generation plants, SiC electronics promises the potential to better the daily lives of all citizens of planet Earth.

5.4 SiC Semiconductor Crystal Growth

As of this writing, much of the outstanding theoretical promise of SiC electronics highlighted in the previous section has largely gone unrealized. A brief historical examination quickly shows that serious shortcomings in SiC semiconductor material manufacturability and quality have greatly hindered the development of SiC semiconductor electronics. From a simple-minded point of view, SiC electronics development has very much followed the general rule of thumb that a solid-state electronic device can only be as good as the semiconductor material from which it is made.

5.4.1 Historical Lack of SiC Wafers

Reproducible wafers of reasonable consistency, size, quality, and availability are a prerequisite for commercial mass production of semiconductor electronics. Many semiconductor materials can be melted and reproducibly recrystallized into large single crystals with the aid of a seed crystal, such as in the Czochralski method employed in the manufacture of almost all silicon wafers, enabling reasonably large wafers to be mass produced. However, because SiC sublimes instead of melting at reasonably attainable pressures, SiC cannot be grown by conventional melt-growth techniques. Prior to 1980, experimental SiC electronic devices were confined to small (typically ~1 cm^2), irregularly shaped SiC crystal platelets grown as a byproduct of the Acheson process for manufacturing industrial abrasives (e.g., sandpaper) [32] or by the Lely process [33]. In the Lely process, SiC sublimed from polycrystalline SiC powder at temperatures near 2500°C are randomly condensed on the walls of a cavity forming small, hexagonally shaped platelets. While these small, nonreproducible crystals permitted some basic SiC electronics research, they were clearly not suitable for semiconductor mass production. As such, silicon became the dominant semiconductor fueling the solid-state technology revolution, while interest in SiC-based microelectronics was limited.

5.4.2 Growth of 3C-SiC on Large-Area (Silicon) Substrates

Despite the absence of SiC substrates, the potential benefits of SiC hostile-environment electronics nevertheless drove modest research efforts aimed at obtaining SiC in a manufacturable wafer form. Toward this end, the heteroepitaxial growth of single-crystal SiC layers on top of large-area silicon

substrates was first carried out in 1983 [34], and subsequently followed by a great many others over the years using a variety of growth techniques. Primarily owing to large differences in lattice constant (~20% difference between SiC and Si) and thermal expansion coefficient (~8% difference), heteroepitaxy of SiC using silicon as a substrate always results in growth of 3C-SiC with a very high density of crystallographic structural defects such as stacking faults, microtwins, and inversion domain boundaries [35]. Other large-area wafer materials besides silicon (such as sapphire, silicon-on-insulator, and TiC) have been employed as substrates for heteroepitaxial growth of SiC epilayers, but the resulting films have been of comparably poor quality with high crystallographic defect densities. The most promising 3C-SiC-on-silicon approach to date that has achieved the lowest crystallographic defect density involves the use of undulant silicon substrates [36]. However, even with this highly novel approach, dislocation densities remain very high compared to silicon and bulk hexagonal SiC wafers.

While some limited semiconductor electronic devices and circuits have been implemented in 3C-SiC grown on silicon, the performance of these electronics (as of this writing) can be summarized as severely limited by the high density of crystallographic defects to the degree that almost none of the operational benefits discussed in Section 5.3 has been viably realized. Among other problems, the crystal defects "leak" parasitic current across reverse-biased device junctions where current flow is not desired. Because excessive crystal defects lead to electrical device shortcomings, there are as yet no commercial electronics manufactured in 3C-SiC grown on large-area substrates. Thus, 3C-SiC grown on silicon presently has more potential as a mechanical material in microelectromechanical systems (MEMS) applications (Section 5.6.5) instead of being used purely as a semiconductor in traditional solid-state transistor electronics.

5.4.3 Growth of Hexagonal Polytype SiC Wafers

In the late 1970s, Tairov and Tzvetkov established the basic principles of a modified seeded sublimation growth process for growth of 6H-SiC [37,38]. This process, also referred to as the modified Lely process, was a breakthrough for SiC in that it offered the first possibility of reproducibly growing acceptably large single crystals of SiC that could be cut and polished into mass-produced SiC wafers. The basic growth process is based on heating polycrystalline SiC source material to ~2400°C under conditions, where it sublimes into the vapor phase and subsequently condenses onto a cooler SiC seed crystal [10,37–39]. This produces a somewhat cylindrical boule of single-crystal SiC that grows taller roughly at the rate of a few millimeters per hour. To date, the preferred orientation of the growth in the sublimation process is such that vertical growth of a taller cylindrical boule proceeds along the <0 0 0 1> crystallographic *c*-axis direction (i.e., vertical direction in Fig. 5.1). Circular "*c*-axis" wafers with surfaces that lie normal (i.e., perpendicular to within 10°) to the c-axis can be sawed from the roughly cylindrical boule. After years of further development of the sublimation growth process, Cree, Inc., became the first company [40] to sell 2.5 cm diameter semiconductor wafers of *c*-axis-oriented 6H-SiC in 1989. Correspondingly, the vast majority of SiC semiconductor electronics development and commercialization has taken place since 1990 using *c*-axis-oriented SiC wafers of the 6H and 4H-SiC polytypes. N-type, p-type, and semi-insulating SiC wafers of various sizes (presently as large as 7.6 cm in diameter) are now commercially available from a variety of vendors [10,39,41]. It is worth noting that attainable substrate conductivities for p-type SiC wafers are more than 10× smaller than for n-type substrates, which is largely due to the difference between donor and acceptor dopant ionization energies in SiC (Table 5.1). More recently, SiC wafers grown with gas sources instead of sublimation of solid sources or a combination of gas and solid sources have also been commercialized [42,43]. Growth of SiC boules and wafers oriented along other crystallographic directions, such as $\langle 11\bar{2}0 \rangle$ and $\langle 1\bar{1}00 \rangle$ "*a*-face" orientations, have also been investigated over the last decade [44]. While these other SiC wafer orientations offer some interesting differences in device properties compared to conventional *c*-axis-oriented wafers (mentioned briefly in Section 5.5.5), all commercial SiC electronic parts produced (as of this writing) are manufactured using *c*-axis-oriented wafers.

Wafer size, cost, and quality are all very critical to the manufacturability and process yield of mass-produced semiconductor microelectronics. Compared to commonplace silicon wafer standards, present-day 4H- and 6H-SiC wafers are smaller, more expensive, and generally of inferior quality containing far

more crystal imperfections (see Section 5.4.5 below). This disparity is not surprising considering that silicon wafers have undergone nearly five decades of commercial process refinement.

5.4.4 SiC Epilayers

Most SiC electronic devices are not fabricated directly in sublimation-grown wafers, but are instead fabricated in much higher quality epitaxial SiC layers that are grown on top of the initial sublimation-grown wafer. Well-grown SiC epilayers have superior electrical properties and are more controllable and reproducible than bulk sublimation-grown SiC wafer material. Therefore, the controlled growth of high-quality epilayers is highly important in the realization of useful SiC electronics.

5.4.4.1 SiC Epitaxial Growth Processes

An interesting variety of SiC epitaxial growth methodologies, ranging from liquid-phase epitaxy, molecular beam epitaxy, and chemical vapor deposition(CVD) have been investigated [10,45]. The CVD growth technique is generally accepted as the most promising method for attaining epilayer reproducibility, quality, and throughputs required for mass production. In the simplest terms, variations of SiC CVD are carried out by heating SiC substrates in a chamber "reactor" with flowing silicon- and carbon-containing gases that decompose and deposit Si and C onto the wafer allowing an epilayer to grow in a well-ordered single-crystal fashion under well-controlled conditions. Conventional SiC CVD epitaxial growth processes are carried out at substrate growth temperatures between 1400°C and 1600°C at pressures from 0.1 to 1 atm resulting in growth rates of the order of a few micrometers per hour [10,41,46]. Higher temperature (up to 2000°C) SiC CVD growth processes, some using halide-based growth chemistries, are also being pioneered to obtain higher SiC epilayer growth rates of the order of hundreds of micrometers per hour that appear sufficient for growth of bulk SiC boules in addition to very thick epitaxial layers needed for high-voltage devices [42,47,48].

Despite the fact that SiC growth temperatures significantly exceed epitaxial growth temperatures used for most other semiconductors, a variety of SiC CVD epitaxial growth reactor configurations have been developed and commercialized [41,46,49]. For example, some reactors employ horizontal reactant gas flow across the SiC wafer, while others rely on vertical flow of reactant gases; some reactors have wafers surrounded by heated "hot-wall" or "warm-wall" configurations, while other "cold-wall" reactors heat only a susceptor residing directly beneath the SiC wafer. Most reactors used for commercial production of SiC electronics rotate the sample to ensure high uniformity of epilayer parameters across the wafer. SiC CVD systems capable of simultaneously growing epilayers on multiple wafers have enabled higher wafer throughput for SiC electronic device manufacture.

5.4.4.2 SiC Epitaxial Growth Polytype Control

Homoepitaxial growth, whereby the polytype of the SiC epilayer matches the polytype of the SiC substrate, is accomplished by "step-controlled" epitaxy [50–52]. Step-controlled epitaxy is based upon growing epilayers on an SiC wafer polished at an angle (called the "tilt-angle" or "off-axis angle") of typically 3°–8° off the (0 0 0 1) basal plane, resulting in a surface with atomic steps and relatively long, flat terraces between steps. When growth conditions are properly controlled and there is a sufficiently short distance between steps, Si and C adatoms impinging onto the growth surface find their way to step risers, where they bond and incorporate into the crystal. Thus, ordered, lateral "step-flow" growth takes place which enables the polytypic stacking sequence of the substrate to be exactly mirrored in the growing epilayer. SiC wafers cut with nonconventional surface orientations such as $(11\bar{2}0)$ and $(03\bar{3}8)$, provide a favorable surface geometry for epilayers to inherit stacking sequence (i.e., polytype) via step flow from the substrate [53,54].

When growth conditions are not properly controlled when steps are too far apart, as can occur with poorly prepared SiC substrate surfaces that are polished to within <1° of the (0 0 0 1) basal plane, growth adatoms island nucleate and bond in the middle of terraces instead of at the steps. Uncontrolled island nucleation (also referred to as terrace nucleation) on SiC surfaces leads to heteroepitaxial growth

of poor-quality 3C-SiC [51,52]. To help prevent spurious terrace nucleation of 3C-SiC during epitaxial growth, most commercial 4H- and 6H-SiC substrates are polished to tilt angles of 8° and 3.5° off the (0 0 0 1) basal plane, respectively. To date, all commercial SiC electronics rely on homoepitaxial layers that are grown on these "off-axis" prepared (0 0 0 1) *c*-axis SiC wafers.

Proper removal of residual surface contamination and defects left over from the SiC wafer cutting and polishing process is also vital to obtaining high-quality SiC epilayers with minimal dislocation defects. Techniques employed to better prepare the SiC wafer surface prior to epitaxial growth range from dry etching to chemical-mechanical polishing (CMP) [55]. As the SiC wafer is heated up in a growth chamber in preparation for initiation of epilayer growth, a high-temperature in-situ pregrowth gaseous etch (typically using H_2 and/or HCl) is usually carried out to further eliminate surface contamination and defects [46,56,57]. It is worth noting that optimized pregrowth processing enables step-flow growth of high-quality homoepilayers even when the substrate tilt angle is reduced to <0.1° off-axis from the (0 0 0 1) basal plane [56]. In this case, axial screw dislocations are required to provide a continual spiral template of steps needed to grow epilayers in the <0 0 0 1> direction while maintaining the hexagonal polytype of the substrate [58].

5.4.4.3 SiC Epilayer Doping

In-situ doping during CVD epitaxial growth is primarily accomplished through the introduction of nitrogen (usually N_2) for n-type and aluminum (usually trimethyl- or triethylaluminum) for p-type epilayers [10,59]. Some alternative dopants such as phosphorus and boron have also been investigated for the n-and p-type epilayers, respectively [59,60]. While some variation in epilayer doping can be carried out strictly by varying the flow of dopant gases, the site-competition doping methodology has enabled a much broader range of SiC doping to be accomplished [59,61]. In addition, site competition has also made moderate epilayer dopings more reliable and repeatable. The site-competition dopant-control technique is based on the fact that many dopants of SiC preferentially incorporate into either Si lattice sites or C lattice sites. As an example, nitrogen preferentially incorporates into lattice sites normally occupied by carbon atoms. By epitaxially growing SiC under carbon-rich conditions, most of the nitrogen present in the CVD system (whether it is a residual contaminant or intentionally introduced) can be excluded from incorporating into the growing SiC crystal. Conversely, by growing in a carbon-deficient environment, the incorporation of nitrogen can be enhanced to form very heavily doped epilayers for ohmic contacts. Aluminum, which is opposite to nitrogen, prefers the Si site of SiC, and other dopants have also been controlled through site competition by properly varying the Si/C ratio during crystal growth. SiC epilayer dopings ranging from 9×10^{14} to 1×10^{19} cm^{-3} are commercially available, and researchers have reported obtaining dopings over a factor of 10 larger and smaller than this range for the n- and p-type dopings [40]. The surface orientation of the wafer also affects the efficiency of doping incorporation during epilayer growth [54]. As of this writing, epilayers available for consumers to specify and purchase to meet their own device application needs have thickness and doping tolerances of ±25% and ±50%, respectively [40]. However, some SiC epilayers used for high-volume device production are far more optimized, exhibiting <5% variation in doping and thickness [41].

5.4.5 SiC Crystal Dislocation Defects

Table 5.2 summarizes the major known dislocation defects found in present-day commercial 4H- and 6H-SiC wafers and epilayers [10,39,41,62,63]. Since the active regions of devices reside in epilayers, the epilayer defect content is clearly of primary importance to SiC device performance. However, as evidenced by Table 5.2, most epilayer defects originate from dislocations found in the underlying SiC substrate prior to epilayer deposition. More details on the electrical impact of some of these defects on specific devices are discussed later in Section 5.6.

The micropipe defect is regarded as the most obvious and damaging "device-killer" defect to SiC electronic devices [64]. A micropipe is an axial screw dislocation with a hollow core (diameter of the order of a micrometer) in the SiC wafer and epilayer that extends roughly parallel to the crystallographic

c-axis normal to the polished *c*-axis wafer surface [65–67]. These defects impart considerable local strain to the surrounding SiC crystal that can be observed using X-ray topography or optical cross polarizers [39,41,68,69]. Over the course of a decade, substantial efforts by SiC material vendors has succeeded in reducing SiC wafer micropipe densities nearly 100-fold, and some SiC boules completely free of micropipes have been demonstrated [10,41,70]. In addition, epitaxial growth techniques for closing SiC substrate micropipes (effectively dissociating the hollow-core axial dislocation into multiple closed-core dislocations) have been developed [71]. However, this approach has not yet met the demanding electronic reliability requirements for commercial SiC power devices that operate at high electric fields [72].

Even though micropipe "device-killer" defects have been almost eliminated, commercial 4H- and 6H-SiC wafers and epilayers still contain very high densities (>10,000 cm^{-2}, summarized in Table 5.2) of other less-harmful dislocation defects. While these remaining dislocations are not presently specified in SiC material vendor specification sheets, they are nevertheless believed responsible for a variety of nonideal device behaviors that have hindered reproducibility and commercialization of some (particularly high electric field) SiC electronic devices [63,73,74]. Closed-core axial screw dislocation defects are similar in structure and strain properties to micropipes, except that their Burgers vectors are smaller so that the core is solid instead of a hollow void [66,67,75,76]. As shown in Table 5.2, basal plane dislocation defects and threading edge dislocation defects are also plentiful in commercial SiC wafers [39,62].

As discussed later in Section 5.6.4.1.2, 4H-SiC electrical device degradation caused by the expansion of stacking faults initiated from basal plane dislocation defects has hindered commercialization of bipolar power devices [63,74,77,78]. Similar stacking fault expansion has also been reported when doped 4H-SiC epilayers have been subjected to modest (~1150°C) thermal oxidation processing [79,80]. While epitaxial growth techniques to convert basal-plane dislocations into threading-edge dislocations have recently been reported, the electrical impact of threading-edge dislocations on the performance and reliability of high-electric field SiC devices remains to be fully ascertained [39]. It is also important to note that present-day commercial SiC epilayers still contain some undesirable surface morphological features such as "carrot defects" which could affect SiC device processing and performance [40,81,82].

In an exciting initial breakthrough, a Japanese team of researchers reported in 2004 that they achieved a 100-fold reduction in dislocation density in prototype 4H-SiC wafers of up to 3 in. in diameter [83]. While such greatly improved SiC wafer quality offered by this "multiple *a*-face" growth technique should prove highly beneficial to electronic (especially high-power) SiC device capabilities, it remains uncertain as of this writing as to when this significantly more complex (and therefore expensive) growth process will result in commercially viable mass-produced SiC wafers and devices.

5.5 SiC Device Fundamentals

To minimize the development and production costs of SiC electronics, it is important that SiC device fabrication takes advantage of existing silicon and GaAs wafer processing infrastructure as much as possible. As will be discussed in this section, most of the steps necessary to fabricate SiC electronics starting from SiC wafers can be accomplished using somewhat modified commercial silicon electronics processes and fabrication tools.

5.5.1 Choice of Polytype for Devices

As discussed in Section 4, 4H- and 6H-SiC are the far superior forms of semiconductor device quality SiC commercially available in mass-produced wafer form. Therefore, only 4H- and 6H-SiC device processing methods will be explicitly considered in the rest of this section. It should be noted, however, that most of the processing methods discussed in this section are applicable to other polytypes of SiC, except for the case of a 3C-SiC layer still residing on a silicon substrate, where all processing temperatures need to be kept well below the melting temperature of silicon (~1400°C). It is generally accepted that 4H-SiC's substantially higher carrier mobility and shallower dopant ionization energies compared to 6H-SiC (Table 5.1) should make it the polytype of choice for most SiC electronic devices, provided that all other device processing,

performance, and cost-related issues play out as being roughly equal between the two polytypes. Furthermore, the inherent mobility anisotropy that degrades conduction parallel to the crystallographic *c*-axis in 6H-SiC particularly favors 4H-SiC for vertical power device configurations (Section the 5.6.4). Because the ionization energy of the p-type acceptor dopants is significantly deeper than for the n-type donors, a much higher conductivity can be obtained for the n-type SiC substrates than for the p-type substrates.

5.5.2 SiC-Selective Doping: Ion Implantation

The fact that diffusion coefficients of most SiC dopants are negligibly small (at ≤1800°C) is excellent for maintaining device junction stability, because dopants do not undesirably diffuse as the device is operated long term at high temperatures. Unfortunately, this characteristic also largely (except for B at extreme temperatures [84]) precludes the use of conventional dopant diffusion, a highly useful technique widely employed in silicon microelectronics manufacturing, for patterned doping of SiC.

Laterally patterned doping of SiC is carried out by ion implantation. This somewhat restricts the depth that most dopants can be conventionally implanted to <1 μm using conventional dopants and implantation equipment. Compared to silicon processes, SiC ion implantation requires a much higher thermal budget to achieve acceptable dopant implant electrical activation. Summaries of ion implantation processes for various dopants can be found in [85–96]. Most of these processes are based on carrying out implantation at temperatures ranging from room temperature to 800°C using a patterned (sometimes high-temperature) masking material. The elevated temperature during implantation promotes some lattice self-healing during the implant, so that damage and segregation of displaced silicon and carbon atoms does not become excessive, especially in high-dose implants often employed for ohmic contact formation. Co-implantation of carbon with dopants has been investigated as a means to improve the electrical conductivity of the more heavily doped implanted layers [88,95,97].

Following implantation, the patterning mask is stripped and a higher temperature (~1200 to 1800°C) anneal is carried out to achieve maximum electrical activation of dopant ions. The final annealing conditions are crucial to obtaining desired electrical properties from ion-implanted layers. At higher implant anneal temperature, the SiC surface morphology can seriously degrade [87,98]. Because sublimation etching is driven primarily by loss of silicon from the crystal surface, annealing in silicon overpressures can be used to reduce surface degradation during high-temperature anneals [99]. Such overpressure can be achieved by close-proximity solid sources such as using an enclosed SiC crucible with SiC lid and/or SiC powder near the wafer, or by annealing in a silane-containing atmosphere. Similarly, robust deposited capping layers such as AlN and graphite, have also proven effective at better preserving SiC surface morphology during high-temperature ion implantation annealing [91,92].

As evidenced by a number of works, the electrical properties and defect structure of 4H-SiC doped by ion implantation and annealing are generally inferior to SiC doped in-situ during epitaxial growth [89,100–103]. Naturally, the damage imposed on the SiC lattice roughly scales with implantation dose. Even though reasonable electrical dopant activations have been achieved, thermal annealing processes developed to date for SiC have not been able to thoroughly repair all damage imposed on the crystal lattice by higher-dose ion implantations (such as those often used to form heavily doped layers in preparation of ohmic contact formation, Section 5.5.3). The degraded crystal quality of highly implanted SiC layers has been observed to degrade carrier mobilities and minority carrier lifetimes, thereby causing significant degradation to the electrical performance of some devices [90,103]. Until large further improvements to ion-implanted doping of SiC are developed, SiC device designs will have to account for nonideal behavior associated with SiC-implanted layers.

5.5.3 SiC Contacts and Interconnect

All useful semiconductor electronics require conductive signal paths in and out of each device as well as conductive interconnects to carry signals between devices on the same chip and to external circuit elements that reside off-chip. While SiC itself is theoretically capable of fantastic electrical operation

under extreme conditions (Section 5.3), such functionality is useless without contacts and interconnects that are also capable of operation under the same conditions. The durability and reliability of metal–semiconductor contacts and interconnects are one of the main factors limiting the operational high-temperature limits of SiC electronics. Similarly, SiC high-power device contacts and metallizations will have to withstand both high temperature and high current density stress never before encountered in silicon power electronics experience.

The subject of metal–semiconductor contact formation is a very important technical field too broad to be discussed in great detail here. For general background discussions on metal–semiconductor contact physics and formation, the reader should consult narratives presented in References 15 and 104. These references primarily discuss ohmic contacts to conventional narrow-bandgap semiconductors such as silicon and GaAs. Specific overviews of SiC metal–semiconductor contact technology can be found in References 105–110.

As discussed in References 105–110, there are both similarities and a few differences between SiC contacts and contacts to conventional narrow-bandgap semiconductors (e.g., silicon, GaAs). The same basic physics and current transport mechanisms that are present in narrow-bandgap contacts such as surface states, Fermi-pinning, thermionic emission, and tunneling, also apply to SiC contacts. A natural consequence of the wider bandgap of SiC is the higher effective Schottky barrier heights. Analogous with narrow-bandgap ohmic contact physics, the microstructural and chemical state of the SiC–metal interface is crucial to contact electrical properties. Therefore, premetal-deposition surface preparation, metal deposition process, choice of metal, and post-deposition annealing can all greatly impact the resulting performance of metal–SiC contacts. Because the chemical nature of the starting SiC surface is strongly dependent on surface polarity, it is not uncommon to obtain significantly different results when the same contact process is applied to the silicon face surface versus the carbon face surface.

5.5.3.1 SiC Ohmic Contacts

Ohmic contacts serve the purpose of carrying electrical current into and out of the semiconductor, ideally with no parasitic resistance. The properties of various ohmic contacts to SiC reported to date are summarized elsewhere [107–110]. While SiC-specific ohmic contact resistances at room temperature are generally higher than in contacts to narrow-bandgap semiconductors, they are nevertheless sufficiently low for most envisioned SiC applications. Lower specific contact resistances are usually obtained to n-type than to p-type 4H- and 6H-SiC. Consistent with narrow-bandgap ohmic contact technology, it is easier to make low-resistance ohmic contacts to heavily doped SiC and thermal annealing is almost always employed to promote favorable interfacial reactions.

Truly enabling harsh-environment SiC electronics will require ohmic contacts that can reliably withstand prolonged harsh-environment operation. Most reported SiC ohmic metallizations appear sufficient for long-term device operation up to 300°C. SiC ohmic contacts that withstand heat soaking under no electrical bias at 500–600°C for hundreds or thousands of hours in nonoxidizing gas or vacuum environments have also been demonstrated [110]. Only recently has successful long-term electrical operation of n-type ohmic contacts in oxidizing 500–600°C air ambients been demonstrated in relatively low-current density devices [111,112]. Further research is needed to obtain similarly durable high-temperature contacts to p-type SiC. Electromigration, oxidation, and other electrochemical reactions driven by high-temperature electrical bias in a reactive oxidizing environment are likely to limit SiC ohmic contact reliability for the most demanding applications that simultaneously require both high temperature and high power (i.e., high current density). The durability and reliability of SiC ohmic contacts is one of the critical factors limiting the practical high-temperature limits of SiC electronics.

5.5.3.2 SiC Schottky Contacts

Rectifying metal–semiconductor Schottky barrier contacts to SiC are useful for a number of devices, including commercialized SiC metal–semiconductor field-effect transistors (MESFETs) and fast-switching rectifiers [40,113]. References 105, 106, 108, and 114 summarize electrical results obtained in a variety

of SiC Schottky studies. Owing to the wide bandgap of SiC, almost all unannealed metal contacts to lightly doped 4H- and 6H-SiC are rectifying. Rectifying contacts permit extraction of Schottky barrier heights and diode ideality factors by well-known current–voltage (*I*–*V*) and capacitance–voltage (*C*–*V*) electrical measurement techniques [104]. While these measurements show a general trend that Schottky junction barrier height does somewhat depend on metal–semiconductor work function difference, the dependence is weak enough to suggest that surface state charge also plays a significant role in determining the effective barrier height of SiC Schottky junctions. At least some experimental scatter exhibited for identical metals can be attributed to surface cleaning and metal deposition process differences, as well as different barrier height measurement procedures. For example, the work by Teraji et al. [115], in which two different surface-cleaning procedures prior to titanium deposition lead to ohmic behavior in one case and rectifying behavior in the other, clearly shows that the process plays a significant role in determining SiC Schottky contact electrical properties.

It is important to note that nonuniformities in electrical behavior, many of which have been traced to SiC crystal defects (Section 5.4.5) have been documented to exist across the lateral area of most SiC Schottky contacts with areas $>10^{-4}$ cm^2 [116–118]. Furthermore, the reverse current drawn in experimental SiC diodes, while small, is nevertheless larger than expected based on theoretical substitution of SiC parameters into well-known Schottky diode reverse leakage current equations developed for narrow-bandgap semiconductors. Models based on spatially localized Schottky barrier lowering as well as quantum mechanical tunneling owing to higher SiC electric fields, have been proposed to explain the nonideal reverse leakage behavior of SiC Schottky diodes [119–121]. In addition, electric field crowding along the edge of a SiC Schottky contact can also lead to increased reverse-bias leakage current and reduced reverse breakdown voltage [15,18,104]. Edge-termination techniques to relieve electric field edge crowding and improve Schottky rectifier reverse properties are briefly discussed later in Section 5.6.4. The practical operation of rectifying SiC Schottky diodes is usually limited to temperatures below 400°C; above this temperature, reverse-bias thermionic emission leakage current and thermally driven SiC–metal interface degradation (via material intermixing and chemical reactions) tend to become undesirably large.

5.5.4 Patterned Etching of SiC for Device Fabrication

At room temperature, there are no known conventional wet chemicals that etch single-crystal SiC. Most patterned etching of SiC for electronic devices and circuits is accomplished using dry etching techniques. The reader should consult References 122–124 which contain summaries of dry SiC etching results obtained to date. The most commonly employed process involves reactive ion etching (RIE) of SiC in fluorinated plasmas. Sacrificial etch masks (such as aluminum metal) are deposited and photolithographically patterned to protect desired areas from being etched. The SiC RIE process can be implemented using standard silicon RIE hardware and typical 4H- and 6H-SiC RIE etch rates of the order of hundreds of angstroms per minute. Well-optimized SiC RIE processes are typically highly anisotropic with little undercutting of the etch mask, leaving smooth surfaces. One of the keys to achieving smooth surfaces is preventing "micromasking", wherein the masking material is slightly etched and randomly redeposited onto the sample effectively masking very small areas on the sample that were intended for uniform etching. This can result in "grass"-like etch-residue features being formed in the unmasked regions, which is undesirable in most cases.

While RIE etch rates are sufficient for many electronic applications, much higher SiC etch rates are necessary to carve features of the order of tens to hundreds of micrometers deep that are needed to realize advanced sensors, MEMS, and through-wafer holes useful for SiC RF devices. High-density plasma dry-etching techniques such as electron cyclotron resonance and inductively coupled plasma have been developed to meet the need for deep etching of SiC. Residue-free patterned etch rates exceeding a thousand angstroms a minute have been demonstrated [122,123,125–128].

Patterned etching of SiC at very high etch rates has also been demonstrated using photo-assisted and dark electrochemical wet etching [129,130]. By choosing proper etching conditions, this technique has demonstrated a very useful dopant-selective etch-stop capability. However, there are major incompatibilities

of the electrochemical process that make it undesirable for VLSI mass production, including extensive preetching and postetching sample preparation, etch isotropy and mask undercutting, and somewhat nonuniform etching across the sample. Laser etching techniques are capable of etching large features, such as via through-wafer holes useful for RF chips [131].

5.5.5 SiC Insulators: Thermal Oxides and MOS Technology

The vast majority of semiconductor-integrated circuit chips in use today rely on silicon metal-oxide–semiconductor field-effect transistors (MOSFETs), whose electronic advantages and operational device physics are summarized in Katsumata's chapter and elsewhere [15,18,132]. Given the extreme usefulness and success of inversion channel MOSFET-based electronics in VLSI silicon (as well as discrete silicon power devices), it is naturally desirable to implement high-performance inversion channel MOSFETs in SiC. Like silicon, SiC forms a thermal SiO_2 when it is sufficiently heated in an oxygen environment. While this enables SiC MOS technology to somewhat follow the highly successful path of silicon MOS technology, there are nevertheless important differences in insulator quality and device processing that are presently preventing SiC MOSFETs from realizing their full beneficial potential. While the following discourse attempts to quickly highlight key issues facing SiC MOSFET development, more detailed insights can be found in References 133–142.

From a purely electrical point of view, there are two prime operational deficiencies of SiC oxides and MOSFETs compared to silicon MOSFETs. First, effective inversion channel mobilities in most SiC MOSFETs are lower than one would expect based on silicon inversion channel MOSFET carrier mobilities. This seriously reduces the transistor gain and current-carrying capability of SiC MOSFETs, so that SiC MOSFETs are not nearly as advantageous as theoretically predicted. Second, SiC oxides have not proven as reliable and immutable as well-developed silicon oxides, in that SiC MOSFETs are more prone to threshold voltage shifts, gate leakage, and oxide failures than comparably biased silicon MOSFETs. In particular, SiC MOSFET oxide electrical performance deficiencies are attributed to differences between silicon and SiC thermal oxide quality and interface structure that cause the SiC oxide to exhibit undesirably higher levels of interface state densities ($\sim10^{11}$–10^{13} eV^{-1} cm^{-2}), fixed oxide charges ($\sim10^{11}$–10^{12} cm^{-2}), charge trapping, carrier oxide tunneling, and lowered mobility of inversion channel carriers.

In highlighting the difficulties facing SiC MOSFET development, it is important to keep in mind that early silicon MOSFETs also faced developmental challenges that took many years of dedicated research efforts to successfully overcome. Indeed, tremendous improvements in 4H-SiC MOS device performance have been achieved in recent years, giving hope that beneficial 4H-SiC power MOSFET devices for operation up to 125°C ambient temperatures might become commercialized within the next few years. For example, 4H-SiC MOSFET inversion channel mobility for conventionally oriented (8° off (0001) *c*-axis) wafers has improved from <10 to >200 $cm^2/V^{-1}s^{-1}$, while the density of electrically detrimental SiC–SiO_2 interface state defects energetically residing close to the conduction band edge has dropped by an order of magnitude [141,143,144]. Likewise, alternative SiC wafer surface orientations such as $(11\bar{2}0)$ and $(03\bar{3}8)$ that are obtained by making devices on wafers cut with different crystallographic orientations (Section 5.2.1), have also yielded significantly improved 4H-SiC MOS channel properties [54,139]. One key step to obtaining greatly improved 4H-SiC MOS devices has been the proper introduction of nitrogen-compound gases (in the form of N_2, NO, N_2O, or NH_3) during the oxidation and post-oxidation annealing process [136,137,141,142]. These nitrogen-based anneals have also improved the stability of 4H-SiC oxides to high electric field and high-temperature stressing used to qualify and quantify the reliability of MOSFETs [140]. However, as Agarwal et al. [145] have pointed out, the wide bandgap of SiC reduces the potential barrier impeding tunneling of damaging carriers through oxides grown on 4H-SiC, so that 4H-SiC oxides cannot be expected to attain identical high reliability as thermal oxides on silicon. It is highly probable that alternative gate insulators besides thermally grown SiO_2 will have to be developed for optimized implementation of inversion channel 4H-SiC insulated gate transistors for the most demanding high-temperature and high-power electronic applications. As

with silicon MOSFET technology, multilayer dielectric stacks will likely be developed to further enhance SiC MOSFET performance [133,146].

5.5.6 SiC Device Packaging and System Considerations

Hostile-environment SiC semiconductor devices and ICs are of little advantage if they cannot be reliably packaged and connected to form a complete system capable of hostile-environment operation. With proper material selection, modifications of existing IC packaging technologies appear feasible for non-power SiC circuit packaging up to 300°C [147]. Recent work is beginning to address the needs of the most demanding aerospace electronic applications, whose requirements include operation in high-vibration 500–600°C oxidizing-ambient environments, sometimes with very high power [7,148–152]. For example, some prototype electronic packages and circuit boards that can withstand over a thousand hours at 500°C have been demonstrated. Harsh-environment passive components such as inductors, capacitors, and transformers, must also be developed for operation in demanding conditions before the full system-level benefits of SiC electronics discussed in Section 5.3 can be successfully realized.

5.6 SiC Electronic Devices and Circuits

This section briefly summarizes a variety of SiC electronic device designs broken down by major application areas. SiC process and material technology issues limiting the capabilities of various SiC device topologies are highlighted as key issues to be addressed in further SiC technology maturation. Throughout this section, it should become apparent to the reader that the most difficult general challenge preventing SiC electronics from fully attaining beneficial capabilities is attaining long-term high operational reliability, while operating in previously unattained temperature and power density regimes. Because many device reliability limitations can be traced to fundamental material and junction/interface issues already mentioned in Sections 5.4 and 5.5, efforts to enable useful (i.e., reliable) SiC electronics should focus on improvements to these fundamental areas.

5.6.1 SiC Optoelectronic Devices

The wide bandgap of SiC is useful for realizing short-wavelength blue and ultraviolet (UV) optoelectronics. 6H-SiC-based pn junction light-emitting diodes (LEDs) were the first semiconductor devices to cover the blue portion of the visible color spectrum, and became the first SiC-based devices to reach high-volume commercial sales [153]. Because SiC's bandgap is indirect (i.e., the conduction minimum and valence band maximum do not coincide in crystal momentum space), luminescent recombination is inherently inefficient [154]. Therefore, LEDs based on SiC pn junctions were rendered quite obsolete by the emergence of much brighter, much more efficient direct-bandgap Group III-nitride (III-N such as GaN, and InGaN) blue LEDs [155]. However, SiC wafers are still employed as one of the substrates (along with sapphire) for growth of III-N layers used in high-volume manufacture of green and blue nitride-based LEDs.

SiC has proven much more efficient at absorbing short-wavelength light, which has enabled the realization of SiC UV-sensitive photodiodes that serve as excellent flame sensors in turbine-engine combustion monitoring and control [153,156]. The wide bandgap of 6H-SiC is useful for realizing low photodiode dark currents as well as sensors that are blind to undesired near-infrared wavelengths produced by heat and solar radiation. Commercial SiC-based UV flame sensors, again based on epitaxially grown dry-etch mesa-isolated 6H-SiC pn junction diodes, have successfully reduced harmful pollution emissions from gas-fired ground-based turbines used in electrical power generation systems [156]. The low dark-currents of SiC diodes are also useful for X-ray, heavy ion, and neutron detection in nuclear reactor monitoring and enhanced scientific studies of high-energy particle collisions and cosmic radiation [157,158].

5.6.2 SiC RF Devices

The main use of SiC RF devices appears to lie in high-frequency solid-state high-power amplification at frequencies from around 600 MHz (UHF-band) to perhaps as high as a few gigahertz (X-band). As discussed in far greater detail in References 5, 6, 25, 26, 159, and elsewhere, the high breakdown voltage and high thermal conductivity coupled with high carrier saturation velocity allow SiC RF transistors to handle much higher power densities than their silicon or GaAs RF counterparts, despite SiC's disadvantage in low-field carrier mobility (Table 5.1). The higher thermal conductivity of SiC is also crucial in minimizing channel self-heating so that phonon scattering does not seriously degrade carrier velocity. These material advantage RF power arguments apply to a variety of different transistor structures such as MESFETs and static induction transistors (SITs) and other wide bandgap semiconductors (such as Group III-nitrides) besides SiC. The high power density of wide bandgap transistors will prove quite useful in realizing solid-state transmitter applications, where higher power with smaller size and mass are crucial. Fewer transistors capable of operating at higher temperatures reduce matching and cooling requirements, leading to reduced overall size and cost of these systems.

SiC-based high-frequency RF MESFETs are now commercially available [40]. However, it is important to note that this occurred after years of fundamental research tracked down and eliminated poor reliability owing to charge-trapping effects arising from immature semi-insulating substrates, device epilayers, and surface passivation [159]. One key material advancement that enabled reliable operation was the development of "high-purity"semi-insulating SiC substrates (needed to minimize parasitic device capacitances) with far less charge trapping induced than the previously developed vanadium-doped semi-insulating SiC wafers. SiC MESFET devices fabricated on semi-insulating substrates are conceivably less susceptible to adverse yield consequences arising from micropipes than vertical high-power switching devices, primarily because a *c*-axis micropipe can no longer short together two conducting sides of a high field junction in most areas of the lateral channel MESFET structure.

SiC mixer diodes also show excellent promise for reducing undesired intermodulation interference in RF receivers [160–162]. More than 20 dB dynamic range improvement was demonstrated using non-optimized SiC Schottky diode mixers. Following further development and optimization, SiC-based mixers should improve the interference immunity in situations (such as in aircraft or ships) where receivers and high-power transmitters are closely located.

5.6.3 SiC High-Temperature Signal-Level Devices

Most analog signal conditioning and digital logic circuits are considered "signal level" in that individual transistors in these circuits do not typically require any more than a few milliamperes of current and <20 V to function properly. Commercially available silicon-on-insulator circuits can perform complex digital and analog signal-level functions up to 300°C when high-power output is not required [163]. Besides ICs in which it is advantageous to combine signal-level functions with high-power or unique SiC sensors/MEMS onto a single chip, more expensive SiC circuits solely performing low-power signal-level functions appear largely unjustifiable for low-radiation applications at temperatures below 250–300°C [7].

As of this writing, there are no commercially available semiconductor transistors or integrated circuits (SiC or otherwise) for use in ambient temperatures above 300°C. Even though SiC-based high-temperature laboratory prototypes have improved significantly over the last decade, achieving long-term operational reliability remains the primary challenge of realizing useful 300–600°C devices and circuits. Circuit technologies that have been used to successfully implement VLSI circuits in silicon and GaAs such as CMOS, ECL, BiCMOS, DCFL, etc., are to varying degrees candidates for $T > 300°C$ SiC-integrated circuits. High-temperature gate-insulator reliability (Section 5.5.5) is critical to the successful realization of MOSFET-based integrated circuits. Gate-to-channel Schottky diode leakage limits the peak operating temperature of SiC MESFET circuits to around 400°C (Section 5.5.3.2). Therefore, pn junction-based devices such as bipolar junction transistors (BJTs) and junction field effect transistors (JFETs), appear to be stronger (at least in the nearer term) candidate technologies to attain long-duration operation in

300–600°C ambients. Because signal-level circuits are operated at relatively low electric fields well below the electrical failure voltage of most dislocations, micropipes and other SiC dislocations affect signal-level circuit process yields to a much lesser degree than they affect high-field power device yields.

As of this writing, some discrete transistors and small-scale prototype logic and analog amplifier SiC-based ICs have been demonstrated in the laboratory using SiC variations of NMOS, CMOS, JFET, and MESFET device topologies [164–170]. However, none of these prototypes are commercially viable as of this writing, largely owing to their inability to offer prolonged-duration electrically stable operation at ambient temperatures beyond the ~250–300°C realm of silicon-on-insulator technology. As discussed in Section 5.5, a common obstacle to all high-temperature SiC device technologies is reliable long-term operation of contacts, interconnect, passivation, and packaging at $T > 300$°C. By incorporating highly durable high-temperature ohmic contacts and packaging, prolonged continuous electrical operation of a packaged 6H-SiC field effect transistor at 500°C in oxidizing air environment was recently demonstrated [111,112,149].

As further improvements to fundamental SiC device processing technologies (Section 5.5) are made, increasingly durable $T > 300$°C SiC-based transistor technology will evolve for beneficial use in harsh-environment applications. Increasingly complex high-temperature functionality will require robust circuit designs that accommodate large changes in device operating parameters over the much wider temperature ranges (as large as 650°C spread) enabled by SiC. Circuit models need to account for the fact that SiC device epilayers are significantly "frozen-out" owing to deeper donor and acceptor dopant ionization energies, so that nontrivial percentages of device-layer dopants are not ionized to conduct current near room temperature [171]. Because of these carrier freeze-out effects, it will be difficult to realize SiC-based ICs operational at junction temperatures much lower than –55°C (the lower end of U.S. Mil-Spec. temperature range).

5.6.4 SiC High-Power Switching Devices

The inherent material properties and basic physics behind the large theoretical benefits of SiC over silicon for power switching devices were discussed Section 5.3.2. Similarly, it was discussed in Section 5.4.5 that crystallographic defects found in SiC wafers and epilayers are presently a primary factor limiting the commercialization of useful SiC high-power switching devices. This section focuses on the additional developmental aspects of SiC power rectifiers and power switching transistor technologies.

Most SiC power device prototypes employ similar topologies and features as their silicon-based counterparts such as vertical flow of high current through the substrate to maximize device current using minimal wafer area (i.e., maximize current density) [18]. In contrast to silicon, however, the relatively low conductivity of present-day p-type SiC substrates (Section 5.4.3) dictates that all vertical SiC power device structures be implemented using n-type substrates in order to achieve beneficially high vertical current densities. Many of the device design trade-offs roughly parallel well-known silicon power device trade-offs, except for the fact that numbers for current densities, voltages, power densities, and switching speeds are much higher in SiC.

For power devices to successfully function at high voltages, peripheral breakdown owing to edge-related electric field crowding [15,18,104] must be avoided through careful device design and proper choice of insulating/passivating dielectric materials. The peak voltage of many prototype high-voltage SiC devices has often been limited by destructive edge-related breakdown, especially in SiC devices capable of blocking multiple kilovolts. In addition, most testing of many prototype multikilovolt SiC devices has required the device to be immersed in specialized high-dielectric strength fluids or gas atmospheres to minimize damaging electrical arcing and surface flashover at device peripheries. A variety of edge-termination methodologies, many of which were originally pioneered in silicon high-voltage devices, have been applied to prototype SiC power devices with varying degrees of success, including tailored dopant and metal guard rings [172–179]. The higher voltages and higher local electric fields of SiC power devices will place larger stresses on packaging and on wafer insulating materials, so some of the materials used to insulate/passivate silicon high-voltage devices may not

prove sufficient for reliable use in SiC high-voltage devices, especially if those devices are to be operated at high temperatures.

5.6.4.1 SiC High-Power Rectifiers

The high-power diode rectifier is a critical building block of power conversion circuits. Recent reviews of experimental SiC rectifier results are given in References 3, 134, 172, 180, and 181. Most important SiC diode rectifier device design trade-offs roughly parallel well-known silicon rectifier trade-offs, except for the fact that current densities, voltages, power densities, and switching speeds are much higher in SiC. For example, semiconductor Schottky diode rectifiers are majority carrier devices that are well known to exhibit very fast switching owing to the absence of minority carrier charge storage that dominates (i.e., slows, adversely resulting in undesired waste power and heat) the switching operation of bipolar pn junction rectifiers. However, the high breakdown field and wide energy bandgap permit operation of SiC metal–semiconductor Schottky diodes at much higher voltages (above 1 kV) than is practical with silicon-based Schottky diodes that are limited to operation below ~200 V owing to much higher reverse-bias thermionic leakage.

5.6.4.1.1 SiC Schottky Power Rectifiers.

4H-SiC power Schottky diodes (with rated blocking voltages up to 1200 V and rated on-state currents up to 20 A as of this writing) are now commercially available [40,113]. The basic structure of these unipolar diodes is a patterned metal Schottky anode contact residing on top of a relatively thin (roughly of the order of 10 μm in thickness) lightly n-doped homoepitaxial layer grown on a much thicker (around 200–300 μm) low-resistivity n-type 4H-SiC substrate (8° off axis, as discussed in Section 5.4.4.2) with backside cathode contact metallization [172,182]. Guard ring structures (usually p-type implants) are usually employed to minimize electric field crowding effects around the edges of the anode contact. Die passivation and packaging help prevent arcing/surface flashover harmful to reliable device operation.

The primary application of these devices to date has been switched-mode power supplies, where (consistent with the discussion in Section 5.3.2) the SiC Schottky rectifier's faster switching with less power loss has enabled higher frequency operation and shrinking of capacitors, inductors and the overall power supply size and weight [3,23]. In particular, the effective absence of minority carrier charge storage enables the unipolar SiC Schottky devices to turn off much faster than the silicon rectifiers (which must be pn junction diodes above ~200 V blocking) which must dissipate injected minority carrier charge energy when turned off. Even though the part cost of SiC rectifiers has been higher than competing silicon rectifiers, an overall lower power supply system cost with useful performance benefits is nevertheless achieved. It should be noted, however, that changes in circuit design are sometimes necessary to best enhance circuit capabilities with acceptable reliability when replacing silicon with SiC components.

As discussed in Section 5.4.5, SiC material quality presently limits the current and voltage ratings of SiC Schottky diodes. Under high forward bias, Schottky diode current conduction is primarily limited by the series resistance of the lightly doped blocking layer. The fact that this series resistance increases with temperature (owing to decreased epilayer carrier mobility) drives equilization of high forward currents through each diode when multiple Schottky diodes are paralleled to handle higher on-state current ratings [17].

5.6.4.1.2 Bipolar and Hybrid Power Rectifiers.

For higher voltage applications, bipolar minority carrier charge injection (i.e., conductivity modulation) should enable SiC pn diodes to carry higher current densities than unipolar Schottky diodes whose drift regions conduct solely using dopant-atom majority carriers [19–21,172,180]. Consistent with silicon rectifier experience, SiC pn junction generation-related reverse leakage is usually smaller than thermionic-assisted Schottky diode reverse leakage. As with silicon bipolar devices, reproducible control of minority carrier lifetime will be essential in optimizing the switching-speed versus on-state current density performance trade-offs of SiC bipolar devices for specific applications. Carrier lifetime reduction via intentional impurity incorporation and introduction of radiation-induced defects appears feasible. However,

TABLE 5.2 Major Types of Extended Crystal Defects Reported in SiC Wafers and Epilayers

Crystal Defect	Density in Wafer (cm^{-2})	Density in Epilayer (cm^{-2})	Comments
Micropipe (Hollow-core axial screw dislocation)	~10–100 (0)	~10–100 (0)	Known to cause severe reduction in power device breakdown voltage and increase in off-state leakage
Closed–core axial screw dislocation	~10^3–10^4 (~10^2)	~10^3–10^4 (~10^2)	Known to cause reduction in device breakdown voltage, increase in leakage current, reduction in carrier lifetime
Basal plane dislocation	~10^4 (~10^2)	~10^2–10^3 (<10)	Known nucleation source of expanding stacking faults leading to bipolar power device degradation, reduction in carrier lifetime
Threading-edge dislocation	~10^2–10^3 (~10^2)	~10^4 (~10^2)	Impact not well known
Stacking faults (disruption of stacking sequence)	~10–10^4 (0)	~10–10^4 (0)	Faults known to degrade bipolar power devices, reduce carrier lifetime
Carrot defects	N/A	1–10 (0)	Known to causes severe reduction in power device breakdown voltage and increase in off-state leakage
Low-angle grain boundaries	~10^2–10^3 (0)	~10^2–10^3 (0)	Usually more dense near edges of wafers, impact not well known

Note: Numbers in parentheses denote research laboratory "best" results that were not commercially available for use in SiC electronics manufacture in 2005.

the ability to obtain consistently long minority carrier lifetimes (above a microsecond) has proven somewhat elusive as of this writing, indicating that further improvement to SiC material growth processes are needed to enable the full potential of bipolar power rectifiers to be realized [183].

As of this writing, SiC bipolar power rectifiers are not yet commercially available. Poor electrical reliability caused by electrically driven expansion of 4H-SiC epitaxial layer stacking faults initiated from basal plane dislocation defects (Table 5.2) effectively prevented concerted efforts for commercialization of 4H-SiC pn junction diodes in the late 1990s [63,74,184]. In particular, bipolar electron–hole recombination that occurs in forward-biased pn junctions drove the enlargement of stacking disorder in the 4H-SiC blocking layer, forming an enlarging quantum well (based on narrower 3C-SiC bandgap) that effectively degrades transport (diffusion) of minority carriers across the lightly doped junction blocking layer. As a result, the forward voltages of 4H-SiC pn rectifiers required to maintain rated on-state current increase unpredictably and undesirably over time. As discussed in Section 5.4.5, research toward understanding and overcoming this material defect-induced problem has made important progress, so that hopefully SiC bipolar power devices might become commercialized within a few years [39,41].

A drawback of the wide bandgap of SiC is that it requires larger forward-bias voltages to reach the turn-on "knee" of a diode where significant on-state current begins flowing. In turn, the higher knee voltage can lead to an undesirable increase in on-state power dissipation. However, the benefits of 100× decreased drift region resistance and much faster dynamic switching should greatly overcome SiC on-state knee voltage disadvantages in most high-power applications. While the initial turn-on knee of SiC pn junctions is higher (around 3 V) than for SiC Schottky junctions (around 1 V), conductivity modulation enables SiC pn junctions to achieve lower forward voltage drop for higher blocking voltage applications [172,180].

Hybrid Schottky/pn rectifier structures first developed in silicon that combine pn junction reverse blocking with low Schottky forward turn-on should prove extremely useful in realizing application-optimized SiC rectifiers [134,172,180,181]. Similarly, combinations of dual Schottky metal structures and trench pinch rectifier structures can also be used to optimize SiC rectifier forward turn-on and reverse leakage properties [185].

5.6.4.2 SiC High-Power Switching Transistors

Three terminal power switches that use small drive signals to control large voltages and currents (i.e., power transistors) are also critical building blocks of high-power conversion circuits. However, as of this writing, SiC high-power switching transistors are not yet commercially available for beneficial use in power system circuits. As well summarized in References 134, 135, 172, 180, and 186–188, a variety of improving three-terminal SiC power switches have been prototyped in recent years.

The present lack of commercial SiC power switching transistors is largely due to several technological difficulties discussed elsewhere in this chapter. For example, all high-power semiconductor transistors contain high-field junctions responsible for blocking current flow in the off-state. Therefore, performance limitations imposed by SiC crystal defects on diode rectifiers (Sections 5.4.5 and 5.6.4.1) also apply to SiC high-power transistors. Also, the performance and reliability of inversion channel SiC-based MOS field-effect gates (i.e., MOSFETs, IGBTs, etc.) has been limited by poor inversion channel mobilities and questionable gate-insulator reliability discussed in Section 5.5.5. To avoid these problems, SiC device structures that do not rely on high-quality gate insulators, such as the MESFET, JFET, BJT, and depletion-channel MOSFET, have been prototyped toward use as power switching transistors. However, these other device topologies impose non-standard requirements on power system circuit design that make them unattractive compared with the silicon-based inversion-channel MOSFETs and IGBTs. In particular, silicon power MOSFETs and IGBTs are extremely popular in power circuits largely because their MOS gate drives are well insulated from the conducting power channel, require little drive signal power, and the devices are "normally off" in that there is no current flow when the gate is unbiased at 0 V. The fact that the other device topologies lack one or more of these highly circuit-friendly aspects has contributed to the inability of SiC-based devices to beneficially replace silicon-based MOSFETs and IGBTs in power system applications.

As discussed in Section 5.5.5, continued substantial improvements in 4H-SiC MOSFET technology will hopefully soon lead to the commercialization of 4H-SiC MOSFETs. In the meantime, advantageous high-voltage switching by pairing a high-voltage SiC JFET with a lower-voltage silicon power MOSFETs into a single module package appears to be nearing practical commercialization [188]. Numerous designs for SiC doped-channel FETs (with both lateral and vertical channels) have been prototyped, including depletion-channel (i.e., buried or doped channel) MOSFETs, JFETs, and MESFETs [187]. Even though some of these have been designed to be "normally-off" at zero applied gate bias, the operational characteristics of these devices have not (as of this writing) offered sufficient benefits relative to cost to enable commercialization.

Substantial improvements to the gain of prototype 4H-SiC power BJTs have been achieved recently, in large part by changing device design to accommodate for undesired large minority carrier recombination occurring at p-implanted base contact regions [103]. IGBTs, thyristors, Darlington pairs, and other bipolar power device derivatives from silicon have also been prototyped in SiC [134,180,186]. Optical transistor triggering, a technique quite useful in previous high-power silicon device applications, has also been demonstrated for SiC bipolar devices [189]. However, because all bipolar power transistors operate with at least one pn junction injecting minority carriers under forward bias, crystal defect-induced bipolar degradation discussed for pn junction rectifiers (Section 5.6.4.1.2) also applies to the performance of bipolar transistors. Therefore, the effective elimination of basal plane dislocations from 4H-SiC epilayers must be accomplished before any power SiC bipolar transistor devices can become sufficiently reliable for commercialization. SiC MOS oxide problems (Section 5.5.5) will also have to be solved to realize beneficial SiC high-voltage IGBTs. However, relatively poor p-type SiC substrate conductivity may force development of p-IGBTs instead of n-IGBT structures that presently dominate in silicon technology.

As various fundamental SiC power device technology challenges are overcome, a broader array of SiC power transistors tackling increasingly widening voltage, current, and switching speed specification will enable beneficial new power system circuits.

5.6.5 SiC MicroElectromechanical Systems (MEMS) and Sensors

As described in Hesketh's chapter on micromachining in this book, the development and use of silicon-based MEMS continues to expand. While the previous sections of this chapter have centered on the use

of SiC for traditional semiconductor electronic devices, SiC is also expected to play a significant role in emerging MEMS applications [124,190]. SiC has excellent mechanical properties that address some shortcomings of silicon-based MEMS such as extreme hardness and low friction reducing mechanical wear-out as well as excellent chemical inertness to corrosive atmospheres. For example, SiCs excellent durability is being examined as enabling for long-duration operation of electric micromotors and micro jet-engine power generation sources where the mechanical properties of silicon appear to be insufficient [191].

Unfortunately, the same properties that make SiC more durable than silicon also make SiC more difficult to micromachine. Approaches to fabricating harsh-environment MEMS structures in SiC and prototype SiC-MEMS results obtained to date are reviewed in References 124 and 190. The inability to perform fine-patterned etching of single-crystal 4H- and 6H-SiC with wet chemicals (Section 5.5.4) makes micromachining of this electronic-grade SiC more difficult. Therefore, the majority of SiC micromachining to date has been implemented in electrically inferior heteroepitaxial 3C-SiC and polycrystalline SiC deposited on silicon wafers. Variations of bulk micromachining, surface micromachining, and micromolding techniques have been used to fabricate a wide variety of micromechanical structures, including resonators and micromotors. A standardized SiC on silicon wafer micromechanical fabrication process foundry service, which enables users to realize their own application-specific SiC micromachined devices while sharing wafer space and cost with other users, is commercially available [192].

For applications requiring high temperature, low-leakage SiC electronics not possible with SiC layers deposited on silicon (including high-temperature transistors, as discussed in Section 5.6.2), concepts for integrating much more capable electronics with MEMS on 4H/6H SiC wafers with epilayers have also been proposed. For example, pressure sensors being developed for use in higher temperature regions of jet engines are implemented in 6H-SiC, largely owing to the fact that low junction leakage is required to achieve proper sensor operation [152,193]. On-chip 4H/6H integrated transistor electronics that beneficially enable signal conditioning at the high-temperature sensing site are also being developed [112]. With all micromechanical-based sensors, it is vital to package the sensor in a manner that minimizes the imposition of thermomechanical induced stresses (which arise owing to thermal expansion coefficient mismatches over much larger temperature spans enabled by SiC) onto the sensing elements. Therefore (as mentioned previously in Section 5.5.6), advanced packaging is almost as critical as the use of SiC toward usefully expanding the operational envelope of MEMS in harsh environments.

As discussed in Section 5.3.1, a primary application of SiC harsh-environment sensors is to enable active monitoring and control of combustion engine systems to improve fuel efficiency while reducing pollution. Toward this end, SiC's high-temperature capabilities have enabled the realization of catalytic metal–SiC and metal-insulator–SiC prototype gas sensor structures with great promise for emission monitoring applications and fuel system leak detection [194,195]. High-temperature operation of these structures, not possible with silicon, enables rapid detection of changes in hydrogen and hydrocarbon content to sensitivities of parts per million in very small-sized sensors that could easily be placed unobtrusively on an engine without the need for cooling. However, further improvements to the reliability, reproducibility, and cost of SiC-based gas sensors are needed before these systems will be ready for widespread use in consumer automobiles and aircraft. In general, the same can be said for most SiC MEMS, which will not achieve widespread beneficial system insertion until high reliability in harsh environments is assured via further technology development.

5.7 Future of SiC

It can be safely predicted that SiC will never displace silicon as the dominant semiconductor used for the manufacture of the vast majority of the world's electronic chips that are primarily low-voltage digital and analog chips targeted for operation in normal human environments (computers, cell phones, etc.). SiC will only be used where substantial benefits are enabled by SiC's ability to expand the envelope of high-power and high-temperature operational conditions such as the applications described in Section 5.3. Perhaps,

the only major existing application area where SiC might substantially displace today's use of silicon is the area of discrete power devices used in power conversion, motor control, and management circuits.

The power device market, along with the automotive sensing market present the largest-volume market opportunity for SiC-based semiconductor components. However, the end consumers in both of these applications demand excruciatingly high reliability (i.e., no operational failures) combined with competitively low overall cost. For SiC electronics technology to have large impact, it must greatly evolve from its present status to meet these demands. There is clearly a very large discrepancy between the revolutionary broad theoretical promise of SiC semiconductor electronics technology (Section 5.3) versus the operational capability of SiC-based components that have actually been deployed in only a few commercial and military applications (Section 5.6). Likewise, a large discrepancy also exists between the capabilities of laboratory SiC devices compared with commercially deployed SiC devices. The inability of many "successful" SiC laboratory prototypes to rapidly transition to commercial product demonstrates both the difficulty and criticality of achieving acceptable reliability and costs.

5.7.1 Future Tied to Material Issues

The previous sections of this chapter have already highlighted major known technical obstacles and immaturities that are largely responsible for hindered SiC device capability. In the most general terms, these obstacles boil down to a handful of key fundamental material issues. The rate at which the most critical of these fundamental issues is solved will greatly impact the availability, capability, and usefulness of SiC semiconductor electronics. Therefore, the future of SiC electronics is linked to investment in basic material research toward solving challenging material-related impediments to SiC device performance, yield, and reliability.

The material challenge that is arguably the biggest key to the future of SiC is the removal of dislocations from SiC wafers. As described previously in this chapter and references therein, the most important SiC power rectifier performance metrics, including device ratings, reliability, and cost are inescapably impacted by high dislocation densities present in commercial SiC wafers and epilayers. If mass-produced SiC wafer quality approached that of silicon wafers (which typically contain less than one dislocation defect per square centimeter), far more capable SiC unipolar and bipolar high-power rectifiers (including devices with kilovolt and kiloampere ratings) would rapidly become widely available for beneficial use in a far larger variety of high-power applications. Similar improvements would also be realized in SiC transistors, paving the way for SiC high-power devices to indeed beneficially displace silicon-based power devices in a tremendously broad and useful array of applications and systems (Section 5.3). This advancement would unlock a much more rapid and broad SiC-enabled power electronic systems "revolution" compared to the relatively slower "evolution" and niche-market insertion that has occurred since SiC wafers were first commercialized roughly 15 years ago. As mentioned in Section 5.4, recent laboratory results [83] indicate that drastic reductions in SiC wafer dislocations are possible using radically new approaches to SiC wafer growth compared to standard boule-growth techniques practiced by all commercial SiC wafer vendors for over a decade. Arguably, the ultimate future of SiC high-power devices may hinge on the development and practical commercialization of low dislocation density SiC growth techniques substantially different from those employed today.

It is important to note that other emerging wide bandgap semiconductors besides SiC theoretically offer similarly large electrical system benefits over silicon semiconductor technology as described in Section 5.3. For example, diamond and some Group III-nitride compound semiconductors (such as GaN; Table 5.1) have high breakdown field and low intrinsic carrier concentration that enables operation at power densities, frequencies, and temperatures comparable to or exceeding SiC. Like SiC, however, electrical devices in these semiconductors are also hindered by a variety of difficult material challenges that must be overcome in order for beneficially high performance to be reliably achieved and commercialized. If SiC electronics capability expansion evolves too slowly compared to other wide bandgap semiconductors, the possibility exists that the latter will capture applications and markets originally envisioned for SiC. However, if SiC succeeds in being the first to offer reliable and cost-effective wide

bandgap capability to a particular application, subsequent wide-bandgap technologies would probably need to achieve far better cost/performance metrics in order to displace SiC. It is therefore likely that SiC, to some degree, will continue its evolution toward expanding the operational envelope of semiconductor electronics capability.

5.7.2 Further Recommended Reading

This chapter has presented a brief summary overview of evolving SiC semiconductor device technology. The following publications, which were heavily referenced in this chapter, are highly recommended as supplemental reading to more completely cover SiC electronics technology development in much greater technical detail than possible within this short chapter.

Reference 11 is a collection of invited in-depth papers from recognized leaders in SiC technology development that first appeared in special issues of the journal *Physica Status Solidi* (a 162 (1)) and (b 202, (1)) in 1997. In 2003, the same editors published a follow-on book [12] containing additional invited papers to update readers on new "recent major advances" in SiC since the 1997 book.

One of the best sources of the most up-to-date SiC electronics technology development information is the *International Conference on Silicon Carbide and Related Materials (ICSCRM)*, which is held every 2 years (years ending in odd numbers). To bridge the 24-month gap between international SiC meetings, the *European Conference on Silicon Carbide and Related Materials (ECSCRM)* is held in years ending in even numbers. Since 1999, the proceedings of peer-reviewed papers presented at both the International and European SiC conferences have been published by Trans Tech Publications as volumes in its Materials Science Forum offering, which are available online via paid subscription (http://www.scientific.net). In addition, the meetings of the Materials Research Society (MRS) often hold symposiums and publish proceedings (book and online editions; http://www.mrs.org) dedicated to SiC electronics technology development. Reference 200 is the proceedings of the most recent MRS SiC symposium held in April 2004, and the next such symposium is scheduled for the 2006 MRS spring meeting in San Francisco.

The following technical journal issues contain collections of invited papers from SiC electronics experts that offer more detailed insights than this-chapter, yet are conveniently brief compared to other volumes already mentioned in this section:

1. *Proceedings of the IEEE*, Special Issue on Wide Bandgap Semiconductor Devices, 90 (6), June 2002.
2. *Materials Research Society Bulletin*, Advances in Silicon Carbide Electronics, 30(4), April 2005.

In addition, a variety of internet websites contain useful SiC information and links can be located using widely available internet search engine services. The author of this chapter maintains a website that contains information and links to other useful SiC internet websites at http://www.grc.nasa.gov/WWW/SiC/.

References

1. Baliga, B.J., "Power Semiconductor Devices for Variable-Frequency Drives," *Proceedings of the IEEE* 82(8), 1112, 1994.
2. Baliga, B.J., "Trends in Power Semiconductor Devices," *IEEE Transactions on Electron Devices* 43(10), 1717, 1996.
3. Elasser, A. and Chow, T.P., "Silicon Carbide Benefits and Advantages for Power Electronics Circuits and Systems," *Proceedings of the IEEE* 90(6), 969, 2002.
4. Johnson, C.M., "Clear road ahead?" *Power Engineer* 18(4), 34, 2004.
5. Weitzel, C.E., Palmour, J.W., Carter, C.H., Jr., Moore, K., Nordquist, K.J., Allen, S., Thero, C., and Bhatnagar, M., "Silicon Carbide High Power Devices," *IEEE Transactions on Electron Devices* 43(10), 1732, 1996.

6. Trew, R.J., "SiC and GaN Transistors—Is There One Winner for Microwave Power Applications," *Proceedings of the IEEE* 90(6), 1032, 2002.
7. Neudeck, P.G., Okojie, R.S., and Chen, L.-Y., "High-Temperature Electronics—A Role for Wide-Bandgap Semiconductors," *Proceedings of the IEEE* 90(6), 1065, 2002.
8. Bhatnagar, M. and Baliga, B.J., "Comparison of 6H-SiC, 3C-SiC, and Si for Power Devices," *IEEE Transactions on Electron Devices* 40(3), 645, 1993.
9. Powell, J.A., Pirouz, P., and Choyke, W.J., "Growth and Characterization of Silicon Carbide Polytypes for Electronic Applications," in *Semiconductor Interfaces, Microstructures, and Devices: Properties and Applications*, Ed. Feng, Z.C., Institute of Physics Publishing, Bristol, United Kingdom, 1993, p. 257.
10. Powell, A.R. and Rowland, L.B., "SiC Materials—Progress, Status, and Potential Roadblocks," *Proceedings of the IEEE* 90(6), 942, 2002.
11. Choyke, W.J., Matsunami, H., and Pensl, G., *Silicon Carbide—A Review of Fundamental Questions and Applications to Current Device Technology*, Wiley-VCH, Berlin, 1997.
12. Choyke, W.J., Matsunami, H., and Pensl, G., *Silicon Carbide: Recent Major Advances,* Springer, Berlin, 2003.
13. Ioffe Physico-Technical Institute, http://www.ioffe.ru/SVA/NSM/Semicond/SiC.
14. Pierret, R.F., *Advanced Semiconductor Fundamentals,* Addison-Wesley, Reading, MA, 1987.
15. Sze, S.M., *Physics of Semiconductor Devices, 2nd ed.*, Wiley-Interscience, New York, 1981.
16. Dreike, P.L., Fleetwood, D.M., King, D.B., Sprauer, D.C., and Zipperian, T.E., "An Overview of High-Temperature Electronic Device Technologies and Potential Applications," *IEEE Transactions on Components, Packaging, and Manufacturing Technology* 17(4), 594, 1994.
17. Kodani, K., Matsurnoto, T., Saito, S., Takao, K., Mogi, T., Yatsuo, T., and Arai, K., "Evaluation of parallel and series connection of silicon carbide Schottky barrier diode (SiC-SBD)," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, 2004, p. 3971.
18. Baliga, B.J., *Modern Power Devices, 1st ed.*, Wiley, New York, 1987.
19. Ruff, M., Mitlehner, H., and Helbig, R., "SiC Devices: Physics and Numerical Simulation," *IEEE Transactions on Electron Devices* 41(6), 1040, 1994.
20. Chow, T.P., Ramungul, N., and Ghezzo, M., "Wide-Bandgap Semiconductor Power Devices," in Power Semiconductor Materials and Devices, *Materials Research Society Symposia Proceedings*, vol. 483, Eds. Pearton, S.J., Shul, R.J., Wolfgang, E., Ren, F., and Tenconi, S., Materials Research Society, Warrandale, PA, 1998, p. 89.
21. Bakowski, M., Gustafsson, U., and Lindefelt, U., "Simulation of SiC High-Power Devices," *Physica Status Solidi (a)* 162(1), 421, 1997.
22. Tolbert, L.M., Ozpineci, B., Islam, S.K., and Peng, F.Z., "Impact of SiC Power Electronic Devices for Hybrid Electric Vehicles," in *2002 Future Car Congress Proceedings,* June 3–5, 2002, Arlington, VA, Soceity of Automotive Engineers, Warrendale, PA, 2002.
23. Rupp, R. and Zverev, I., "System Design Considerations for Optimizing the Benefit by Unipolar SiC Power Devices," in Silicon Carbide 2002—Materials, Processing and Devices, *Materials Research Society Symposia Proceedings,* vol. 742, Eds. Saddow, S.E., Larkin, D.J., Saks, N.S., Schoener, A., and Skowronski, M., Materials Research Society, Warrendale, PA, 2003, p. 329.
24. Trew, R.J., "Experimental and Simulated Results of SiC Microwave Power MESFETs," *Physica Status Solidi (a)* 162(1), 409, 1997.
25. Clarke, R.C. and Palmour, J.W., "SiC Microwave Power Technologies," *Proceedings of the IEEE* 90(6), 987, 2002.
26. Morvan, E., Kerlain, A., Dua, C., and Brylinski, C., "Development of SiC Devices for Microwave and *RF* Power Amplifiers," in *Silicon Carbide: Recent Major Advances*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer Berlin, 2003, p. 839.
27. Baliga, B.J., "Power ICs In The Saddle," *IEEE Spectrum* 32(7), 34, 1995.
28. Heydt, G.T. and Skromme, B.J., "Applications of High-Power Electronic Switches In The Electric Power Utility Industry and The Needs For High-Power Switching Devices," in Power Semiconductor

Materials and Devices, *Materials Research Society Symposia Proceedings*, vol. 483, Eds. Pearton, S.J., Shul, R.J., Wolfgang, E., Ren, F., and Tenconi, S., Materials Research Society, Warrandale, PA, 1998, p. 3.
29. Ozpineci, B., Tolbert, L.M., Islam, S.K., and Hasanuzzaman, M., “System Impact of Silicon Carbide Power Devices,” *International Journal of High Speed Electronics and Systems* 12(2), 439, 2002.
30. Johnson, C.M., “Comparison of Silicon and Silicon Carbide Semiconductors for a 10 kV Switching Application,” in *IEEE 35th Annual Power Electronics Specialists Conference*, IEEE, Piscataway, NJ, 2004, p. 572.
31. Ericsen, T., “Future Navy Application of Wide Bandgap Power Semiconductor Devices,” *Proceedings of the IEEE* 90(6), 1077, 2002.
32. Acheson, A.G., England Patent 17911, 1892.
33. Lely, J.A., “Darstellung von Einkristallen von Silicium carbid und Beherrschung von Art und Menge der eingebautem Verunreingungen,” *Ber. Deut. Keram. Ges.* 32, 229, 1955.
34. Nishino, S., Powell, J.A., and Will, H.A., “Production of Large-Area Single-Crystal Wafers of Cubic SiC for Semiconductor Devices,” *Applied Physics Letters* 42(5), 460, 1983.
35. Pirouz, P., Chorey, C.M., and Powell, J.A., “Antiphase Boundaries in Epitaxially Grown Beta-SiC,” *Applied Physics Letters* 50(4), 221, 1987.
36. Nagasawa, H., Yagi, K., Kawahara, T., Hatta, N., Pensl, G., Choyke, W.J., Yamada, T., Itoh, K.M., and Schöner, A., “Low-Defect 3*C*-SiC Grown on Undulant-Si (001) Substrates,” in *Silicon Carbide: Recent Major Advances*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer, Berlin, 2003, p. 207.
37. Tairov, Y.M. and Tsvetkov, V.F., “Investigation of Growth Processes of Ingots of Silicon Carbide Single Crystals,” *Journal of Crystal Growth* 43, 209, 1978.
38. Tairov, Y.M. and Tsvetkov, V.F., “General Principles of Growing Large-Size Single Crystals of Various Silicon Carbide Polytypes,” *Journal of Crystal Growth* 52, 146, 1981.
39. Sumakeris, J.J., Jenny. J.R., and Powell, A.R., “Bulk Crystal Growth, Epitaxy, and Defect Reduction in Silicon Carbide Materials For Microwave and Power Devices,” *MRS Bulletin* 30(4), 280, 2005.
40. Cree, Inc., http://www.cree.com.
41. Powell, A.R., Sumakeris, J.J., Leonard, R.T., Brady, M.F., Muller, S.G., Tsvetkov, V.F., Hobgood, H.M.D., Burk, A.A., Paisley, M.J., and Glass, R.C., “Status of 4H-SiC Substrate and Epitaxial Materials for Commercial Power Applications,” in Silicon Carbide 2004—Materials, Processing and Devices, *Materials Research Society Symposium Proceedings*, vol. 815, Eds. Dudley, M., Gouma, P., Kimoto, T., Neudeck, P.G., and Saddow, S.E., Materials Research Society, Warrendale, PA, 2004, p. 3.
42. Ellison, A., Magnusson, B., Sundqvist, B., Pozina, G., Bergman, J.P., Janzen, E., and Vehanen, A., “SiC Crystal Growth by HTCVD,” in Silicon Carbide and Related Materials 2003, *Materials Science Forum*, vol. 457–460, Eds. Madar, R., Camassel, J., and Blanquet, E., Trans Tech, Switzerland, 2004, p. 9.
43. Balkrishna, V., Augustine, G., Gaida, W.E., Thomas, R.N., and Hopkins, R.H., “Advanced Physical Vapor Transport Method and Apparatus for Growing High-Purity Single-Crystal Silicon Carbide,” US Patent 6,056,820, 2000.
44. Ohtani, N., Katsuno, M., Fujimoto, T., and Yashiro, H., “Defect Formation and Reduction During Bulk SiC Growth,” in *Silicon Carbide: Recent Major Advances*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer, Berlin, 2003, p. 137.
45. Davis, R.F., Kelner, G., Shur, M., Palmour, J.W., and Edmond, J.A., “Thin Film Deposition and Microelectronic and Optoelectronic Device Fabrication and Characterization in Monocrystalline Alpha and Beta Silicon Carbide,” *Proceedings of the IEEE* 79(5), 677, 1991.
46. Schöner, A., “New Development in Hot Wall Vapor Phase Epitaxial Growth of Silicon Carbide,” in *Silicon Carbide: Recent Major Advances*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer, Berlin, 2003, p. 229.
47. Kordina, O., Hallin, C., Henry, A., Bergman, J.P., Ivanov, I., Ellison, A., Son, N.T., and Janzen, E., “Growth of SiC by” “Hot-Wall” “CVD and HTCVD,” *Physica Status Solidi (b)* 202(1), 321, 1997.
48. Fanton, M., Skowronski, M., Snyder, D., Chung, H.J., Nigam, S., Weiland, B., and Huh, S.W., “Growth of Bulk SiC by Halide Chemical Vapor Deposition,” in Silicon Carbide and Related Materials 2003,

Materials Science Forum, vol. 457–460, Eds. Madar, R., Camassel, J., and Blanquet, E., Trans Tech, Switzerland, 2004, p. 87.

49. Rupp, R., Wiedenhofer, A., and Stephani, D., "Epitaxial Growth of SiC in a Single and a Multi Wafer Vertical CVD System: A Comparison," *Materials Science and Engineering B* 61–62, 125, 1999.
50. Kong, H.S., Glass, J.T., and Davis, R.F., "Chemical Vapor Deposition and Characterization of 6H-SiC Thin Films on Off-Axis 6H-SiC Substrates," *Journal of Applied Physics* 64, 2672, 1988.
51. Kimoto, T., Itoh, A., and Matsunami, H., "Step-Controlled Epitaxial Growth of High-Quality SiC Layers," *Physica Status Solidi (b)* 202(1), 247, 1997.
52. Powell, J.A. and Larkin, D.J., "Process-Induced Morphological Defects in Epitaxial CVD Silicon Carbide," *Physica Status Solidi (b)* 202(1), 529, 1997.
53. Burk, A.A., Jr. and Rowland, L.B., "Homoepitaxial VPE Growth of SiC Active Layers," *Physica Status Solidi (b)* 202(1), 263, 1997.
54. Kimoto, T., Yano, H., Negoro, Y., Hashimoto, K., and Matsunami, H., "Epitaxial Growth and Device Processing of SiC on Non-Basal Planes," in *Silicon Carbide: Recent Major Advances*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer, Berlin, 2003, p. 711.
55. Monnoye, S., Turover, D., and Vincente, P., "Surface Preparation Techniques for SiC Wafers," in *Silicon Carbide: Recent Major Advances*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer, Berlin, 2003, p. 699.
56. Powell, J.A., Petit, J.B., Edgar, J.H., Jenkins, I.G., Matus, L.G., Yang, J.W., Pirouz, P., Choyke, W.J., Clemen, L., and Yoganathan, M., "Controlled Growth of 3C-SiC and 6H-SiC Films on Low-Tilt-Angle Vicinal (0001) 6H-SiC Wafers," *Applied Physics Letters* 59(3), 333, 1991.
57. Burk, A.A., Jr. and Rowland, L.B., "The Role of Excess Silicon and In Situ Etching on 4H-SiC and 6H-SiC Epitaxial Layer Morphology," *Journal of Crystal Growth* 167(3–4), 586, 1996.
58. Neudeck, P.G. and Powell, J.A., "Homoepitaxial and Heteroepitaxial Growth on Step-Free SiC Mesas," in *Recent Major Advances in SiC*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer, Berlin, 2003, p. 179.
59. Larkin, D.J., "SiC Dopant Incorporation Control Using Site-Competition CVD," *Physica Status Solidi (b)* 202(1), 305, 1997.
60. Wang, R., Bhat, I.B., and Chow, T.P., "Epitaxial growth of n-type SiC using phosphine and nitrogen as the precursors," *Journal of Applied Physics* 92(12), 7587, 2002.
61. Larkin, D.J., Neudeck, P.G., Powell, J.A., and Matus, L.G., "Site-Competition Epitaxy for Superior Silicon Carbide Electronics," *Applied Physics Letters* 65(13), 1659, 1994.
62. Ha, S., Mieszkowski, P., Skowronski, M., and Rowland, L.B., "Dislocation Conversion in 4H Silicon Carbide Epitaxy," *Journal of Crystal Growth* 244(3–4), 257, 2002.
63. Lendenmann, H., Dahlquist, F., Bergman, J.P., Bleichner, H., and Hallin, C., "High-Power SiC Diodes: Characteristics, Reliability and Relation to Material Defects," in Silicon Carbide and Related Materials 2001, *Materials Science Forum*, vol. 389–393, Eds. Yoshida, S., Nishino, S., Harima, H., and Kimoto, T., Trans Tech Publications, Switzerland, 2002, p. 389.
64. Neudeck, P.G. and Powell, J.A., "Performance Limiting Micropipe Defects in Silicon Carbide Wafers," *IEEE Electron Device Letters* 15(2), 63, 1994.
65. Yang, J.-W., "SiC: Problems in Crystal Growth and Polytypic Transformation," PhD, Case Western Reserve University, 1993.
66. Si, W., Dudley, M., Glass, R., Tsvetkov, V., and Carter, C.H., Jr., "Hollow-Core Screw Dislocations in 6H-SiC Single Crystals: A Test of Frank's Theory," *Journal of Electronic Materials* 26(3), 128, 1997.
67. Si, W. and Dudley, M., "Study of Hollow-Core Screw Dislocations in 6H-SiC and 4H-SiC Single Crystals," in Silicon Carbide, III-Nitrides, and Related Materials, *Materials Science Forum*, vol. 264–268, Eds. Pensl, G., Morkoc, H., Monemar, B., and Janzen, E., Trans Tech Publications, Switzerland, 1998, p. 429.

68. Dudley, M., Huang, X., and Vetter, W.M., "Synchrotron White Beam X-Ray Topography and High-Resolution X-Ray Diffraction Studies of Defects in SiC Sibstrates, Epilayers and Device Structures," in *Silicon Carbide: Recent Major Advances*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer, Berlin, 2003, p. 629.
69. Ma, X., Dudley, M., Vetter, W., and Sudarshan, T., "Extended SiC Defects: Polarized Light Microscopy Delineation and Synchrotron White-Beam X-Ray Topography Ratification," *Japanese Journal of Applied Physics* 42(9A/B), L1077, 2003.
70. Basceri, C., Khlebnikov, I., Khlebnikov, Y., Sharma, M., Muzykov, P., Stratiy, G., Silan, M., and Balkas, C., "Micropipe-Free Single-Crystal Silicon Carbide (SiC) Ingots via Physical Vapor Transport (PVT)," in Silicon Carbide and Related Materials 2005, Materials Science Forum, vols. 527–529, Eds. Devaty, R.P., Larkin, D.J., and Saddow, S.E., *Trans Tech Publications,* Switzerland, 2006, p. 32.
71. Tsuchida, H., Kamata, I., Izumi, S., Tawara, T., Jikimoto, T., Miyanagi, T., Nakamura, T., and Izumi, K., "Homoepitaxial Growth and Characterization of Thick SiC Layers With a Reduced Micropipe Density," in Materials Research Society Symposium Proceedings, vol. 815, 2004, p. 35.
72. Rupp, R., Treu, M., Turkes, P., Beermann, H., Scherg, T., Preis, H., and Cerva, H., "Influence of Overgrown Micropipes in the Active Area of SiC Schottky Diodes on Long-Term Reliability," in Silicon Carbide and Related Materials 2004, *Materials Science Forum,* vols. 483–485, Eds. Nipoti, R., Poggi, A., and Scorzoni, A., Trans Tech Publicatons, Switzerland, 2005, p. 925.
73. Neudeck, P.G., Huang, W., and Dudley, M., "Study of Bulk and Elementary Screw Dislocation Assisted Reverse Breakdown in Low-Voltage (<250 V) 4H-SiC p^+n Junction Diodes—Part 1: DC Properties," *IEEE Transactions on Electron Devices* 46(3), 478, 1999.
74. Ha, S. and Bergman. J.P., "Degradation of SiC High-Voltage pin Diodes," *MRS Bulletin* 30(4), 305, 2005.
75. Wang, S., Dudley, M., Carter, C.H., Jr., Tsvetkov, V.F., and Fazi, C., "Synchrotron White Beam Topography Studies of Screw Dislocations in 6H-SiC Single Crystals," in Applications of Synchrotron Radiation Techniques to Materials Science, *Materials Research Society Symposium Proceedings*, vol. 375, Eds. Terminello, L., Shinn, N., Ice, G., D'Amico, K., and Perry, D., Materials Research Society, Warrandale, PA, 1995, p. 281.
76. Dudley, M., Wang, S., Huang, W., Carter, C.H., Jr., and Fazi, C., "White Beam Synchrotron Topographic Studies of Defects in 6H-SiC Single Crystals," *Journal of Physics D: Applied Physics* 28, A63, 1995.
77. Pirouz, P., Zhang, M., Galeckas, A., and Linnros, J., "Microstructural Aspects and Mechanism of Degradation of 4H-SiC PiN Diodes Under Forward Biasing," in *Materials Research Society Symposium Proceedings*, vol. 815, Eds. Dudley, M., Gouma, P., Kimoto, T., Neudeck, P.G., and Saddow, S.E., Materials Research Society, Warrendale, 2004, p. 91.
78. Stahlbush, R.E., Twigg, M.E., Sumakeris, J.J., Irvine, K.G., and Losee, P.A., "Mechanisms of Stacking Fault Growth in SiC PiN Diodes," in *Materials Research Society Symposium Proceedings*, vol. 815, Eds. Dudley, M., Gouma, P., Kimoto, T., Neudeck, P.G., and Saddow, S.E., Materials Research Society, Warrendale, PA, 2004, p. 103.
79. Okojie, R.S., Xhang, M., Pirouz, P., Tumakha, S., Jessen, G., and Brillson, L.J., "Observation of 4H-SiC to 3C-SiC Polytypic Transformation During Oxidation," *Applied Physics Letters* 79(19), 3056, 2001.
80. Okojie, R.S. and Zhang, M., "Thermoplastic Deformation and Residual Stress Topography of 4H-SiC Wafers," in *Materials Research Society Symposium Proceedings*, vol. 815, Eds. Dudley, M., Gouma, P., Kimoto, T., Neudeck, P.G., and Saddow, S.E., Materials Research Society, Warrendale, PA, 2004, p. 133.
81. Diaz-Guerra, C. and Piqueras, J., "Electron-beam-induced current study of electrically active defects in 4H-SiC," *Journal of Physics: Condensed Matter* 16(2), S217, 2004.
82. Wahab, Q., Ellison, A., Henry, A., Janzén, E., Hallin, C., Persio, J.D., and Martinez, R., "Influence of Epitaxial Growth and Substrate-Induced Defects on the Breakdown of 4H–SiC Schottky Diodes," *Applied Physics Letters* 76(19), 2725, 2000.
83. Nakamura, D., Gunjishima, I., Yamaguchi, S., Ito, T., Okamoto, A., Kondo, H., Onda, S., and Takatori, K., "Ultrahigh-Quality Silicon Carbide Single Crystals," *Nature* 430, 1109, 2004.

84. Soloviev, S., Gao, Y., Wang, X., and Sudarshan, T., “Boron Diffusion into 6H-SiC Through Graphite Mask,” *Journal of Electronic Materials* 30(3), 224, 2001.
85. Troffer, T., Schadt, M., Frank, T., Itoh, H., Pensl, G., Heindl, J., Strunk, H.P., and Maier, M., “Doping of SiC by Implantation of Boron and Aluminum,” *Physica Status Solidi (a)* 162(1), 277, 1997.
86. Kimoto, T., Itoh, A., Inoue, N., Takemura, O., Yamamoto, T., Nakajima, T., and Matsunami, H., “Conductivity Control of SiC by In-Situ Doping and Ion Implantation” , in Silicon Carbide, III-Nitrides, and Related Materials, *Materials Science Forum*, vols. 264–268, Eds. Pensl, G., Morkoc, H., Monemar, B., and Janzen, E., Trans Tech Publications, Switzerland, 1998, p. 675.
87. Capano, M., Ryu, S., Cooper, J. A. Jr., Melloch, M., Rottner, K., Karlsson, S., Nordell, N., Powell, A., and D. Walker, J., “Surface Roughening in Ion Implanted 4H-Silicon Carbide,” *Journal of Electronic Materials* 28(3), 214, 1999.
88. Tone, K. and Zhao, J., “A Comparative Study of C Plus Al Coimplantation and Al Implantation in 4H- and 6H-SiC,” *IEEE Transactions on Electron Devices* 46(3), 612, 1999.
89. Saks, N.S., Agarwal, A.K., Mani, S.S., and Hegde, V.S., “Low-Dose Nitrogen Implants in 6H–Silicon Carbide,” *Applied Physics Letters* 76(14), 1896, 2000.
90. Saks, N.S., Agarwal, A.K., Ryu, S.-H., and Palmour, J.W., “Low-dose Aluminum and Boron Impants in 4H and 6H Silicon Carbide,” *Journal of Applied Physics* 90(6), 2796, 2001.
91. Jones, K.A., Ervin, M.H., Shah, P.B., Derenge, M.A., Vispute, R.D., Venkatesan, T., and Freitas, J.A., “Electrical Activation Processes in Ion Implanted SiC Device Structures,” *AIP Conference Proceedings* 680(1), 694, 2003.
92. Negoro, Y., Katsumoto, K., Kimoto, T., and Matsunami, H., “Electronic Behaviors of High-Dose Phosphorus-Ion Implanted 4H-SiC (0001),” *Journal of Applied Physics* 96(1), 224, 2004.
93. Negoro, Y., Kimoto, T., and Matsunami, H., “Aluminum-Ion Implantation into 4H-SiC (11–20) and (0001)” , in *Materials Research Society Symposium Proceedings*, vol. 815, Eds. Dudley, M., Gouma, P., Kimoto, T., Neudeck, P.G., and Saddow, S.E., Materials Research Society, Warrendale, PA, 2004, p. 217.
94. Saks, N.S., Suvorov, A.V., and Capell, D.C., “High-Temperature High-Dose Implantation of Aluminium in 4H-SiC,” *Appled Physics Letters* 84(25), 5195, 2004.
95. Schmid, F. and Pensl, G., “Comparison of the Electrical Activation of P^+ and N^+ Ions Co-Implanted Along With Si^+ or C^+ Ions Into 4H-SiC,” *Applied Physics Letters* 84(16), 3064, 2004.
96. Negoro, Y., Kimoto, T., and Matsunami, H., “Technological Aspects of Ion Implantation in SiC Device Processes”, in Silicon Carbide and Related Materials 2004, *Materials Science Forum*, vols. 483–485, Eds. Nipoti, R., Poggi, A., and Scorzoni, A., Trans Tech Publicatons, Switzerland, 2005, p. 599.
97. Zhao, J.H., Tone, K., Weiner, S., R., Caleca, M.A., Du, H., and Withrow, S.P., “Evaluation of Ohmic Contacts to P-Type 6H-SiC Created by C and Al Coimplantation,” *IEEE Electron Device Letters* 18(8), 375, 1997.
98. Capano, M.A., Ryu, S., Melloch, M.R., Cooper, J.A., Jr., and Buss, M.R., “Dopant Activation and Surface Morphology of Ion Implanted 4H- and 6H-Silicon Carbide,” *Journal of Electronic Materials* 27(4), 370, 1998.
99. Rao, S., Saddow, S.E., Bergamini, F., Nipoti, R., Emirov, Y., and Agrawal, A., “A Robust Process for Ion Implant Annealing of SiC in a Low-Pressure Silane Ambient”, in Silicon Carbide 2004—Materials, Processing, and Devices, *Materials Research Society Symposium Proceedings*, vol. 815, Eds. Dudley, M., Gouma, P., Kimoto, T., Neudeck, P.G., and Saddow, S.E., Materials Research Society, Warrendale, PA, 2004, p. 229.
100. Pensl, G., Frank, T., Krieger, M., Laube, M., Reshanov, S., Schmid, F., and Weidner, M., “Implantation-Induced Defects in Silicon Carbide,” *Physica B: Condensed Matter* 340–342, 121, 2003.
101. Anwand, W., Brauer, G., Wirth, H., Skorupa, W., and Coleman, P.G., “The Influence of Substrate Temperature On the Evolution of Ion Implantation-Induced Defects in Epitaxial 6H-SiC,” *Applied Surface Science* 194(1–4), 127, 2002.
102. Ohno, T., Onose, H., Sugawara, Y., Asano, K., Hayashi, T., and Yatasuo, T., “Electron Microscopic Study on Residual Defects of Al+ or B+ Implanted 4H-SiC,” *Journal of Electronic Materials* 28(3), 180, 1999.

103. Huang, C.-F. and Cooper, J.A., Jr., “High Current Gain 4H-SiC npn Bipolar Junction Transistors,” *IEEE Electron Device Letters* 24(6), 396, 2003.
104. Rhoderick, E.H. and Williams, R.H., Metal-Semiconductor Contacts Clarendon Press, Oxford, UK, 1988.
105. Porter, L.M. and Davis, R.F., “A Critical Review of Ohmic and Rectifying Contacts for Silicon Carbide,” *Materials Science and Engineering B* B34, 83, 1995.
106. Bozack, M.J., “Surface Studies on SiC as Related to Contacts,” *Physica Status Solidi (b)* 202(1), 549, 1997.
107. Crofton, J., Porter, L.M., and Williams, J.R., “The Physics of Ohmic Contacts to SiC,” *Physica Status Solidi (b)* 202(1), 581, 1997.
108. Saxena, V. and Steckl, A.J., “Building Blocks for SiC Devices: Ohmic Contacts, Schottky Contacts, and p-n Junctions,” in *Semiconductors and Semimetals*, vol. 52, Academic Press, New York, 1998, p. 77.
109. Madsen, L., “Formation of Ohmic Conacts to α-SiC and Their Impact on Devices,” *Journal of Electronic Materials* 30(10), 1353, 2001.
110. Tanimoto, S., Okushi, H., and Arai, K., “Ohmic Contacts for Power Devices on SiC,” in *Silicon Carbide: Recent Major Advances*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer, Berlin, 2003, p. 651.
111. Okojie, R.S., Lukco, D., Chen, Y.L., and Spry, D.J., “Reliability assessment of Ti/TaSi2/Pt ohmic contacts on SiC after 1000 h at 600 °C,” *Journal of Applied Physics* 91(10), 6553, 2002.
112. Spry, D., Neudeck, P., Okojie, R., Chen, L.-Y., Beheim, G., Meredith, R., Mueller, W., and Ferrier, T., “Electrical Operation of 6H-SiC MESFET at 500 °C for 500 h in Air Ambient,” in *Proceedings 2004 IMAPS International Conference and Exhibition on High Temperature Electronics (HiTEC 2004),* May 19–12, 2004, Santa Fe, NM, International Microelectronics and Packaging Society (IMAPS), Washington, DC, 2004.
113. Infineon Technologies, http://www.infineon.com/sic.
114. Itoh, A. and Matsunami, H., “Analysis of Schottky Barrier Heights of Metal/SiC Contacts and Its Possible Application to High-Voltage Rectifying Devices,” *Physica Status Solidi (a)* 162(1), 389, 1997.
115. Teraji, T., Hara, S., Okushi, H., and Kajimura, K., “Ideal Ohmic Contact to n-Type 6H-SiC by Reduction of Schottky Barrier Height,” *Applied Physics Letters* 71(5), 689, 1997.
116. Schnabel, C.M., Tabib-Azar, M., Neudeck, P.G., Bailey, S.G., Su, H.B., Dudley, M., and Raffaelle, R.P., “Correlation of EBIC and SWBXT Imaged Defects and Epilayer Growth Pits in 6H-SiC Schottky Diodes,” in Silicon Carbide and Related Materials 1999, *Materials Science Forum*, vols. 338–342, Eds. Carter, C.H., Jr., Devaty, R.P., and Rohrer, G.S., Trans Tech Publications, Switzerland, 2000, p. 489.
117. Manfredotti, C., Vittone, E., Paolini, C., Olivero, P., Lo Giudice, A., Jaksic, M., and Barrett, R., “Investigation of 4H-SiC Schottky Diodes by Ion and X-ray Micro Beam Induced Charge Collection Techniques,” *Diamond and Related Materials* 12(3–7), 667, 2003.
118. Wang, Y., Ali, G.N., Mikhov, M.K., Vaidyanathan, V., Skromme, B.J., Raghothamachar, B., and Dudley, M., “Correlation Between Morphological Defects, Electron Beam-Induced Current Imaging, and the Electrical Properties of 4H-SiC Schottky Diodes,” *Journal of Applied Physics* 97(1), 013540, 2005.
119. Bhatnagar, M., Baliga, B.J., Kirk, H.R., and Rozgonyi, G.A., “Effect of Surface Inhomogenities on the Electrical Characteristics of SiC Schottky Contacts,” *IEEE Transactions on Electron Devices* 43(1), 150, 1996.
120. Crofton, J. and Sriram, S., “Reverse Leakage Current Calculations for SiC Schottky Contacts,” *IEEE Transactions on Electron Devices* 43(12), 2305, 1996.
121. Defives, D., Noblanc, O., Dua, C., Brylinski, C., Barthula, M., Aubry-Fortuna, V., and Meyer, F., “Barrier Inhomogeneities and Electrical Characteristics of Ti/4H-SiC Schottky Rectifiers,” *IEEE Transactons on Electron Devices* 46(3), 449, 1999.

122. Yih, P.H., Saxena, V., and Steckl, A.J., "A Review of SiC Reactive Ion Etching in Fluorinated Plasmas," *Physica Status Solidi (b)* 202(1), 605, 1997.
123. Beheim, G., "Deep Reactive Ion Etching of Silicon Carbide," in *The MEMS Handbook*, Ed. Gad-el-Hak, M., CRC Press, Boca Raton, FL, 2002, p. 21-1.
124. Zorman, C.A. and Mehregany, M., "Micromachining of SiC," in *Silicon Carbide: Recent Major Advances*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer, Berlin, 2003, p. 671.
125. Cao, L., Li, B., and Zhao, J.H., "Inductively Coupled Plasma Etching of SiC for Power Switching Device Fabrication", in Silicon Carbide, III-Nitrides, and Related Materials, *Materials Science Forum,* vols. 264–268, Eds. Pensl, G., Morkoc, H., Monemar, B., and Janzen, E., Trans Tech Publications, Switzerland, 1998, p. 833.
126. McLane, G.F. and Flemish, J.R., "High Etch Rates of SiC in Magnetron Enhanced SF_6 Plasmas," *Applied Physics Letters* 68(26), 3755, 1996.
127. Chabert, P., Proust, N., Perrin, J., and Boswell, R.W., "High rate etching of 4H–SiC using a SF_6/O_2 helicon plasma," *Applied Physics Letters* 76(16), 2310, 2000.
128. Cho, H., Leerungnawarat, P., Hays, D.C., Pearton, S.J., Chu, S.N.G., Strong, R.M., Zetterling, C.-M., Östling, M., and Ren, F., "Ultradeep, low-damage dry etching of SiC," *Applied Physics Letters* 76(6), 739, 2000.
129. Shor, J.S. and Kurtz, A.D., "Photoelectrochemical Etching of 6H-SiC," *Journal of the Electrochemical Society* 141(3), 778, 1994.
130. Shor, J.S., Kurtz, A.D., Grimberg, I., Weiss, B.Z., and Osgood, R.M., "Dopant-Selective Etch Stops in 6H and 3C SiC," *Journal of Applied Physics* 81(3), 1546, 1997.
131. Kim, S., Bang, B.S., Ren, F., D'Entremont, J., Blumenfeld, W., Cordock, T., and Pearton, S.J., "SiC Via Holes by Laser Drilling," *Journal of Electronic Materials* 33(5), 477, 2004.
132. Pierret, R.F., *Field Effect Devices*, Addison-Wesley, Reading, MA, 1983.
133. Afanas'ev, V.V., Ciobanu, F., Pensl, G., and Stesmans, A., "Contributions to the Density of Interface States in SiC MOS Structures," in *Silicon Carbide: Recent Major Advances*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer, Berlin, 2003, p. 343.
134. Agarwal, A., Das, M., Krishnaswami, S., Palmour, J., Richmond, J., and Ryu, S.H., "SiC Power Devices-An Overview," in Silicon Carbide 2004—Materials, Processing and Devices, *Materials Research Society Symposium Proceedings,* vol. 815, Eds. Dudley, M., Gouma, P., Kimoto, T., Neudeck, P.G., and Saddow, S.E., Materials Research Society, Warrendale, PA, 243, 2004.
135. Agarwal, A., Ryu, S.-H., and Palmour, J., "Power MOSFETs in 4H-SiC: Device Design and Technology," in *Silicon Carbide: Recent Major Advances*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer, Berlin, 2003, p. 785.
136. Dimitrijev, S., Harrison, H.B., Tanner, P., Cheong, K.Y., and Han, J., "Properties of Nitrided Oxides on SiC," in *Silicon Carbide: Recent Major Advances*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer, Berlin, 2003, p. 373.
137. Dimitrijev, S. and Jamet, P., "Advances in SiC power MOSFET technology," *Microelectronics Reliability* 43(2), 225, 2003.
138. Saks, N.S., "Hall Effect Studies of Electron Mobility and trapping at the SiC/SiO_2 Interface," in *Silicon Carbide: Related Major Advances*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer-Berlin, 2003, p. 387.
139. Kimoto, T., Kanzaki, Y., Noborio, M., Kawano, H., and Matsunami, H., "MOS Interface Properties and MOSFET Performance on 4H-SiC and Non-Basal Faces Processed by N_2O Oxidation," in Silicon Carbide 2004—Materials, Processing and Devices, *Materials Research Society Symposium Proceedings*, vol. 815, Eds. Dudley, M., Gouma, P., Kimoto, T., Neudeck, P.G., and Saddow, S.E., Materials Research Society, Warrendale, PA, 2004, p. 199.
140. Krishnaswami, S., Das, M.K., Agarwal, A.K., and Palmour, J.W., "Reliability of Nitrided Oxides in n- and p-Type 4H-SiC MOS Structures," in *Materials Research Society Symposium Proceedings,* vol. 815, Eds. Dudley, M., Gouma, P., Kimoto, T., Neudeck, P.G., and Saddow, S.E., Materials Research Society, Warrendale, PA, 2004, p. 205.

141. Das, M.K., "Recent Advances in (0001) 4H-SiC MOS Device Technology," in Silicon Carbide and Related Materials 2003, *Materials Science Forum*, vol. 457–460, Eds. Madar, R., Camassel, J., and Blanquet, E., Trans Tech, Switzerland, 2004, p. 1275.
142. Dhar, S., Wang. S, Williams, J.R., Pantelides, S.T., Feldman, L.C., "Interface Passivation for Silicon Dioxide Layers on Silicon Carbide," *MRS Bulletin* 30(4), 288, 2005.
143. Gudjonsson, G., Olafsson, H.O., Allerstam, F., Nilsson, P.-A., Sveinbjornsson, E.O., Zirath, H., Rodle, T., and Jos, R., "High Field-Effect Mobility in n-Channel Si Face 4H-SiC MOSFETs With Gate Oxide Grown On Aluminum Ion-Implanted Material," *IEEE Electron Device Letters* 26(2), 96, 2005.
144. Sveinbjornsson, E.O., Olafsson, H.O., Gudjonsson, G., Allerstam, F., Nilsson, P.A., Syvajarvi, M., Yakimova, R., Hallin, C., Rodle, T., and Jos, R., "High Field Effect Mobility in Si Face 4H-SiC MOSFET Made on Sublimation Grown Epitaxial Material," in Silicon Carbide and Related Materials 2004, *Materials Science Forum* vol. 483–485, Eds. Nipoti, R., Poggi, A., and Scorzoni, A., Trans Tech, Switzerland, 841, 2005.
145. Agarwal, A.K., Seshadri, S., and Rowland, L.B., "Temperature Dependence of Fowler-Nordheim Current in 6H- and 4H-SiC MOS Capacitors," *IEEE Electron Device Letters* 18(12), 592, 1997.
146. Tanimoto, S., Tanaka, H., Hayashi, T., Shimoida, Y., Hoshi, M., and Mihara, T., "High-reliability ONO Gate Dielectric for Power MOSFETs" , in Silicon Carbide and Related Materials 2004, *Materials Science Forum*, vol. 677–680, Eds. Nipoti, R., Poggi, A., and Scorzoni, A., Trans Tech, Switzerland, 2005, p. 677.
147. Johnson, R.W. and Williams, J., "SiC Power Device Packaging Technologies for 300 to 350 °C Applications," *Materials Science Forum* vol. 483–485, Eds. Nipoti, R., Poggi, A., and Scorzoni, A., Trans Tech, Switzerland, 785, 2005.
148. Salmon, J.S., Johnson, R.W., and Palmer, M., "Thick Film Hybrid Packaging Techniques for 500 °C Operation," in *4th International High Temperature Electronics Conference*, June 14–18, 1998, Albuquerque, NM, IEEE, Piscataway, NJ, 1998, p. 103.
149. Chen, L.-Y., Okojie, R.S., Neudeck, P.G., Hunter, G.W., and Lin, S.-T., "Material System for Packaging 500 °C MicroSystem," in Microelectronic, Optoelectronic, and MEMS Packaging, *Materials Research Society Symposia Proceedings*, vol. 682, Eds. Boudreaux, J.C., Dauskardt, R.H., Last, H.R., and McCluskey, F.P., Materials Research Society, Warrandale, PA, 2001.
150. Savrun, E., "Packaging Considerations for Very High Temperature Microsystems," in *Proceedings 2004 IMAPS International Conference and Exhibition on High Temperature Electronics (HiTEC 2004),* May 19–12, 2004, Santa Fe, NM, International Microelectronics and Packaging Society (IMAPS), Washington, DC, 2004.
151. Casady, J.B., Dillard, W.C., Johnson, R.W., and Rao, U., "A hybrid 6H-SiC temperature sensor operational from 25 °C to 500 °C," *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A* 19(3), 416, 1996.
152. Okojie, R.S., Savrun, E., Phong, N., Vu, N., and Blaha, C., "Reliability Evaluation of Direct Chip Attached Silicon Carbide Pressure Transducers," in *Proceedings of the 2004 IEEE Sensors Conference*, 2004, p. 635.
153. Edmond, J., Kong, H., Suvorov, A., Waltz, D., and Carter, C., Jr., "6H-Silicon Carbide Light-Emitting Diodes and UV Photodiodes," *Physica Status Solidi (a)* 162(1), 481, 1997.
154. Bergh, A.A. and Dean, P.J., *Light-Emitting Diodes,* Clarendon Press, Oxford, 1976.
155. Edmond, J., Abare, A., Bergman, M., Bharathan, J., Lee Bunker, K., Emerson, D., Haberern, K., Ibbetson, J., Leung, M., Russel, P., and Slater, D., "High Efficiency GaN-Based LEDs and Lasers on SiC," *Journal of Crystal Growth* 272(1–4), 242, 2004.
156. Brown, D.M., Downey, E., Kretchmer, J., Michon, G., Shu, E., and Schneider, D., "SiC Flame Sensors for Gas Turbine Control Systems," *Solid-State Electronics* 42(5), 755, 1998.
157. Bertuccio, G., Binetti, S., Caccia, S., Casiraghi, R., Castaldini, A., Cavallini, A., Lanzieri, C., LeDonne, A., Nava, F., and Pizzini, S., "Silicon Carbide for Alpha, Beta, Ion and Soft X-Ray High-Performance Detectors," in *Materials Science Forum* vols. 483–485, Eds. Nipoti, R., Poggi, A., and Scorzoni, A., Trans Tech, Switzerland, 2005, p. 1015.

158. Seshadri, S., Dulloo, A., Ruddy, F., Seidel, J., and Rowland, L., "Demonstration of an SiC Neutron Detector for High-Radiation Environments," *IEEE Transactions on Electron Devices* 46(3), 567, 1999.
159. Sriram, S., Ward. A., Henning, J., and Allen. S.T., "SiC MESFETs for High-Frequency Applications," *MRS Bulletin* 30(4), 308, 2005.
160. Fazi, C. and Neudeck, P., "Use of Wide-Bandgap Semiconductors to Improve Intermodulation Distortion in Electronic Systems," in Silicon Carbide, III-Nitrides, and Related Materials, *Materials Science Forum*, vols. 264–268, Eds. Pensl, G., Morkoc, H., Monemar, B., and Janzen, E., Trans Tech Publications, Switzerland, 1998, p. 913.
161. Eriksson, J., Rorsman, N., and Zirath, H., "4H-Silicon Carbide Schottky Barrier Diodes for Microwave Applications," *IEEE Transactions on Microwave Theory and Techniques* 51(3), 796, 2003.
162. Simons, R.N. and Neudeck, P.G., "Intermodulation-distortion performance of silicon-carbide Schottky-barrier RF mixer diodes," *IEEE Transactions on Microwave Theory and Techniques* 51(2), 669, 2003.
163. Honeywell Solid State Electronics Center, http://www.ssec.honeywell.com.
164. Xie, W., Cooper, J.A., Jr., and Melloch, M.R., "Monolithic NMOS Digital Integrated Circuits in 6H-SiC," *IEEE Electron Device Letters* 15(11), 455, 1994.
165. Brown, D.M., Ghezzo, M., Kretchmer, J., Krishnamurthy, V., Michon, G., and Gati, G., "High-Temperature Silicon Carbide Planar IC Technology and First Monolithic SiC Operational Amplifier IC," in *Transactions Second International High Temperature Electronics Conference*, June 5–10, 1994, Charlotte, NC, Sandia National Laboratories, Albuquerque, NM, 1994, p. XI.
166. Brown, D.M., Downey, E., Ghezzo, M., Kretchmer, J., Krishnamurthy, V., Hennessy, W., and Michon, G., "Silicon Carbide MOSFET Integrated Circuit Technology," *Physica Status Solidi (a)* 162(1), 459, 1997.
167. Ryu, S.H., Kornegay, K.T., Cooper, J.A., Jr., and Melloch, M.R., "Digital CMOS ICs in 6H-SiC Operating on a 5 V Power Supply," *IEEE Transactions on Electron Devices* 45(1), 45, 1998.
168. Diogu, K.K., Harris, G.L., Mahajan, A., Adesida, I., Moeller, D.F., and Bertram, R.A., "Fabrication and Characterization of a 83 MHz High-Temperature β-SiC MESFET Operational Amplifier With an AlN Isolation Layer on (100) 6H-SiC," in *54th Annual IEEE Device Research Conference* IEEE, Santa Barbara, CA, 1996, p. 160.
169. Harris, G.L., Wongchotigul, K., Henry, H., Diogu, K., Taylor, C., and Spencer, M.G., "Beta SiC Schottky Diode FET Inverters Grown on Silicon," in Silicon Carbide and Related Materials: Proceedings of the Fifth International Conference, *Institute of Physics Conference Series*, Eds. Spencer, M.G., Devaty, R.P., Edmond, J.A., Kahn, M.A., Kaplan, R., and Rahman, M., IOP Publishing, Bristol, United Kingdom, 1994, p. 715.
170. Neudeck, P.G., Beheim, G.M., and Salupo, C.S., "600 C Logic Gates Using Silicon Carbide JFET's," in *Government Microcircuit Applications Conference Technical Digest*, March 20–23, 2000, Anaheim, CA, p. 421.
171. Pierret, R.F., *Semiconductor Fundamentals*, Addison-Wesley, Reading, MA, 1983.
172. Cooper, J.A., Jr. and Agarwal, A., "SiC Power-Switching Devices—The Second Electronics Revolution?," *Proceedings of the IEEE* 90(6), 956, 2002.
173. Sochacki, M., Lukasiewicz, R., Rzodkiewicz, W., Werbowy, A., Szmidt, J., and Staryga, E., "Silicon Dioxide and Silicon Nitride as a Passivation and Edge Termination for 4H-SiC Schottky Diodes," *Diamond and Related Materials* 14(3–7), 1138, 2005.
174. Chang, S.-C., Wang, S.-J., Uang, K.-M., and Liou, B.-W., "Design and Fabrication of High Breakdown Voltage 4H-SiC Schottky Barrier Diodes With Floating Metal Ring Edge Terminations," *Solid-State Electronics* 49(3), 437, 2005.
175. Hu, S. and Sheng, K., "A New Edge Termination Technique for SiC Power Devices," *Solid-State Electronics* 48(10–11), 1861, 2004.
176. Beck, A.L., Yang, B., Guo, X., and Campbell, J.C., "Edge Breakdown in 4H-SiC Avalanche Photodiodes," *IEEE Journal of Quantum Electronics* 40(3), 321, 2004.
177. Ayalew, T., Gehring, A., Grasser, T., and Selberherr, S., "Enhancement of Breakdown Voltage for Ni-SiC Schottky Diodes Utilizing Field Plate Edge Termination," *Microelectronics Reliability* 44(9–11), 1473, 2004.

178. Nigam, S., Kim, J., Luo, B., Ren, F., Chung, G.Y., Pearton, S.J., Williams, J.R., Shenai, K., and Neudeck, P., "Influence of Edge Termination Geometry On Performance of 4H-SiC p-i-n Rectifiers," *Solid-State Electronics* 47(1), 61, 2003.
179. Tarplee, M.C., Madangarli, V.P., Zhang, Q., and Sudarshan, T.S., "Design Rules for Field Plate Edge Termination in SiC Schottky Diodes," *IEEE Transactions on Electron Devices* 48(12), 2659, 2001.
180. Chow, T.P., "SiC Bipolar Power Devices," *MRS Bulletin* 30(4), 299, 2005.
181. Sugawara, Y., "High Voltage SiC Devices," in *Silicon Carbide: Recent Major Advances*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer, Berlin, 2003, p. 769.
182. Rupp, R., Treu, M., Mauder, A., Griebl, E., Werner, W., Bartsch, W., and Stephani, D., "Performance and Reliability Issues of SiC-Schottky Diodes," in Silicon Carbide and Related Materials 1999, *Materials Science Forum*, vols. 338–342, Eds. Carter, C.H., Jr., Devaty, R.P., and Rohrer, G.S., Trans Tech Publications, Switzerland, 2000, p. 1167.
183. Polyakov, A.Y., Li, Q., Huh, S.W., Skowronski, M., Lopatiuk, O., Chernyak, L., and Sanchez, E., "Minority carrier diffusion length measurements in 6H-SiC," *Journal of Applied Physics* 97(5), 053703, 2005.
184. Lendenmann, H., Bergman, J.P., Dahlquist, F., and Hallin, C., "Degradation in SiC Bipolar Devices: Sources and Consequences of Electrically Active Dislocations in SiC," in Silicon Carbide and Related Materials—2002, *Materials Science Forum*, vols. 433–436, Eds. Bergman, P. and Janzen, E., Trans Tech Publications, Switzerland, 2003, p. 901.
185. Schoen, K.J., Henning, J.P., Woodall, J.M., Cooper, J.A., Jr., and Melloch, M.R., "A Dual-Metal-Trench Schottky Pinch-Rectifier in 4H-SiC," *IEEE Electron Device Letters* 19(4), 97, 1998.
186. Chow, T.P., Ramungul, N., Fedison, J., and Tang, Y., "SiC Power Bipolar Transistors and Thyristors," in *Silicon Carbide: Recent Major Advances*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer, Berlin, 2003, p. 737.
187. Zhao, J.H., "Silicon Carbide Power Field-Effect Transistors," *MRS Bulletin* 30(4), 293, 2005.
188. Friedrichs, P., "Charge Controlled Silicon Carbide Switching Devices," in Silicon Carbide 2004—Materials, Processing and Devices, *Materials Research Society Symposium Proceedings*, vol. 815, Eds. Dudley, M., Gouma, P., Kimoto, T., Neudeck, P.G., and Saddow, S.E., Materials Research Society, Warrendale, PA, 2004, p. 255.
189. Levinshtein, M.E., Ivanov, P.A., Agarwal, A.K., and Palmour, J.W., "Optical Switch-On Of Silicon Carbide Thyristor," *Electronics Letters* 38(12), 592, 2002.
190. Mehregany, M., Zorman, C., Narayanan, N., and Wu, C.H., "Silicon Carbide MEMS for Harsh Environments," *Proceedings of the IEEE* 14(8), 1998.
191. Epstein, A.H., "Millimeter-Scale, Micro-ElectroMechanical Systems Gas Turbine Engines," *ASME Journal of Engineering for Gas Turbines and Power* 126, 205, 2004.
192. FLX Micro, http://www.flxmicro.com.
193. Masheeb, F., Stefanescu, S., Ned, A.A., Kurtz, A.D., and Beheim, G., "Leadless Sensor Packaging For High-Temperature Applications," in *The Fifteenth IEEE International Conference on Micro Electro Mechanical Systems,* January 20–24, 2002, Las Vegas, NV, IEEE, Piscataway, NJ, 2002, p. 392.
194. Hunter, G.W., Neudeck, P.G., Xu, J., Lukco, D., Trunek, A., Artale, M., Lampard, P., Androjna, D., Makel, D., and Ward, B., "Development of SiC-Based Gas Sensors for Aerospace Applications," in Silicon Carbide 2004—Materials, Processing and Devices, *Materials Research Society Symposium Proceedings*, vol. 815, Eds. Dudley, M., Gouma, P., Kimoto, T., Neudeck, P.G., and Saddow, S.E., Materials Research Society, Warrendale, PA, 2004, p. 287.
195. Spetz, A.L. and Savage, S., "Advances in SiC Field Effect Gas Sensors," in *Silicon Carbide: Recent Major Advances*, Eds. Choyke, W.J., Matsunami, H., and Pensl, G., Springer, Berlin, 2003, p. 869.
196. Pensl, G., Morkoc, H., Monemar, B., and Janzen, E., *Silicon Carbide, III-Nitrides, and Related Materials*, Trans Tech Publications, Switzerland, 1998.
197. Harris, G.L., *Properties of SiC,* The Institute of Electrical Engineers, London, 1995.

198. Kemerley, R.T., Wallace, H.B., and Yoder, M.N., "Impact of Wide Bandgap Microwave Devices on DoD Systems," *Proceedings of the IEEE* 90(6), 1059, 2002.
199. Pearton, S.J., Zolper, J.C., Shul, R.J., and Ren, F., "GaN: Processing, defects, and devices," *Journal of Applied Physics* 86(1), 1, 1999.
200. Dudley, M., Gouma, P., Kimoto, T., Neudeck, P.G., and Saddow, S.E., Silicon Carbide 2004—Materials, Processing and Devices, *Materials Research Society Symposium Proceedings*, vol. 815, Materials Research Society, Warrendale, PA, 2004.