Single-Event Effect Performance of a Conductive-Bridge Memory EEPROM

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Abstract: *We investigated the heavy ion SEE characteristics of an EEPROM based on CBRAM technology. SEFI is the dominant type of SEE for each operating mode (standby, read-only, write/read). We also observed single bit upsets in the CBRAM cell, during write/read tests. the SEU LET threshold is between 10 and 20 MeV·cm²/mg, with an upper fluence limit of 3 × 10⁶ cm⁻² at 10 MeV·cm²/mg. In the standby mode, the CBRAM array appears immune to bit upsets.*

INTRODUCTION

Conductive-bridge random access memory (CBRAM) is a programmable metallization cell (PMC) memory in the family of resistive memories [1]−[4]. The scaling limitations of flash spurred the introduction of alternative non-volatile memory technologies. The CBRAM has shown advantages in performance and scalability relative to other alternative non-volatile memory technologies [2]. Additionally, the resistive elements can be fabricated back-end-of-line (BEOL) on CMOS processes [1]. Therefore, it can be more easily integrated into existing CMOS wafer fabrication lines. The rapid development in resistive memories has expedited the release of commercial-ready products. The CBRAM from Adesto Technologies is an electrically erasable programmable read-only memory (EEPROM) [1], [4]−[5].

The CBRAM offers a promising alternative to traditional charge-trap or floating-gate technologies for space applications, due to its intrinsic radiation tolerance. Previous studies found that the Adesto CBRAM EEPROM is error free up to 450 krad(GeS_2) of gamma rays, and up to 3 Mrad(CaF_2) of 10 keV x-rays [13]−[14]. The device is also hardened against displacement damage up to 10^{14} n/cm² of 1 MeV equivalent neutrons [14]. Other studies suggest that single-event upset (SEU) at the cell level can occur, due to upset of the access transistor [16]−[17]. We previously investigated the SEE performance of a microcontroller with embedded reduction-oxidation memory [15]. There is yet to be a comprehensive SEE evaluation of a stand-alone resistive memory product. Here, we investigate the SEE susceptibility of a commercial EEPROM, the first stand-alone memory based on CBRAM technology.

EXPERIMENTAL

Figure 1. Photograph of the test setup inside the LBNL irradiation chamber.

Tester: ARM Cortex-M4-based 32-bit microcontroller operating at 96 MHz with 64kB RAM and 256kB flash memory. Figure 1 shows a photograph of the test board mounted onto a metal plate inside the irradiation chamber. The test samples were acid-etched to expose the die surface.

Data pattern:
- 00, FF, AA, 55

Test mode:
- Static on (standby)
- Random read
- Sequential read
- Random write
- Page write

IRRADIATION DETAILS

We irradiated four parts in vacuum at the Lawrence Berkeley National Laboratory (LBNL) Berkeley Accelerator Space Effects (BASE) Facility with a cocktail of 16 MeV/amu heavy ions. Table I shows the heavy ion beam information, including the ion specie, energy, linear energy transfer (LET), and range.

We also carried out pulsed laser testing at the Naval Research Laboratory with a 590 nm single photon dye laser.

Table I.
Heavy ion characteristics.

Ion	Total Energy (MeV)	LET (MeV·cm²/mg)	Range in Si (μm)
Ne	253	3.1	225
Ar	642	7.3	256
Kr	1225	25.0	165
Xe	1955	49.3	148

DEVICE DETAILS

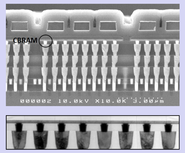

Figure 2. TEM image (*image courtesy of Adesto*).

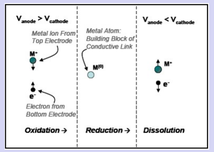

Figure 3. Working principles of the CBRAM technology.

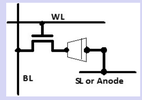

Figure 4. 1T1R implementation of the CBRAM. Program: WL and SL are biased High. BL pulses High to Low. Erase: WL is High. SL is Low. BL pulses Low to High.

The RM24C from Adesto Technologies is the industry's first stand-alone EEPROM built with CBRAM technology [1], [4]−[5]. The EEPROM is available in 32, 64 or 128 Kb. Figure 3 shows a schematic diagram illustrating the physical mechanism of the CBRAM. Figure 4 shows a schematic diagram of the one-transistor-one-resistor (1T1R) architecture of a CBRAM cell. To program a cell, the Word Line (WL) and the anode or Select Line (SL) is High. The Bit Line (BL) pulses High to Low, which forward biases the CBRAM. To erase a cell, the WL is high, and the SL is low. The BL pulses Low to High, which reverse biases the CBRAM.

SINGLE EVENT UPSET

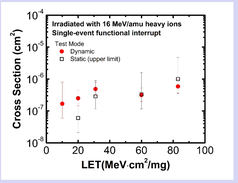

Figure 5. SBU cross section per bit vs. effective LET for each ion specie. SBUs were only observed while the device is continuously exercised in write/read cycles.

SBU characteristics:
- LET_{th} between 10 and 20 MeV·cm²/mg
- Observed in Write/Read mode only; immune during static and read-only tests
- Consisted of 1 to 0 and 0 to 1 type errors; although 1 to 0 errors are theoretically more likely for these devices
- No angular dependence

Figure 5 shows the single-bit upset cross section as a function of LET for each ion specie. The relatively high error standard deviations are the result of the low count of the upsets. The SBUs were rare relative to SEUs that were characteristic of control circuit upsets. We filtered the errors which can be cleared by a second read (likely due to buffer upsets) and SEUs that cleared after power cycle (single-event transient (SEU) in the peripheral circuits).

SBU in the CBRAM cell is possible, consistent with previous studies on test structures [16], [17]. However there are key distinctions for the SBU observed here. For the standalone memory product here, the most vulnerable state for the access transistor is during erase rather than program. The transistors with reverse biased drain are located in the same row as the target cell to be erased. As a result, a SEU from the access transistor will likely change a cell from a low resistive state to a high resistive state. Errors of the opposite polarity will be less likely. However, the fact that we see errors of both polarities raise questions about the origin of the SEUs. It is possible that some of these SEUs are due to unidentified buffer upsets. A larger sample size is needed to investigate the SEU characteristics further. Nonetheless, the results show that ion-induced cell corruption will not be the primary concern for space applications

SINGLE EVENT FUNCTIONAL INTERRUPT

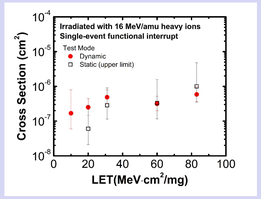

Figure 6. SEFI cross section vs. effective LET for parts irradiated while continuously exercised or statically biased. The cross sections for statically biased case represent upper fluence limits.

Table II
SEFI characteristics.

Test Mode	Recovery method	Data Loss?	Characteristics
Dynamic	Cleared on next read	No	1) address counter offset by 1 byte throughout read in one case 2) random and FF errors in other cases
Static and Dynamic	Power cycle	No	1) mass errors that read all 00 or FF 2) a stuck address error 3) a stuck bit error.
Static and Dynamic	Rewrite	Yes	1) mass errors that read all 00, FF, or random values. 2) errors changed values following power cycle to FF in one case, and to random values in another case.

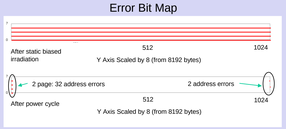

Figure 7. (top) Error bit map following static exposure. (bottom) Error bit map after a power cycle. The addresses are scaled by a factor of 8. Cells were originally programmed to repeating AA pattern prior to irradiation. The SEFI caused the entire memory to read FF. A power cycle cleared most of the errors, except for two pages (34 addresses) and two other address errors.

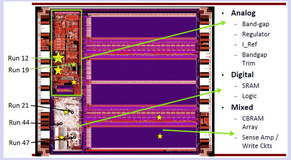

Figure 8. Die map of a first generation device, showing sensitive locations during pulsed-laser testing. The upset areas are indicated by circles and the respective run number. *(Image courtesy of Adesto).*

Figure 6 shows the SEFI cross section vs. effective LET for static and dynamic test modes. Table II categorizes the SEFIs. A potentially dangerous SEFI occurred during static irradiation and resulted in data loss. Figure 7 shows an example of such an event. The memory was programmed with a repeating AA pattern. After the irradiation, all of the memory space read FF (top). A power cycle cleared most of the errors, except for two pages and two SEUs (bottom). These errors signify data corruption during the beam exposure or during read-back. These errors could only be cleared by rewriting the cells. This type of SEFI often produce errors in an entire page or several consecutive pages. Furthermore, in some cases, the supply current showed spikes up to approximately 2 – 3 mA during irradiation, possibly indicating signal contention [18].

We used pulsed-laser testing to determine the origin of the SEFIs. Figure 8 shows a die map with sensitive areas. We determined that SEFI can be triggered from strikes on the Bandgap Reference circuits, Static Random Access Memory (SRAM), and logic circuits. Strikes on the sense amplifier circuits did not lead to upsets, contrary to a previous investigation on another resistive memory device [15]. The metallization overlayers and the residue on the surface of the die likely obstructed the pulsed laser from fully penetrating these sensitive regions. Nonetheless, the pulsed-laser test showed that the CBRAM array is relatively robust against ionizing radiation-induced upsets.

CONCLUSION

The CBRAM appears to be hardened against heavy ion-induced bit upset when powered off or in standby mode, unlike floating-gate or trap-charge flash and EEPROMs. The SEFI response is similar to existing EEPROM and flash technologies, with error modes that include page errors, mass memory errors, device hang-ups, etc. However, unlike modern flash devices, the CBRAM show similar SEFI sensitivity for program, erase, and read operations, owing to the similarity in the electrical conditions. Another key distinction in the SEE response of the CBRAM is the reduced sensitivity to destructive SEE during write/erase operations. The vulnerability to SEDR is reduced significantly, since the CBRAM does not require charge pumps for high voltages program/erase operations. Also, the fact that the CBRAM is fabricated BEOL on a standard CMOS process suggests it could be developed into a space-grade product. The manufacturer or other appropriate military/space chip manufacturers can potentially transfer the CBRAM technology onto a radiation-hardened platform without a complete redesign of the fabrication process. This distinction offers another advantage for the CBRAM's potential utilization for space missions.

The memory architecture for a high density CBRAM device will likely differ significantly than the device studied here. As the technology progresses, the size of the CBRAM stack will shrink and the cell-to-cell noise margin will decrease, both aspects could impact the radiation tolerance.

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