

Recent Radiation Test Results for Power MOSFETs

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Abstract—Single-event effect (SEE) and total ionizing dose (TID) test results are presented for various hardened and commercial power metal-oxide-semiconductor field effect transistors (MOSFETs), including vertical planar, trench, superjunction, and lateral process designs.

I. INTRODUCTION

POWER MOSFETs continue to be used ubiquitously in spacecraft. Several topologies are available. Planar, vertical double-diffused MOSFET (VDMOS) structures (Fig. 1A) have long dominated the radiation-hardened offerings, and the number of manufacturers providing hardened VDMOS has recently expanded. Commercially, vertical trench-gate style MOSFETs (Fig. 1B) have been a staple for low- to medium-voltage applications due to their lower on-state resistance (R_{DS_ON}). The vertically-oriented gates penetrate past the body region thereby eliminating the parasitic junction field effect transistor (JFET) that limits the minimum cell pitch in planar VDMOS. For higher-voltage power MOSFETs, a lower R_{DS_ON} has been achieved through development of the superjunction structure (Fig. 1C). Superjunction power MOSFETs (SJ MOSFETs) have charge-compensating columns within the epilayer that permit a shallower drift region for a given breakdown voltage (BV_{DSS}). Radiation-hardened SJ MOSFETs have just become available in the past year and hardened trench-style MOSFETs are in development. Use of point-of-load (POL) converters for space applications is driving interest in lateral double-diffused MOSFETs (LDMOS) [1] (Fig. 1D) that can be integrated into a monolithic POL design. Finally, an integrable commercial lateral-vertical hybrid design [2] offers increased current

density over the standard LDMOS and improved frequency response over trench-style MOSFETs.

Power MOSFETs, regardless of structure, are susceptible to radiation damage from total ionizing dose (TID) and single-event effects (SEEs), including single-event gate rupture (SEGR) and single-event burnout (SEB). This work presents test data for power MOSFETs of different structures and manufacturers, all evaluated in the past year for potential insertion into space flight missions. Table I provides a list of devices tested. We include SEE test data for two new manufacturers of radiation-hardened VDMOS, Aeroflex Corp. and Solid State Devices, Inc. (SSDI), as well as data for Fuji's 500 V radiation-hardened VDMOS. A Vishay commercial trenchFET[®] reported on previously [3] is further evaluated. We also present both SEE and TID data for Infineon Technologies' radiation-hardened SJ MOSFET and a preliminary look at the SEE response of engineering samples of several LDMOS structures from a commercial fabrication process. SEE data on a Texas Instruments commercial NexFET[™] lateral-vertical hybrid power MOSFET can be found in [4].

II. EXPERIMENTAL METHODS

A. Heavy-Ion Testing for SEEs

We gathered heavy-ion test data at the Texas A&M University Cyclotron Facility (TAMU) or at Lawrence Berkeley National Laboratory (LBNL) (Table II). Fig. 2 shows a diagram of the irradiation test circuit. Six devices-under-test (DUTs) can be mounted on the test board with daughter cards and individually accessed via dry Reed relays controlled by an Agilent 34907A data acquisition/switch unit. All terminals of the devices not under test are then floating. Samples were delidded or decapsulated and fully electrically characterized at NASA Goddard Space Flight Center (GSFC). On-site, prior to the first and following each irradiation run, a gate stress test was performed in which the gate leakage current (I_{GSS}) was measured as a function of gate voltage at 0 drain-source (V_{DS}) bias, and the drain-source breakdown voltage (BV_{DSS}) was measured. Measurement equipment included a Keithley 2400 current-voltage sourcing and measurement instrument (SMU) for gate voltage supply and current measurement (< 1 nA accuracy) and either a Keithley

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2400 or 2410 SMU for the drain voltage supply and drain current measurement.

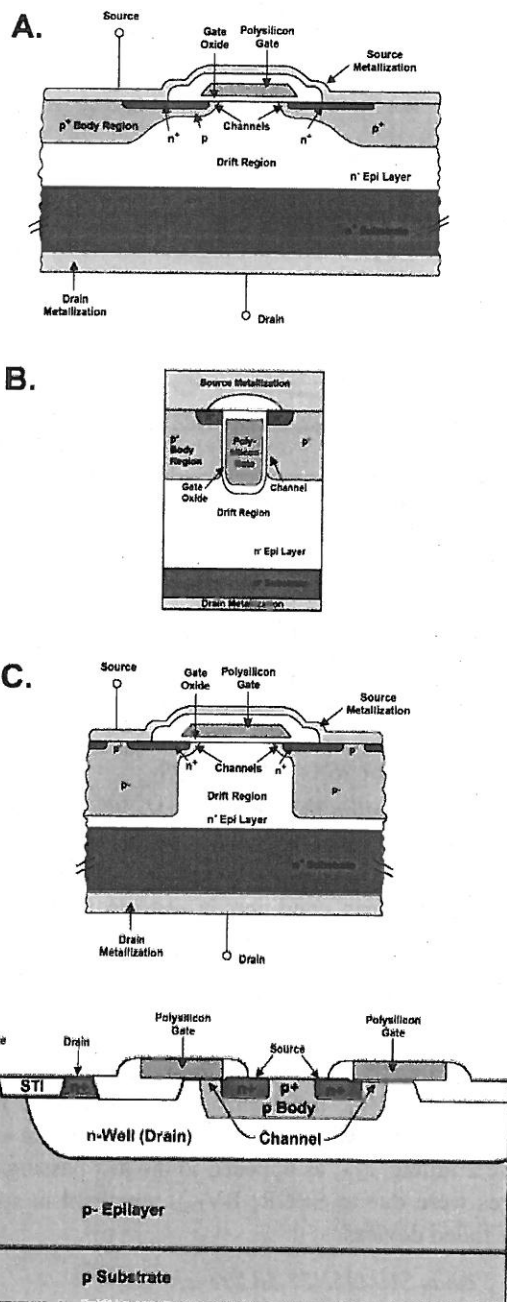


Fig. 1. Illustration of cross sections of n-type power MOSFETs. A. VDMOS; B. trench-gate; C. superjunction; D. LDMOS.

Table I. Summary of Power MOSFETs Tested

Part #	Manufacturer	Technology*	BV _{DSS} (V)	I _D (A)	R _{DS_ON} (Ω)
RAD7264NCx	Aeroflex	RH VDMOS	250	45	0.05
SFR130S.5	SSDI	RH VDMOS	100	30	0.025
JAXA-R-2SK4188	Fuji	RH VDMOS	500	23	0.18
SUM45N25-58	Vishay	Com Trench	250	45	0.058
BUY25CS54A	Infineon	RH SJ	250	54	0.03
Eng. Samples	Vendor A	Com LDMOS	40	--	--

*RH = Radiation hardened; Com = Commercial

Samples were irradiated in air at TAMU or in vacuum at

LBNL at normal incidence unless otherwise indicated. For each sample, the gate-source bias (V_{GS}) was held in the off state and V_{DS} was incremented in steps. At each step, the sample was irradiated with a beam flux indicated in Table II until either the sample failed or the maximum run fluence was reached. A post-irradiation gate stress (PIGS) test was then performed to reveal any latent damage to the gate oxide and the BV_{DSS} recorded. Failure was defined by a sudden increase in drain-source leakage current during the run or the gate leakage current exceeding the vendor specification during the run or following the PIGS test.

B. Total Ionizing Dose Testing

⁶⁰Co TID tests were performed at NASA GSFC's Radiation Effects Facility (REF). Samples were irradiated under one of three different bias conditions: on-state, in which the drain and source were grounded and the gate biased to 60% of maximum on-state bias; off-state, in which the gate and source were grounded and the drain biased at 75% of the rated BV_{DSS}; and grounded, in which all nodes were grounded. Additional unirradiated samples were measured between dose steps as controls. Irradiation was performed under high dose rate (HDR) conditions, which was lowered during overnight irradiation periods. Irradiated samples underwent a one-week biased anneal at room temperature, followed by a HDR irradiation of an additional 50% of the total dose received and then immediately by a one week biased anneal at 100 °C.

Table II. SEE Test Conditions

Part #	Facility	Tune, Species	Flux (#/cm ² /s)	Fluence (#/cm ²)
RAD7264NCx	TAMU	15 MeV/u Ag, Xe	1x10 ⁴	5x10 ⁵
SFR130S.5	LBNL	10 MeV/u Ar, Kr	1x10 ⁴	5x10 ⁵
JAXA R-2SK4188	TAMU	15 MeV/u Ag	1x10 ⁴	5x10 ⁵
SUM45N25-58	LBNL	10 MeV/u Ag	10 – 5x10 ³	5x10 ³ – 3x10 ⁵
BUY25CS54A	TAMU	15 MeV/u Kr, Xe, Au	1x10 ⁴	5x10 ⁵
Eng. Samples	LBNL, TAMU	10 MeV/u Xe; 15 MeV/u Ag	1x10 ⁴ – 1x10 ⁵	1x10 ⁶ – 1x10 ⁷

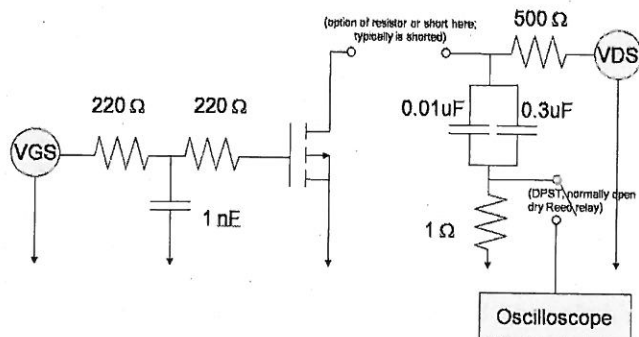


Fig. 2. Diagram of irradiation test circuit. DPST = double-pole, single-throw switch.

III. RESULTS: SEE TESTING

Plots are provided showing the SEE response curves for the devices tested. Data points indicate the maximum V_{DS} for which all samples passed under a given V_{GS} bias, with error bars extending to the V_{DS} at which the first failure occurred.

A. Aeroflex RAD7264NCx VDMOS

Aeroflex Corporation recently introduced a line of radiation hardened planar vertical power MOSFETs, which includes the 250 V, 45 A, 50 m Ω RAD7264. Samples were provided by Aeroflex in TO-3 cans. Fig. 3 shows SEE response curves for 1348 MeV Ag (LET = 42 MeV-cm²/mg, range = 125 μ m) and 1512 MeV Xe (LET = 52 MeV-cm²/mg, range = 120 μ m). For each ion species and V_{GS} condition, 3 samples were irradiated. All failures were due to SEGR; BV_{DSS} remained unchanged in the failed devices.

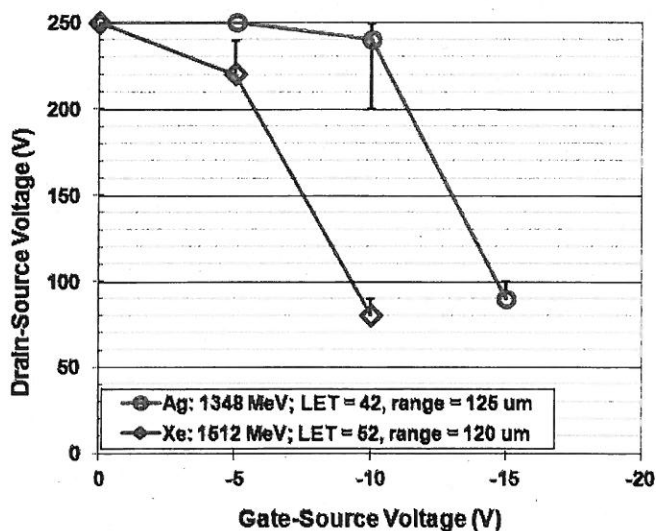


Fig. 3. SEE response curves for the RAD7264NCx VDMOS. Data points are the last passing bias condition, with error bars extending to the first failing V_{DS} .

B. SSDI SFR130S.5 VDMOS

Solid State Devices, Inc. (SSDI) also recently introduced a line of radiation hardened planar vertical power MOSFETs, which includes the 100 V, 30 A, 25 m Ω SFR130. Samples were provided by SSDI in surface-mount device (SMD) 0.5 packages. Fig. 4 shows SEE response curves for 400 MeV Ar (LET = 9.7 MeV-cm²/mg, range = 130 μ m) and 886 MeV Kr (LET = 31 MeV-cm²/mg, range = 113 μ m). For each ion species and V_{GS} condition, 3 samples were irradiated. All failures were due to SEB. To confirm this failure mechanism, protective mode testing under Kr irradiation was performed wherein a 100 k Ω or 1 M Ω resistor was placed in series with the drain node. Under this protected condition, large transients occurred but DUTs remained undamaged even at the full 100 V_{DS} rating under maximum -20 V_{GS} bias. It appears, therefore, that this device may be robust to SEGR. Under this maximum bias condition, the SEB cross section was found to be 2.55×10^{-2} cm². Finally, the angular response of this device was determined by positioning the DUT off-normal from the incident beam path and, under the known failing condition of

0 V_{GS} and 45 V_{DS} but in protected mode (100 k Ω drain resistance), incrementally reducing the tilt angle until non-destructive SEB occurred. For 886 MeV Kr, the DUT passed at a tilt angle of 25°, failing at 20°.

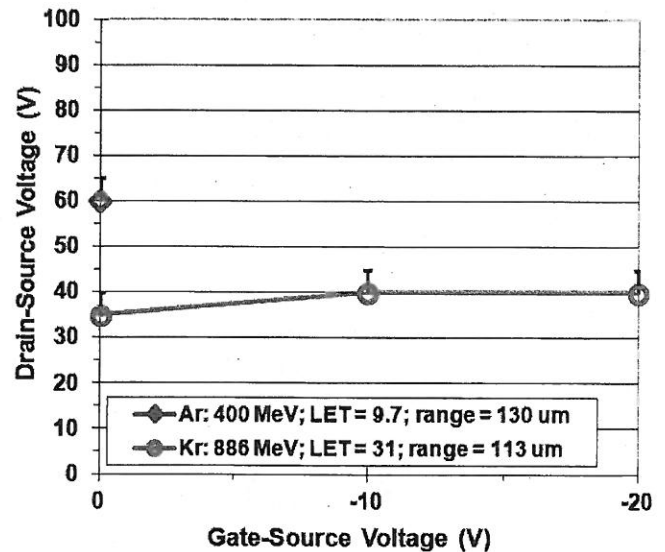


Fig. 4. SEE response curves for the SFR130S.5 VDMOS. Data points are the last passing bias condition, with error bars extending to the first failing V_{DS} .

C. Fuji JAXA R 2SK4188 VDMOS

The Fuji radiation-hardened 500 V, 23 A, 180 m Ω planar VDMOS, part number JAXA-R-2SK4188, was evaluated for potential use in a low V_{DS} , -13 V_{GS} off-state bias application. Note that this bias condition is outside the manufacturer's recommended off-state gate bias with regards to radiation hardness assurance. Samples were provided by Fuji in SMD-2 packages. Fig. 5 shows the SEE response curve for 1289 MeV Ag (LET = 42 MeV-cm²/mg, range = 119 μ m). Three samples were irradiated at -13 V_{GS} and the remaining 2 samples were evaluated at 0 V_{GS}; unfortunately, the threshold failure V_{DS} condition at 0 V_{GS} was not found, so in Fig. 6 data at 0 V_{GS} are for the 2 failing V_{DS} , as opposed to the last passing biases. All failures were due to SEGR; BV_{DSS} remained in specification in the failed devices.

D. Vishay SUM45N25-58 TrenchFET®

Initial SEE test results of the Vishay commercial 250 V, 45 A, 58 m Ω trench-gate style MOSFET have been previously reported by the authors for the 0 V_{GS} bias condition [3]. Fig. 6 presents these previous data as well as new data for non-zero V_{GS} biases. Three samples each were evaluated at 0 and -5 V_{GS}, and 2 samples at -10 V_{GS}. The primary failure mode is likely SEB due to the lack of dependence of the threshold failure V_{DS} on V_{GS}, although in each case the gate was also damaged.

Evaluation of the SEE response at negative gate biases required very low flux to avoid premature failure due to localized total dose effects which caused the drain current to rise during irradiation. In trench-style devices, the orientation of the gate oxide is perpendicular to the surface of the die, increasing the cross-section of vulnerability for a single ion to

traverse from source to drain within the oxide. As the ion passes through the oxide, it generates trapped holes along its path, leading to a sudden rise in drain leakage current due to the lowering of the gate threshold voltage at that location within the transistor. This effect has been studied in the literature [5]. Lowering the flux during these tests permitted charge dissipation between ion strikes, reducing the magnitude of the dose-induced drain leakage current.

E. Infineon BUY25CS54A SJ MOSFET

Infineon Technologies, A.G., introduced the first radiation-hardened superjunction power MOSFETs this past year. Samples of the 250 V, 54 A, 30 mΩ BUY25CS54 were provided by Infineon in SMD-2 packages. Fig. 7 shows SEE response curves for 1289 MeV Ag (LET = 42 MeV-cm²/mg, range = 119 μm), 1512 MeV Xe (LET = 52 MeV-cm²/mg, range = 119 μm), and 2247 MeV Au (LET = 85 MeV-cm²/mg, range = 118 μm). For Ag and Xe tests, 3 samples each were irradiated up to -15 V_{GS}. For Au tests, 1 sample was incremented through all V_{GS} bias conditions, and a total of 5 samples were irradiated at -10 V_{GS} and -15 V_{GS}. Failures were due to SEGR; BV_{DSS} remained unchanged in these devices.

The range in silicon of Au ions at the Bragg peak is 51 μm. Fig. 8 shows the effect of varying the position of the Bragg peak in the device on the threshold V_{DS} for SEGR. For these tests, V_{GS} was held at -15 V. Due to the small sample size, data for all DUTs are shown. A small effect can be seen, with the worst-case position of the Bragg peak being between 42 μm and 58 μm below the surface of the DUT.

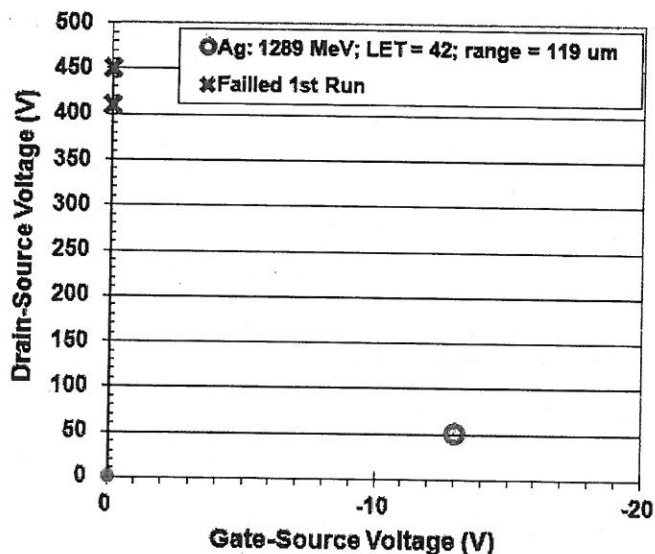


Fig. 5. SEE response of JAXA R 2SK4188 VDMOS. At 0 V_{GS}, the threshold bias for failure was not found; data points therefore show the V_{DS} at which failure occurred. Data at -13 V_{GS} are last passing V_{DS}; error bar is smaller than symbol and reflects a 10 V increment to failure.

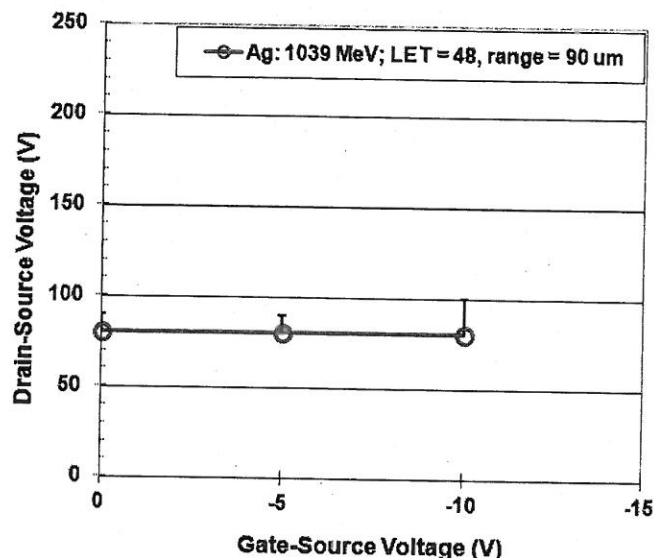


Fig. 6. SEE response of SUM45N25-58 trench MOSFET. Data points are the last passing bias condition, with error bars extending to the first failing V_{DS}.

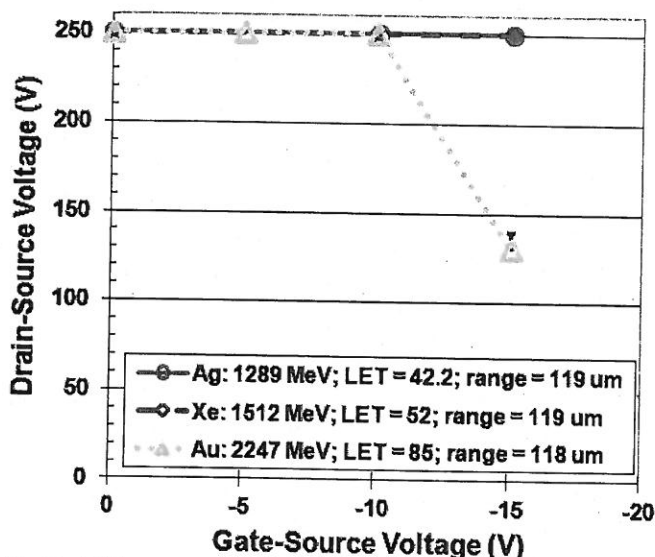


Fig. 7. SEE response curves for the BUY25CS54A SJ MOSFET. Data points are the last passing bias condition, with error bars extending to the first failing V_{DS}.

F. Commercial LDMOS

Engineering samples of a commercial 40 V LDMOS varying in geometry were provided for SEE evaluation. Tests were conducted at TAMU under 1170 MeV Ag irradiation (LET = 44 MeV-cm²/mg, range = 107 μm) on samples having a 2.2 μm drift length (Fig. 1D). At 0 V_{GS}, failure due to SEB occurred at 20 V_{DS} – 22 V_{DS}, with 3 samples passing at 18 V_{DS}. Additional samples were tested at 15° and 30° tilt angles, as well as at 45° tilt and both 0° and 90° roll angles; all samples had the same failure threshold as those irradiated at normal incidence. Upon failure, electrical connection to the MOSFET drain was lost (bond wires were intact), indicating that the metal interconnect had been damaged. PIGS tests

demonstrated either normal or slightly elevated gate leakage current (I_{GSS}).

Tests at LBNL with 1232 MeV Xe (LET = 59 MeV-cm²/mg, range = 90 μ m) revealed less failure susceptibility with shorter drift lengths (1.6 μ m and 0.6 μ m), but the TAMU tests with Ag of the 2.2 μ m vs. 0.6 μ m drift lengths did not support this finding. Further evaluation of these devices will be conducted to establish trends and angular responses as a function of drift length.

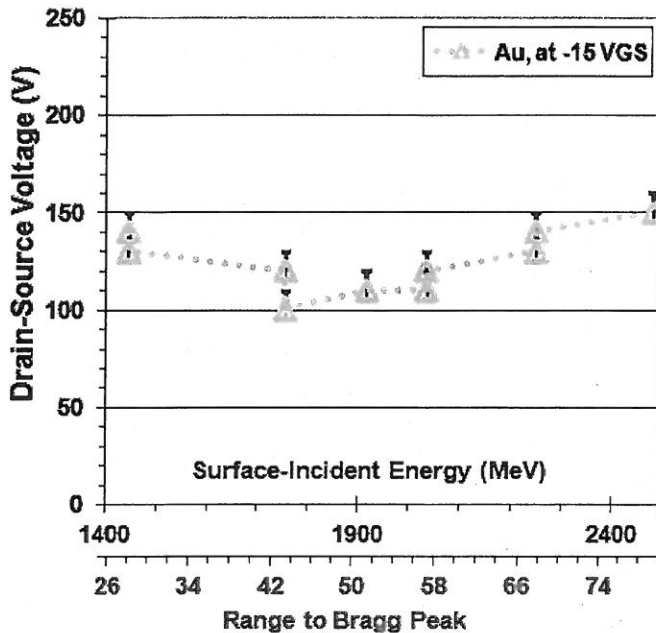


Fig. 8. Effect of Au energy (range to Bragg peak in μ m) on threshold V_{DS} for SEGR. Data for all DUTs shown.

IV. RESULTS: TID TESTING

For completeness, TID test results are included in this work for the Infineon Technologies 250 V SJ power MOSFET. Results on the Vishay 250 V SUM45N25-58 were reported previously [6]. TID evaluations of the SSDI power MOSFET are underway; data will be reported in [7].

A. Infineon BUY25CS54A SJ MOSFET

Samples of the BUY25CS54 were provided by Infineon in SMD-2 packages. The dose rate was approximately 950 rad(Si)/min, with lower rates of 26.4 rad(Si)/min and 98.5 rad(Si)/min during two overnight irradiation steps (125 krad(Si) to 150 krad(Si) and 300 krad(Si) to 400 krad(Si), respectively). Bias conditions were as described in section II.B. Key results are shown in Figs. 9-10.

The worst-case bias condition at high total dose was the on-state bias. All measured parameters of the 5 samples irradiated under this condition stayed within datasheet specification up to 400 krad(Si). As shown in Fig. 9, the non-annealed gate threshold voltage ($V_{GS(th)}$) fell below datasheet specification between 400 krad(Si) and 500 krad(Si). $V_{GS(th)}$ returned to within specification during a 168-hr room-temperature (RT) biased anneal that was performed following 500 krad(Si) total dose. All other static parameters remained within specification up to the maximum 500 krad(Si) ionizing dose exposure, with

some degradation of the drain leakage current (I_{DSS}) as shown in Fig. 10.

The 3 samples per condition irradiated either in the off-state or grounded state remained in specification for all measured parameters at the maximum 500 krad(Si) total accumulated dose, with some degradation of $V_{GS(th)}$ and I_{DSS} .

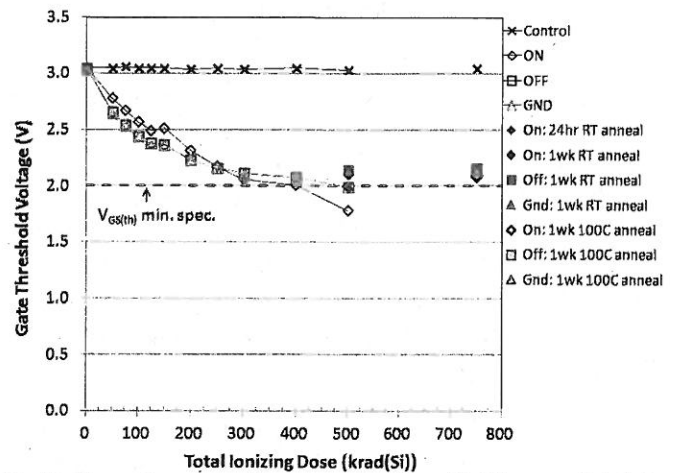


Fig. 9. Change in average $V_{GS(th)}$ as a function of total accumulated dose (open symbols) and annealing (filled symbols). Standard error bars are smaller than the data point symbols and are not shown.

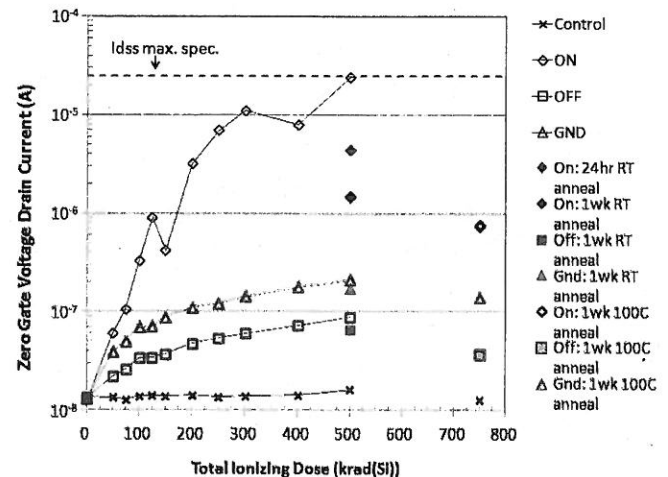


Fig. 10. Change in average I_{DSS} as a function of total accumulated dose (open symbols) and annealing (filled symbols). Standard error bars are smaller than the data point symbols and are not shown.

V. DISCUSSION AND CONCLUSIONS

Over the past few years, the viable options of power MOSFETs for space applications have increased, with new manufacturers of radiation-hardened devices emerging. In addition, goals have been completed or are under way to bring state-of-the-art topologies such as superjunction, trench, and lateral power MOSFETs into the aerospace market. This work provides initial radiation test data on some of the more recent offerings.

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