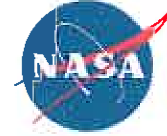
National Aeronautics and Space Administration



Hardness Assurance for Total Dose and Dose Rate Testing of a State-of-the-Art Off-Shore 32 nm SOI CMOS Processor

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CMOS = complementary metal oxide semiconductor
SOI = silicon on insulator

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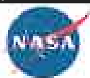

Acronyms

Acronym	Details	Page First Used
AMD	Advanced Micro Devices	3
ATE	Automated Test Equipment	3
CHMOS	Complementary High Performance Metal Oxide Semiconductor	13
CMOS	Complementary Metal Oxide Semiconductor	1
CPU	Central Processing Unit	8
DDR3	Double Date Rate 3	6
DUT	Device Under Test	3
ETW	Electronics Working Group	2
GPU	Graphic Processor Unit	8
GUI	Graphical Interface Unit	8
HKMGs	Hi-K Metal Gates	6
IC	Integrated Circuit	7
IR	Infrared	11
ITAR	International Traffic in Arms	4
LINAC	Linear Accelerator	9
NASA	National Aeronautics and Space Administration	1
NEPP	NASA Electronics Parts and Packaging Program	2
PCI	Peripheral Component Interconnect	6
PD-SOI	partially-depleted silicon-on-insulator	1
POR	Power on Reset	12
SEL	Single-Event Latchup	5
SOI	Silicon on Insulator	1
USB	Universal Serial Bus	8
VGA	Video Graphics Array	3
µPGA	Micro Pin Grid Array	6

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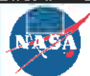
Outline

- Background and Motivation
- Device Under Test (DUT)
- Hardness Assurance Method(s)
- Total Dose Results
- Dose Rate Results
- Analysis
- Summary

Abstract: **Hardness assurance test results of a AMD 32 nm SOI CMOS processor for total dose and dose rate response are presented. Testing was performed using commercial motherboards and software stress applications versus more traditional automated test equipment (ATE).**

AMD = Advanced Micro Devices
CMOS = complementary metal oxide semiconductor
SOI = silicon on insulator



Background and Motivation

- There has been much discussion throughout the community regarding the International Traffic in Arms (ITAR) regulations as they pertain to radiation-induced device tolerance. This is a dual edged sword:
  - How to protect critical U.S. technologies from unfriendly hands, while at the same time,
  - Commercial semiconductor manufacturers fear inadvertently exceeding the ITAR radiation levels.
- The authors selected a representative off-shore foundry product to evaluate how this semiconductor process would fare against a subset of the ITAR criteria: total dose and dose rate limits.
- How the testing was performed is of note and discussion for the radiation effects community:
  - Instead of the traditional bias board/automated test equipment (ATE) combo, we utilized commercial processor motherboards as the tester/bias board and a suite of "stress" tests (software tests that stress the device and measure performance).

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Current ITAR Microelectronics Radiation Levels –

Excerpt from THE UNITED STATES MUNITIONS LIST -§ 121.1

- **(d) Radiation-hardened microelectronic circuits that meet or exceed all five of the following characteristics:**
  - **(1) A total dose of 5×10^5 rad(Si);**
  - **(2) A dose rate upset threshold of 5×10^8 rad(Si)/sec;**
  - **(3) A neutron dose of 1×10^{14} neutrons/cm^2 (1 MeV equivalent);**
  - **(4) A single event upset rate of 1×10^{-10} errors/bit-day or less, for the CREME96 geosynchronous orbit, Solar Minimum Environment;**
  - **(5) Single-event latchup (SEL) free and having a dose rate latch-up threshold of 5×10^8 rad(Si)/sec.**
- **This effort looked at (1), (2), and part of (5)**

The Device Under Test (DUT)

- **The DUT is a modern state-of the-art dual-core processor from Advanced Micro Devices (AMD)**
  - **Part number : AMD A4-Series AD3300OJHXBOX**
  - **Lot date code: DA 1153PGN**
  - **This is a 2.5 GHz dual-core processor**
    - Integrated floating point unit
    - Both level 1 and level 2 caches
    - Die size: 228 mm^2
    - Nominally a 65 Watt thermal design power
    - Package: 905-pin lidded micro-Pin Grid Array (µPGA) package
  - **The device utilizes the Llano processor core with on-chip peripherals including a dual-channel double date rate 3 (DDR3) memory controller, a Peripheral Component Interconnect (PCI) Express 2.0 controller and high definition graphics controller**

AMD A4-3300 series microprocessor

- **AMD is a fabless semiconductor manufacturer**
  - **This specific device is built on GLOBALFOUNDRIES' 32nm fab process located in Dresden, Germany**
  - **The process includes hi-K metal gates (HKMGs) on a partially-depleted silicon-on-insulator (PD-SOI) substrate**

AMD specs: http://www.cpu-world.com/CPUs/K10/AMD-A4-Series%20A4-3300%20AD3300OJZ22HX%20%28AD3300OJHXBOX%29.html

Radiation Test Method – Total Dose

- **Traditional Method**

Custom Bias Board – w/ integrated circuit (IC) sockets and connections to outside the chamber

Courtesy of Hewlett Packard

Automated Test Equipment (ATE) w/test vectors
Step irradiations using Bias Board followed by measurements w/ external ATE at specific intervals

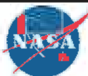
- **Method Utilized Here**

Commercial Biostar A55MLV Motherboard
(http://www.biostar.com.tw/app/en/mb/introduction.php?S_ID=569#dl)

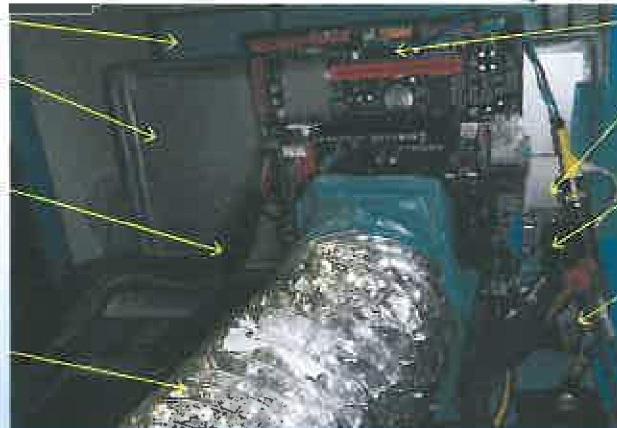
- **one copy used as bias board**
- **one copy used as "tester" running commercial "freeware" stress tester software**

Caveat:
Additional shielding surrounding the processor to minimize exposure levels to non-processor ICs

Sample radiographic film overlay on bias motherboard



Total Dose Test Setup



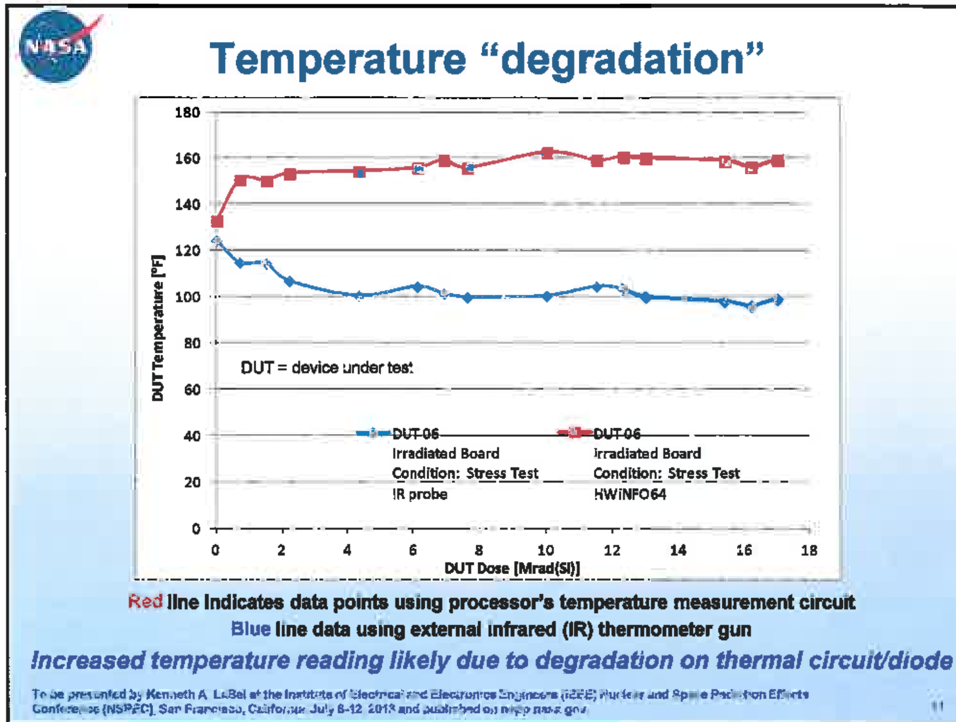
- **Stress software**
  1. **HWiNFO64 (http://www.hwinfo.com/). Collects and displays information about the hardware configuration. Part of that software function is the ability to monitor and log electrical / environmental data from the motherboard, Central Processing Unit (CPU), Graphics Processing Unit (GPU) and other sensors. This data is recorded for all tests.**
  2. **IntelBurnTest (http://www.techspot.com/downloads/4965-intelburntest.html). Provides a useful stress testing tool and benchmark. The program is a graphical interface unit (GUI) front-end for a compiled executable that performs math using the Linpack programming library. This tool burdens the CPU workload and enables the user to determine when/if there are flaws in the CPU's ability to perform operations. Inconsistencies due to radiation are recorded.**

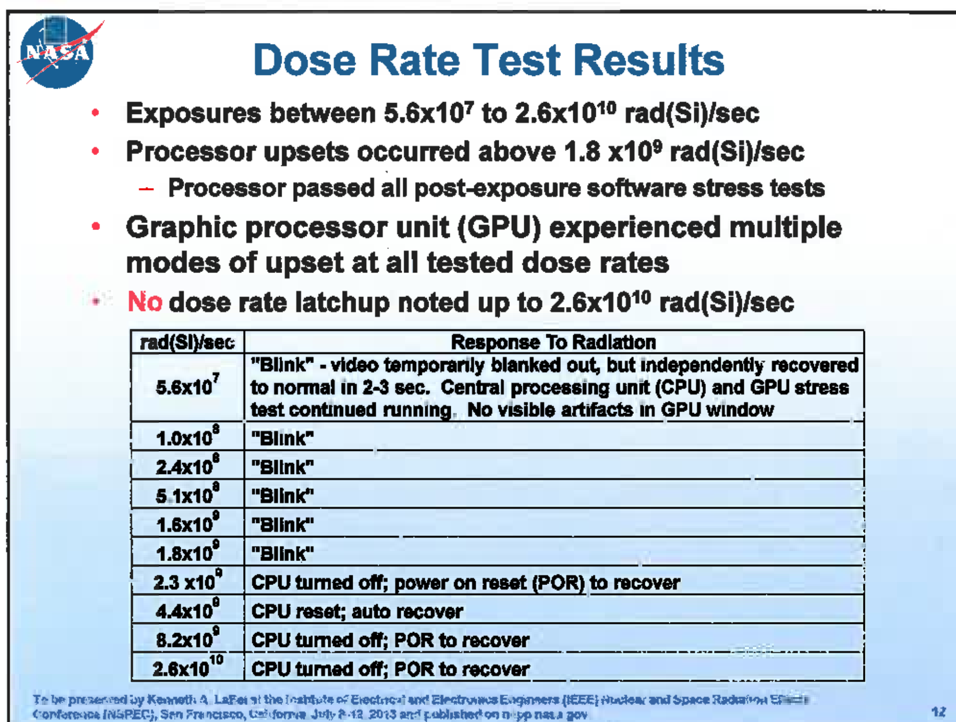
Dose Rate Test Method

- Performed at NAVSEA Crane using the linear accelerator (LINAC) in electron beam mode
- Exposures made while executing IntelBurn Test software on same motherboard as total dose tests. Full suite of stress tests run post-exposure.

Total Dose Results

- Bottom line up front:
  - 3 samples irradiated
  - NO processor failures observed at tested levels (1, 4 and 17 Mrad(Si), respectively). "17" is NOT a typo.
- *However,*
  - Bias motherboard (though all but the processor were heavily shielded) experienced failures/anomalies
    - Surprisingly, DDR3 memory modules failed (though they passed "performance" in a commercial TRIAD memory tester post-irradiation).
      - Varied by memory module with 1.1 krad(Si) being lowest failure level.
    - Fans degraded at ~ 4 krad(Si) – required motherboard swap
    - 1 motherboard failed @ 9.7 krad(Si) – entered a "biased, but unknown" state – required motherboard swap
  - Processor temperature "readings" degraded during all tests (see next chart)





rad(Si)/sec	Response To Radiation
5.6×10^{7}	"Blink" - video temporarily blanked out, but independently recovered to normal in 2-3 sec. Central processing unit (CPU) and GPU stress test continued running. No visible artifacts in GPU window
1.0×10^{8}	"Blink"
2.4×10^{8}	"Blink"
5.1×10^{8}	"Blink"
1.6×10^{9}	"Blink"
1.8×10^{9}	"Blink"
2.3×10^{9}	CPU turned off; power on reset (POR) to recover
4.4×10^{9}	CPU reset; auto recover
8.2×10^{9}	CPU turned off; POR to recover
2.6×10^{10}	CPU turned off; POR to recover

Total Dose Processor "History"

- INTEL 80386-20 (test date: 1993) – 1 µm CHMOS IV
  - Failure between 5-7.5 krad(Si)
    - *http://radhome.gsfc.nasa.gov/radhome/papers/tid/PPM-93-062.pdf*
- INTEL 80486DX2-66 (test date: 1995) – 0.8 µm CHMOS V
  - Failure between 20-25 krad(Si)
    - *http://radhome.gsfc.nasa.gov/radhome/papers/td80486.htm*
- INTEL Pentium III (test date: 2000-2) – 0.25 µm
  - Failure ~500 krad(Si)
    - *http://radhome.gsfc.nasa.gov/radhome/papers/tid/G020802_P3_TID.pdf*
- AMD K7 (test date: 2002) – 0.18 µm
  - Failure >100 krad(Si)
    - *http://radhome.gsfc.nasa.gov/radhome/papers/tid/G020802_P3_TID.pdf*
- *Do we need more proof that scaling is improving digital CMOS total dose performance?*

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Takeaway Thoughts

- Digital CMOS devices
  - Definitely can exceed *portions* of the ITAR criteria tested here without any intentional radiation hardening
- *However*, multiple support/peripheral devices (*i.e.*, surrounding the processor) failed at levels well below ITAR criteria
  - Likely bipolar or analog (video) functions
- No *ONE* conclusion can be made whether "commercial technology is pushing the ITAR envelope inadvertently"
  - Depends on the technology and device, BUT the potential for some devices to "push" is there
- Hardness assurance method used here, while clearly not as thorough as traditional ATE, provides a reasonable approach that is cost-effective

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