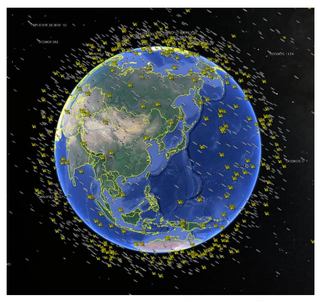
Fabrication of a Silicon Nanowire on a Bulk Substrate by Use of a Plasma Etching and Total Ionizing Dose Effects on a Gate-All-Around Field-Effect Transistor

Dong-Il Moon, Jin-Woo Han, and Meyya Meyyappan
Center for Nanotechnology, NASA Ames Research Center
E-mail: dong-il.moon@nasa.gov

Introduction

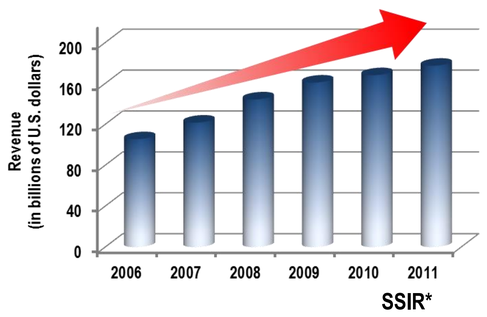
Space Applications

Artificial satellites



Source: Google Earth

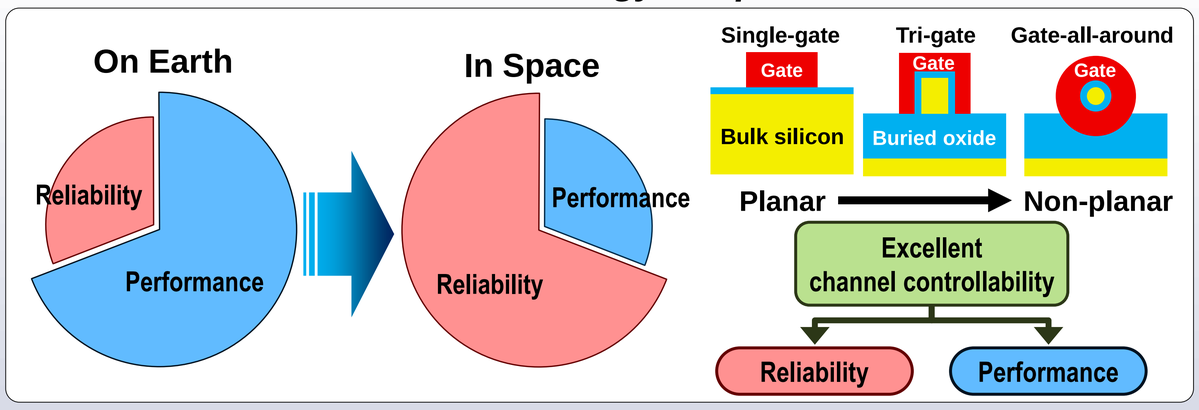
Satellite industry



- Thousands of the artificial satellites are on orbit.
- Continuous growth of the satellite industry is expected.

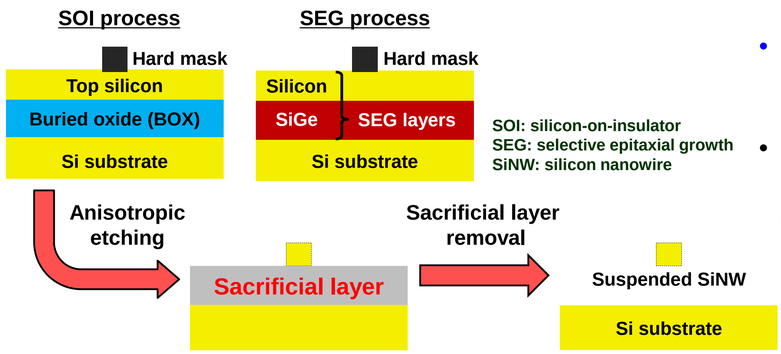
*SSIR: Sate of the Satellite Industry Report, satellite industry association (2012)

CMOS Technology in Space



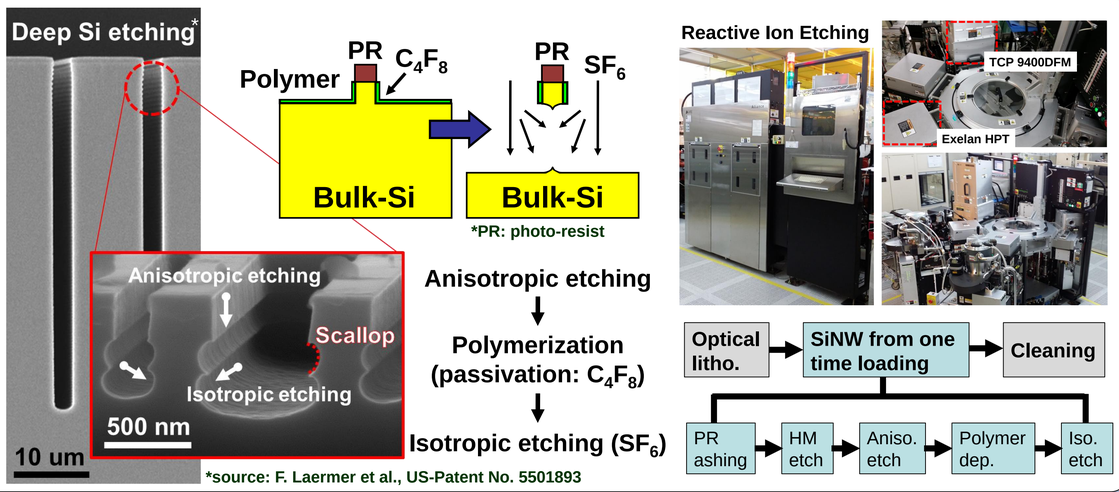
Fabrication of Suspended SiNWs

Previous Approaches

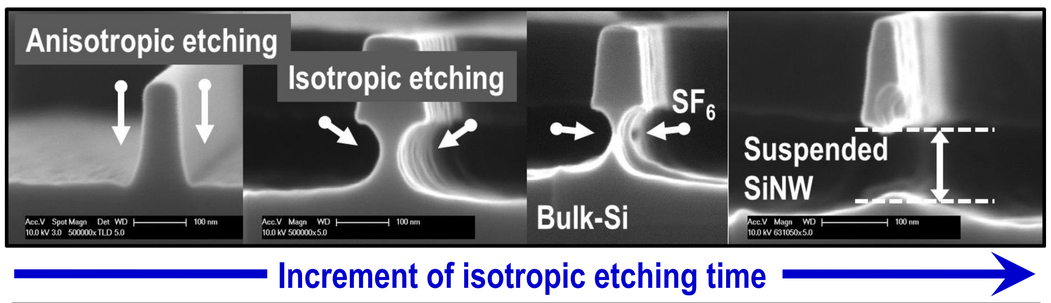


- **Suspended SiNW: basic building block for GAA FETs**
- **Previous approaches: SOI substrate or epitaxial growth on bulk**
  - CMOS low-compatible, high cost, and low throughput

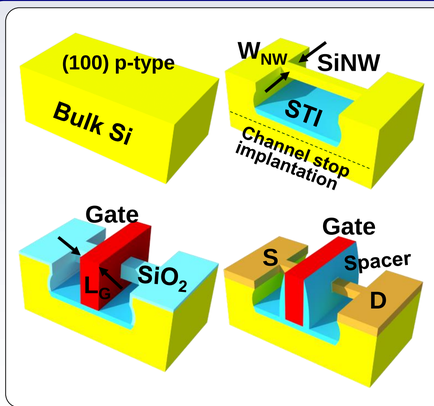
SiNW by One-Step Etching Route (This Work)



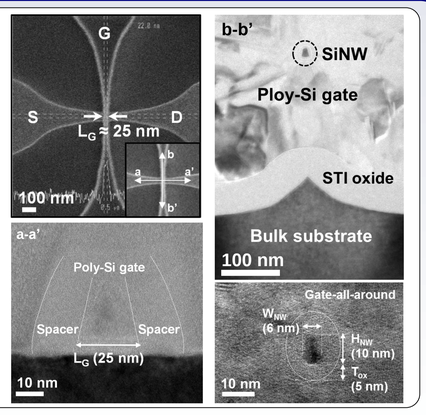
Process Optimization



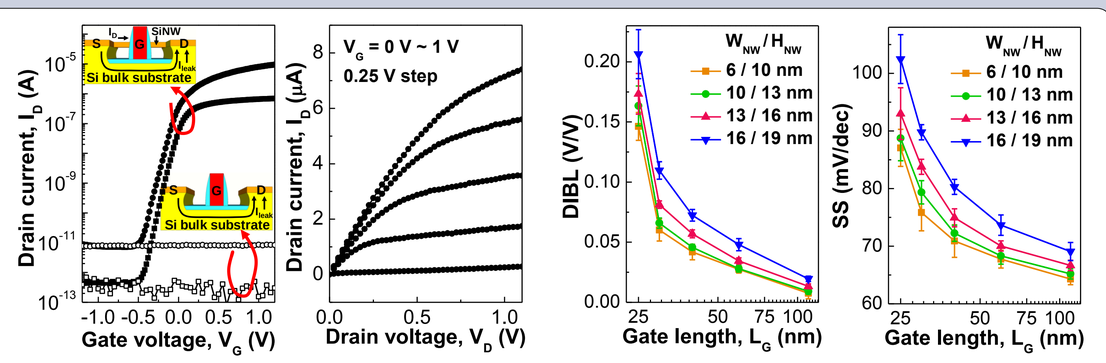
Process Flow of SiNW GAA FETs



- Bulk substrate
- **Suspended SiNW by one-step etching route**
- **Sacrificial oxidation**
- Oxide dep. and CMP
- Partial oxide etching (STI)
- Thermal oxidation
- *in-situ* n^+ poly-Si dep.
- Poly-Si CMP and HM dep.
- **Gate patterning**
- Spacer formation
- S/D implantation
- RTA and H_2 annealing



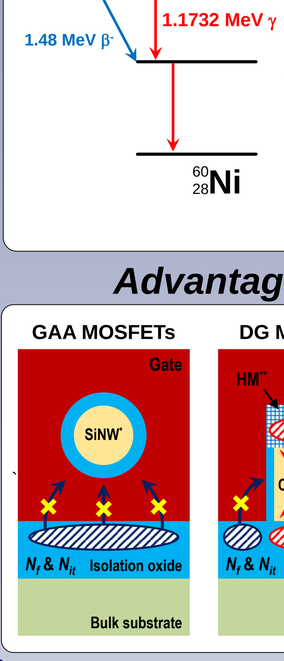
Electrical Characteristics



- **SiNW GAA FET on a bulk substrate**
  DIBL: 150 mV/V, SS: 87 mV/dec, $I_{ON}/I_{OFF} > 10^6$
- **Excellent immunity against SCEs**
  ➔ GAA structure with SiNW channel

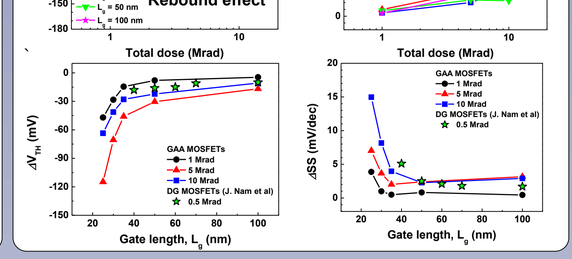
Radiation Effects on SiNW GAA FETs

Radiation Source

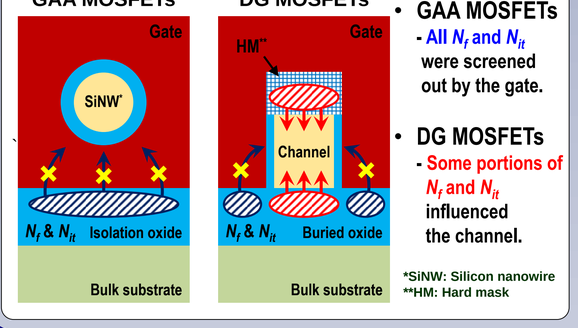


- ^{60}Co (Cobalt-60)
  - Common radiation source
  - g-ray with around 1.3 MeV
  c.f.) Part of cosmic ray
- Specific radiation condition
  - Total dose : 1, 5, 10 Mrad(SiO_2)
  - Dose rate : 460 rad(SiO_2)/s
  c.f.) 1 Mrad : typical tolerance of radiation hardened circuit

Dose Dependency



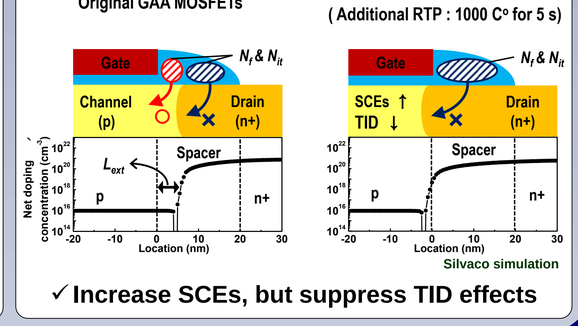
Advantage of GAA



- **GAA MOSFETs**
  - All N_f and N_{it} were screened out by the gate.
- **DG MOSFETs**
  - Some portions of N_f and N_{it} influenced the channel.

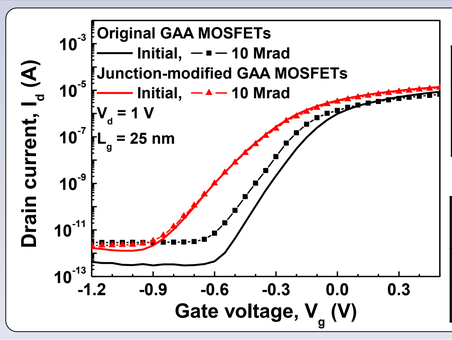
*SiNW: Silicon nanowire
**HM: Hard mask

Junction Modification



✓ Increase SCEs, but suppress TID effects

Optimization of SiNW GAA FETs



- **Increased short-channel effects (SCEs)**

	Original GAA FETs	Junction-modified GAA FETs
$V_{TH,initial}$	-0.332 V	-0.600 V
$SS_{initial}$	76.9 mV/dec	108.5 mV/dec

- **Suppressed total ionizing dose (TID) effects**

	Original GAA FETs	Junction-modified GAA FETs
ΔV_{TH}	- 60 mV	- 0.2 mV
ΔSS	10.9 mV/dec	3.3 mV/dec

Conclusions

- An **one-step plasma etching route** was developed to form a suspended **silicon nanowire** on **a bulk substrate**.
- A **gate-all-around field-effect transistor** was fabricated and characterized for **radiation hardening applications**.
- **The fabricated devices** showed stronger radiation-tolerance than the double-gate MOSFETs due to the **separation between the channel and the isolation oxide**.
- The role of the **gate spacer** on **TID effects** was observed and verified through the **overlapped junction profile**.