Fabrication of a Silicon Nanowire on a Bulk Substrate by Use of a Plasma Etching and Total Ionizing Dose Effects on a Gate-All-Around Field-Effect Transistor

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Introduction

Artificial satellites
Satellite industry

- Thousands of the artificial satellites are on orbit.
- Continuous growth of the satellite industry is expected.

"SSIR: State of the Satellite Industry Report, satellite industry association (2012)"

Space Applications

CMOS Technology in Space

On Earth
In Space

Reliability
Performance
Reliability

Excellent channel controllability

Electrical Characteristics

Increment of isotropic etching time
Optimization of height and width of SiNWs

- Suspended SiNW: basic building block for GAA FETs
- Previous approaches: SOI substrate or epitaxial growth on bulk
  - CMOS low-compatible, high cost, and low throughout

Fabrication of Suspended SiNWs

Previous Approaches

SOI process
- Hard mask
- Top silicon
- Buried oxide (BOX)
- SiGe
- SEG layers
- Sacrificial layer removal
- Sacrificial layer
- Substrate

SEG process
- Hard mask
- Silicon
- Sacrificial layer removal
- Sacrificial layer
- Substrate

SiNW by One-Step Etching Route (This Work)

Deep Si etching
Polymer
PR
C4F8
SF6

Anisotropic etching
Optical lithography
Isotropic etching (SF6)

Suspended SiNW

Process Optimization

Anisotropic etching
Isotropic etching
Sacrificial layer removal
Sacrificial layer
Suspended SiNW

Optimization of height and width of SiNWs

Increment of isotropic etching time

Process Flow of SiNW GAA FETs

Bulk substrate
Suspended SiNW by one-step etching route
Sacrificial oxidation
Cleave step, and CMP
Partial oxide etching (STI)
Thermal oxidation
in air; p+ poly-Si dep.
Poly-Si CMP and HM step.
Gate patterning
Spacer formation
S/D implantation
RTA and H3 annealing

Optimization of SiNW GAA FETs

- Increased short-channel effects (SCEs)
- Suppressed total ionizing dose (TID) effects
- Improved gate spacer on TID effects was observed and verified through the overlapped junction profile.