Reconfigurable Very Long Instruction Word (VLIW) Processor

For software-defined radio applications

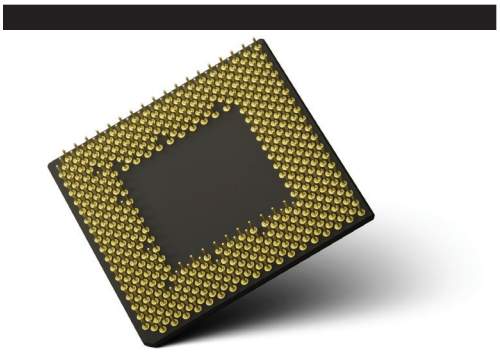
Future NASA missions will depend on radiation-hardened, power-efficient processing systems-on-a-chip (SOCs) that consist of a range of processor cores custom tailored for space applications. Aries Design Automation, LLC, has developed a processing SOC that is optimized for software-defined radio (SDR) uses. The innovation implements the Institute of Electrical and Electronics Engineers (IEEE) RazorII voltage management technique, a microarchitectural mechanism that allows processor cores to self-monitor, self-analyze, and self-heal after timing errors, regardless of their cause (e.g., radiation; chip aging; variations in the voltage, frequency, temperature, or manufacturing process). This highly automated SOC can also execute legacy PowerPC 750 binary code instruction set architecture (ISA), which is used in the flight-control computers of many previous NASA space missions.

In developing this innovation, Aries Design Automation has made significant contributions to the fields of formal verification of complex pipelined microprocessors and Boolean satisfiability (SAT) and has developed highly efficient electronic design automation tools that hold promise for future developments.

Applications

NASA and Commercial

- Implementing and verifying processor SOCs with any legacy ISA
- Adding new instructions that use reconfigurable functional units to accelerate specific applications
- Verifying properties of the resulting binary code



Phase II Objectives

- Design and verify a range of pipelined, dual-issue superscalar and VLIW processor cores
- Guarantee correct execution of legacy binary code from current space missions
- Implement new instructions that use reconfigurable functional units to accelerate SDR algorithms
- Design and verify a range of SOCs consisting of such processor cores
- Perform SAT-based technology mapping, placement, and routing of complex SDR operations to the reconfigurable functional units
- Compile SDR applications to the ISAs supported by the cores
- Run hardware-software cosimulations to measure the performance and power consumption of the SOCs and select an optimal design

Benefits

- Automated
- Fast
- Flexible
- Scalable
- Low power

Firm Contact

Aries Design Automation, LLC
Miroslav N. Velev
miroslav.velev@aries-da.com
2705 W. Byron St.
Chicago, IL 60618–3745
Phone: 773–773–6633

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