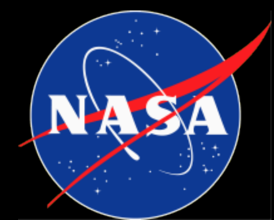

Single Event Effects in FPGA Devices 2015-2016

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Kenneth LaBel: NASA/GSFC

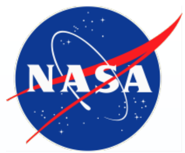
Jonathan Pellish: NASA/GSFC

To be presented by Melanie Berg at the NASA Electronic Parts and Packaging (NEPP) Program Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 13-16, 2016.

Acronyms

- Advanced Encryption Standard (AES)
- Agile Mixed Signal (AMS)
- ARM Holdings Public Limited Company (ARM)
- Block random access memory (BRAM)
- Built-in-self-test (BIST)
- Cache Coherent Interconnect (CCI)
- Combinatorial logic (CL)
- Commercial off the shelf (COTS)
- Complementary metal-oxide semiconductor (CMOS)
- Controller Area Network (CAN)
- Device under test (DUT)
- Digital Signal Processing (DSP)
- Direct Memory Access (DMA)
- Distributed triple modular redundancy (DTMR)
- Double Data Rate (DDR3 = Generation 3; DDR4 = Generation 4)
- Edge-triggered flip-flops (DFFs)
- Equipment Monitor And Control (EMAC)
- Error-Correcting Code (ECC)
- Field programmable gate array (FPGA)
- Floating Point Unit (FPU)
- Global Industry Classification (GIC)
- Global triple modular redundancy (GTMR)
- High Performance Input/Output (HPIO)
- High Pressure Sodium (HPS)
- High Speed Bus Interface (PS-GTR)
- Input – output (I/O)
- Intellectual Property (IP)
- Inter-Integrated Circuit (I2C)
- Internal configuration access port (ICAP)
- Joint test action group (JTAG)
- Lightwatt High Pressure Sodium (LW HPS)
- Linear energy transfer (LET)
- Local triple modular redundancy (LTMR)
- Look up table (LUT)
- Low Power (LP)
- Low-Voltage Differential Signaling (LVDS)
- Memory Management Unit (MMU)
- Microprocessor (MP)
- Multi-die Interconnect Bridge (EMIB)
- MultiMediaCard (MMC)
- Multiport Front-End (MPFE)
- Not OR logic gate (NOR)
- Operational frequency (fs)
- Peripheral Component Interconnect Express (PCIe)
- Personal Computer (PC)
- Phase locked loop (PLL)
- Phase Locked Loop (PLL)
- Power on reset (POR)
- Probability of flip-flop upset (PDFFSEU)
- Probability of logic masking (Plogic)
- Probability of transient generation (Pgen)
- Probability of transient propagation (Pprop)
- Processor (PC)
- Radiation Effects and Analysis Group (REAG)
- Secondary Control Unit (SCU)
- Secure Digital (SD)
- Secure Digital embedded MultiMediaCard (SD/eMMC)
- Secure Digital Input/Output (SDIO)
- Serial Advanced Technology Attachment (SATA)
- Serial Peripheral Interface (SPI)
- Serial Quad Input/Output (QSPI)
- Single event functional interrupt (SEFI)
- Single event latch-up (SEL)
- Single event transient (SET)
- Single event upset (SEU)
- Single event upset cross-section (σSEU)
- Spatial-Division-Multiplexing (SDM)
- Static random access memory (SRAM)
- System Memory Management Unit (SMMU)
- System on a chip (SOC)
- Transceiver Type (GTH/GTY)
- Transient width (τwidth)
- Triple modular redundancy (TMR)
- Universal Asynchronous Receiver/Transmitter (UART)
- Universal Serial Bus (USB)
- Universal Serial Bus (USB)
- Universal Serial Bus On-the-go (USB OTG)
- Watchdog Timer (WDT)
- Windowed Shift Register (WSR)

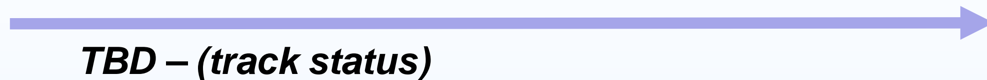
Overview



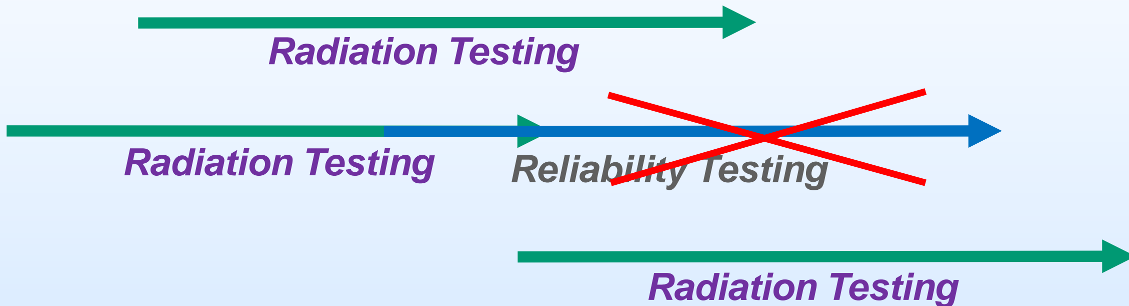
- Review of field programmable gate array (FPGA) roadmap chart (previously presented by Kenneth LaBel).
- Work performed by NASA/GSFC:
  - Security and trust.
  - Heavy-ion radiation testing:
    - Xilinx Kintex-7,
    - Altera Stratix-V, and
    - Microsemi RTG4.
- Plans for FY16 and out:
  - Microsemi, Xilinx, Altera, Synopsis.

Review of FPGA Roadmap Chart

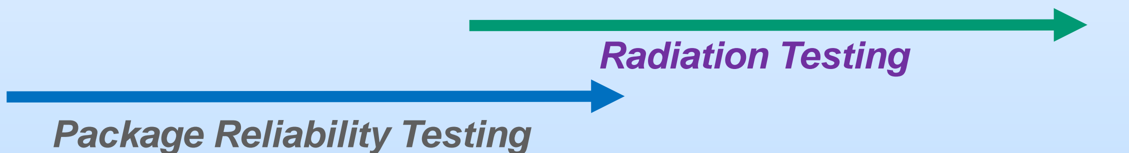
Trusted FPGA
- ***DoD Development***



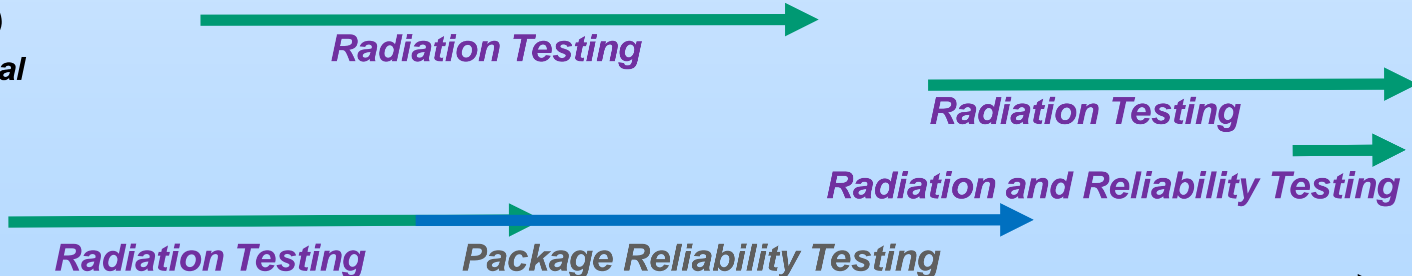
Altera
- ***Stratix 5 (28nm TSMC process commercial)***
- ***Max 10 (55nm NOR based commercial – small mission candidate)***
- ***Stratix 10 (14nm Intel process commercial)***



Microsemi
- ***RTG4 (65nm RH)***



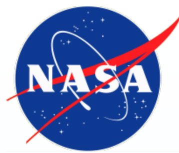
Xilinx
- ***7 series (28nm commercial)***
- ***Ultrascale (20nm commercial – planar)***
- ***Ultrascale+ (16nm commercial - vertical)***
- ***Virtex 5QV (65nm RH)***



FY=Fiscal Year

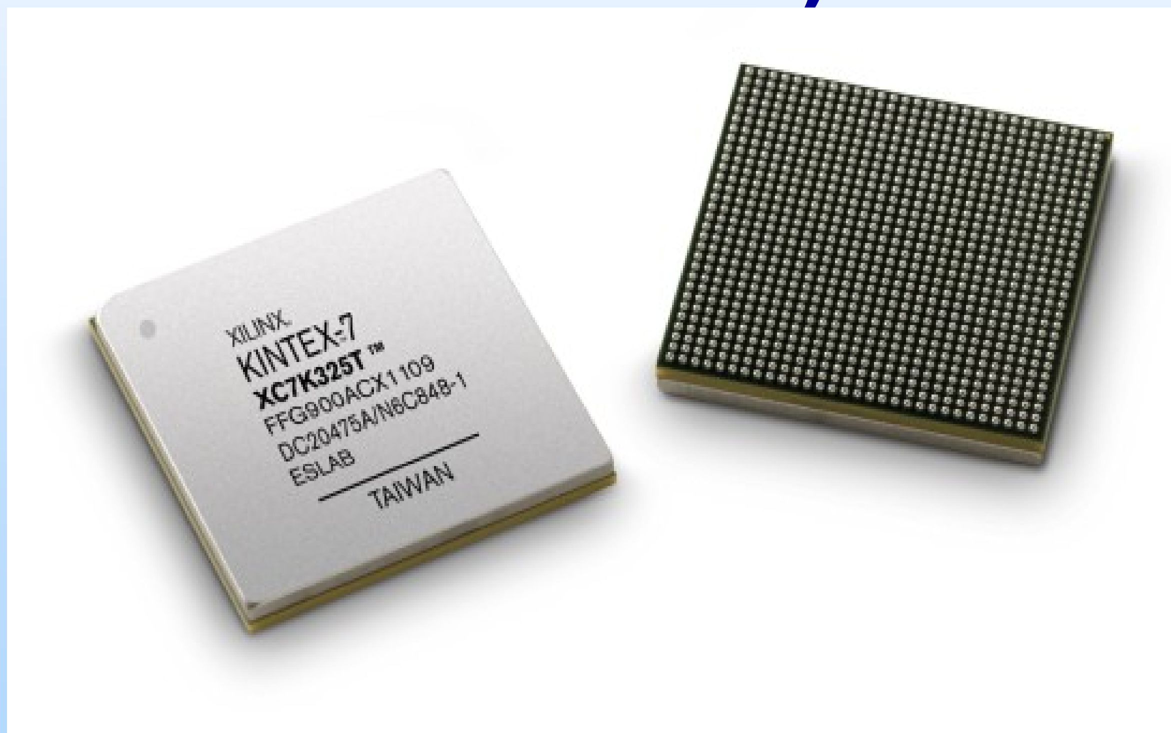
FY14 **FY15** **FY16** **FY17**

FPGA Security and Trust



- Goal: Support the U.S. government concerns over security and trust in FPGAs
- Conference participation:
  - Xilinx Security Working Group (XSWG) 2014 in Boulder/Longmont, CO.
  - Government Microcircuit Applications and Critical Technology Conference (GOMACTech) 2016 in Orlando, FL.
  - Hardened Electronics and Radiation Technology (HEART) 2016 in Monterey, CA.
  - Hardware-Oriented Security and Trust (HOST) 2015, McLean, VA.
- Collaboration with Aerospace Corporation and other agencies.

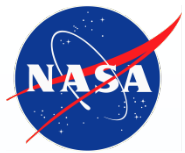
SRAM-based FPGA Mitigation Study using Xilinx Kintex-7 (XC7K325T-1FBG900)



Xilinx Kintex-7 Single Event Latch-up (SEL) Investigation

- **This is an independent study to determine the SEL susceptibility of the Commercial Xilinx Kintex-7 device.**
- **Prior SEL testing has been performed by other groups. They have reported observing SEL in the Xilinx 7-series devices.**
  - **Lee, D.S.; Wirthlin, M.; Swift, G.; Le, A.C., "Single-Event Characterization of the 28 nm Xilinx Kintex-7 Field-Programmable Gate Array under Heavy Ion Irradiation," *Radiation Effects Data Workshop (REDW), 2014 IEEE* , vol., no., pp.1,5, 14-18 July 2014**
- **NEPP decided to perform follow-up tests for validation.**
  - **NEPP test procedure was slightly different:**
    - **Real-time configuration memory scrubbing during irradiation.**
    - **Analog circuitry monitoring.**
    - **Custom DUT board was designed to connect with the NEPP LCDT.**
    - **Temperature variation.**
- **Note: SEL is determined by an increase of DUT current that can only be lowered by reducing the DUT power below threshold.**

Summary of Kintex-7 during Single Event Upset (SEU)-Heavy-Ion Testing



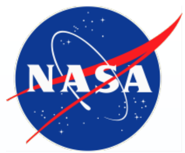
LET: Linear energy transfer

- **Last year's data:** SEL results concur with other groups:
  - With real-time scrubbing.
  - However, on-set SEL was observed at a lower LET by NASA/GSFC (11.6 MeV*cm^2/mg versus 19 MeV*cm^2/mg).
- **NEPP Additional testing:** at elevated temperature.
  - Uncovered susceptibility as low as an LET = 8.6 MeV*cm^2/mg with a SEU cross-section approximately equal to 1x10^{-7} cm^2/device.
  - NEPP is in discussion with Xilinx regarding whether the event should be classified as an SEL (micro-SEL) or "something else." More information to come after July 2016.
- The full Kintex-7 SEU dataset is still currently being analyzed and will be available by August 2016. Challenge is post processing software.

Kintex-7 SEU Mitigation Study Overview

- This is an independent study to determine the effectiveness of various triple modular redundancy (TMR) schemes implemented in SRAM-based FPGA devices.
- TMR schemes are defined by what portion of the circuit is triplicated and where the voters are placed.
  - The strongest TMR implementation will triplicate all data-paths and contain separate voters for each data-path.
  - However, this can be costly: area, power, and complexity.
  - A trade is performed to determine the TMR scheme that requires the least amount of effort and circuitry that will meet project requirements.
- Presentation scope:
  - Block TMR (BTMR), Local TMR (LTMR), Distributed TMR (DTMR), and Global TMR (GTMR) .

TMR Descriptions



DFF: Edge triggered flip-flop; *CL: Combinatorial Logic*

TMR Nomenclature	Description	TMR Acronym
Block TMR	Entire design is triplicated. Voters are placed at the outputs.	BTMR
Local TMR	Only the DFFs are triplicated. Voters are placed after the DFFs.	LTMR
Distributed TMR	DFFs and CL-data-paths are triplicated. Similar to a design being triplicated but voters are placed after the DFFs.	DTMR
Global TMR	DFFs, CL-data-paths and global routes are triplicated. Voters are placed after the DFFs.	GTMR or XTMR

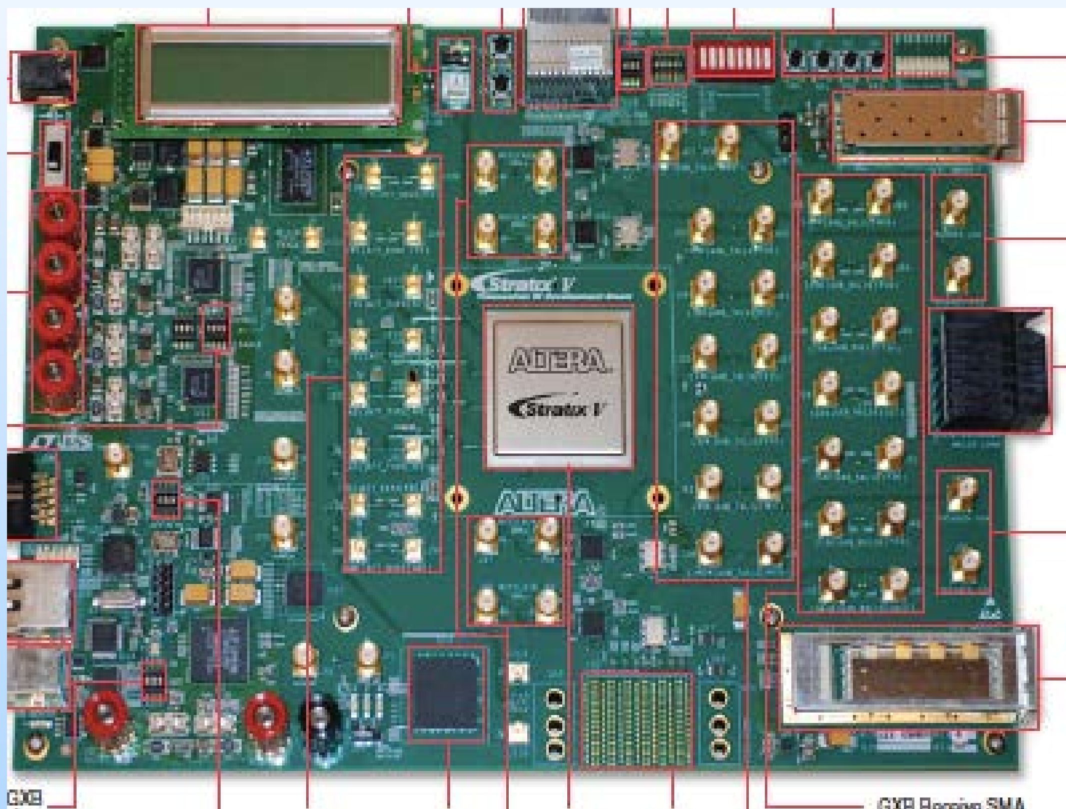
Note: It has been suggested to separate (partition) TMR domains in SRAM based designs so that there are no overlapped shared resources. Shared resources become single points of failure.

Summary of Mitigation Application to Kintex-7 during SEU-Heavy-Ion Testing

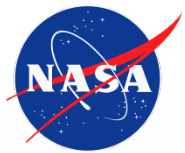
SEFI: single event functional interrupt

- **Mitigation study proves DTMR is effective for this design implemented in an SRAM-based FPGA.**
  - **However, for flushable designs BTMR might be acceptable.**
  - **LTMR is not acceptable in SRAM-based FPGAs for any design.**
  - **Partitioning may not be necessary.**
- **Internal scrubbing will have a higher SEFI rate and may need further investigation for project usage.**
- **Although GTMR has been implemented in V5 families and earlier Xilinx device families, NEPP has suggested to avoid GTMR because clock skew is difficult to control.**
  - **Via heavy-ion SEU testing, It has been observed in the Xilinx 7-series, that clock skew and resultant race conditions are unavoidable.**
  - **This is due to the speed of combinatorial logic and route delays in the 7-series versus earlier Xilinx FPGA device families.**
- **Synopsis is working on their tool. However, it is not ready.**

SRAM-based FPGA Study using the Altera Stratix-V (5SGTMC7K3F40C2)

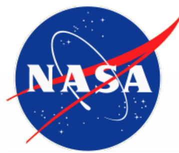


Stratix-V SEE Testing Overview and Goals



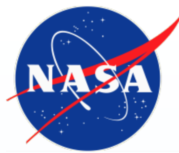
- This is a NASA Electronics Parts and Packaging (NEPP) investigation to determine the single event destructive and transient susceptibility of the Altera Stratix-V device under test (DUT).
- For preliminary evaluation: the DUT is configured to have shift registers as test structures to measure specific potential single event effect (SEE) susceptibilities of the device.
- Design/Device susceptibility is determined by monitoring the DUT for Single Event Transient (SET) and SEU induced faults by exposing the DUT to a heavy-ion beam.
- Potential SEL is checked throughout heavy-ion testing by monitoring device current.

Altera Stratix-V Radiation Test Development



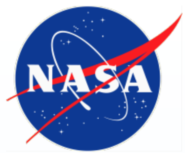
- New entry into the aerospace market with commercial off the shelf (COTS) expectation
  - 28nm bulk CMOS
- Accelerated SEE testing was performed on Altera Signal Integrity (SI) evaluation boards that contained one Stratix V GX FPGA .
  - Custom interface was designed to connect to the LCDT for increased visibility during accelerated radiation testing.
  - Voltage supplies are separated for accurate voltage monitoring.
- Phase I tests (dates: June 2015 and October 2015):
  - Tests were performed in collaboration with Cobham.
  - SEU evaluation of shift registers and internal scrubbing was performed.
  - SEL evaluation was performed.
- Phase II tests (TBD yet most likely cancelled):
  - Shift registers, counters, PLLs, and DSPs.
  - Use of Synopsis tool for mitigation insertion.
- Phase III tests:(TBD yet most likely cancelled):
  - High speed serial interfaces (TBD), instantiated processor(TBD).

Altera Stratix-V (5SGTMC7K3F40C2) Evaluation Board Schematic



Buttons, Switches, Displays
16 Char x 2 Line LCD
8 User LEDs
4 User Push Buttons
8 User DIP Switch
10/100/1000 Ethernet
RJ45+ Magnetics
Marvell 88E1111 Ethernet PHY
USB-Blaster
USB Type-B Connector
FTDI 745BL USB PHY
MAX II EPM570M CPLD
Temperature Measure
5-V Fan
Dual Temp Sensor
TDIODES
Temperature
Power Monitor
15-bit ADCs 10-bit IDACs
ADC
2-wire Ch1
2-wire Ch8
Power Circuitry
Pwrgood
ALTERA
Stratix V GT
12.5-Gbps Channels
7 TX/RX
Tyco Connector
1 TX/RX
1 SFP+
7 TX/RX
Amphl/FCI Connector
7 TX/RX
28 SMA Connectors
1 TX/RX
XFP
7 TX/RX
Molex Connector
25.78-Gbps Channels
4-ATT TX/RX
16 MMPX Connectors
1 Gb Flash
Flash
FPP Config
MAX II EPM2210 CPLD
PGMSEL
Clock Circuitry
3 Configuration Status LEDs
FPP Configuration

Altera Stratix-V Configuration Evaluation



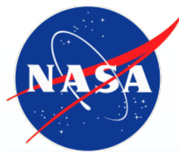
- It is important to note that currently there is no independent method to evaluate Altera configuration memory.
- This is noted because the Stratix-V has a SRAM-based configuration.
  - From previous studies of SRAM-based FPGAs (e.g., Xilinx commercial devices), the configuration (SRAM) proved to be the most susceptible.
  - Outside of bit-interleaving and internal scrubbing, no radiation hardening of the Stratix-V configuration SRAM cells has been reported by Altera. This leaves Stratix-V SEU-characterization similar to a commercially available Xilnx device families.
- It is imperative to be able to perform a thorough and independent evaluation of the most susceptible portions of an FPGA that can potentially be targeted for critical applications.

Altera Stratix-V Radiation Phase I Test Results: Core Current Rise during Irradiation

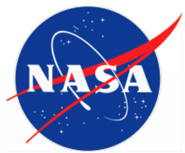
- **NASA Goddard (NEPP) originally preformed accelerated heavy-ion testing on shift registers with 100,000 flip-flop (DFF) stages.**
  - Significant core current increase while under the beam is linear. Current rise is LET dependent and was observed to reach 5x normal operating conditions at Xe.
  - Core current stops increasing when beam is removed, and returns to pre rad values after re-program
- **Other teams tested with a significantly smaller number of shift register DFF stages and did not observe the current increase.**
- **Cobham decided to investigate the discrepancy and implemented a large shift register. Cobham was able to observe the same core current rises as NASA Goddard.**

The original NEPP test evaluation board used during heavy-ion testing was thinned to 110um and was donated by Altera and LANL.

Altera Stratix-V Radiation Phase I Test Results: Questionable Power Cycle



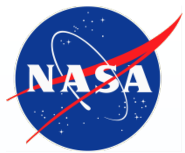
- The following data was obtained in collaboration with Cobham. Two evaluation boards were used: original used by NEPP and another thinned by Cobham to 50um.
- There was one run at 80 MeV*cm^2/mg, ~105°C, angle 60,(effective LET=102 MeV*cm^2/mg) where the device did not recover with a re-configuration after the beam was removed. After the test, the team cycled power.
  - Additional studies need to occur to determine what happened. The flux was 1x10^4 particles/s*cm^2 and the goal was to demonstrate SEL immunity by reaching a fluence of 1e^{7}particles/cm^2 .
  - The high-current condition occurred within ~4 seconds.
  - The flux was lowered to 1x10^{3}particles/cm^2 and re-ran the test to a fluence of 1x10^{6}particles/cm^2 (~20 mins). The test was run without any alarming anomalies. Whenever the beam was turned off, we could re-configure the device successfully.



Altera Stratix-V Radiation Phase I Test Results: FPGA Fabric Shielding – I/O Isolation

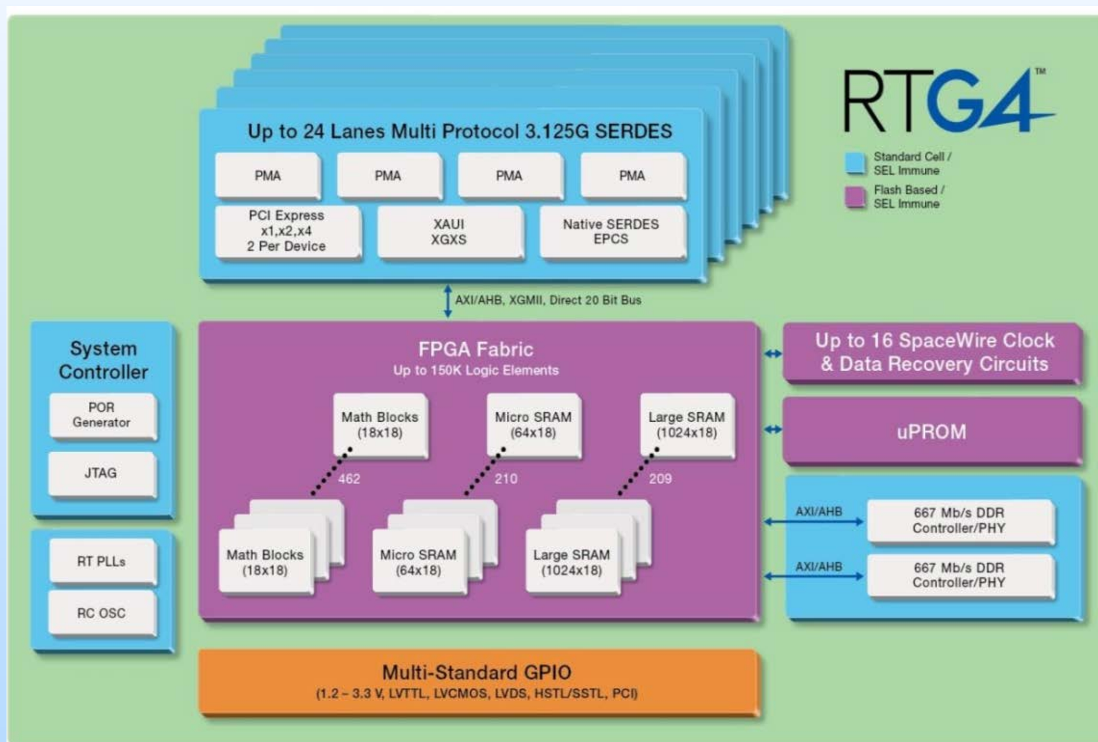
- **Cobham specific test:**
  - A test was performed with the FPGA fabric shielded and only the GPIO sides of the die exposed.
  - The design was a high-fanout design using 300 IOs. The DUT was irradiated at a $5x10^3$ /cm^2/s flux rate, at 80 Mev*cm^2/mg and a DUT temp of 105°C.
  - A fluence of $1x10^6$ /cm^2 was reached on this run, without any anomalies.

Altera Stratix-V Radiation Phase I Test Results: FPGA Fabric Shielding – Internal Scrubber

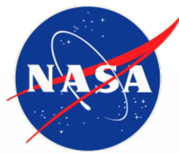


- **Internal scrubber failed during all tests.**
- **Flux was relatively high to draw conclusions. Flux was high because the primary goal of testing was SEL.**
- **The effectiveness of the internal need more investigation.**
- **The level of mitigation of the internal scrubber is unknown.**

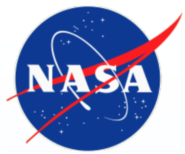
Flash-based FPGA Study using the Microsemi RTG4 (RT4G150-CG1657M)



Microsemi RTG4



- New Entry into the Aerospace Market with Space-grade Expectation
  - 65nm
- Custom daughter DUT cards have been built.
- Phase I tests (date: Winter 2015 – Summer 2016):
  - Shift registers and counters.
- Phase II and Phase III tests (date Summer 2016-2017):
  - PLLs and DSPs
  - High speed serial interfaces (XAUI, PCIe, Spacewire, and Spacefiber), instantiated processor (TBD).
  - Use of Synopsis tool for mitigation insertion.



Plans for FY16 and out: Xilinx, Altera, and Synopsis. We Looking for Collaborators

Xilinx Kintex UltraScale

- New Entry into the Aerospace Market with COTS Expectation
  - 20 nm planar process (TSMC)
- Prototype evaluation board will be purchased for early design development and early latch-up testing.
  - Custom interface will be designed to connect to the LCDT for increased visibility during accelerated radiation testing.
- Phase I tests (fall 2016):
  - Evaluation board latch-up investigation.
- Phase II tests (date TBD):
  - Shift registers, counters, PLLs, and DSPs.
  - Use of Synopsis tool for mitigation insertion.
- Phase III tests (TBD):
  - High speed serial interfaces (TBD), embedded processors.

Xilinx Zynq UltraScale+ Figure

Figure is compliments of Xilinx

Processing System

Application Processing Unit
- Quad ARM Cortex™-A53
- NEON™
- Floating Point Unit
- 32KB I-Cache with Parity
- 32KB D-Cache with ECC
- Memory Management Unit
- SCU
- GIC
- CCI/SMMU
- 1MB L2 Cache/ECC

Graphic Processing Unit
- ARM Mali™- 400 MP
- Geometry Processor
- 2 Pixel Processors
- Memory Management Unit
- 64KB L2 Cache

DDR Controller
- DDR4/3/3L, LPDDR4/3, ECC Support

256KB OCM with ECC

High Speed
- Display Port
- USB 3.0
- SATA 3.0
- PCIe Gen2
- PS-GTR

Real-Time Processing Unit
- Dual ARM Cortex™-R5
- Vector Floating Point Unit
- Memory Protection Unit
- 128KB TCM with ECC
- 32KB I-Cache with ECC
- 32KB D-Cache with ECC
- GIC

Security
- Configuration AES Decryption, Authentification and Secure Boot
- TrustZone
- Voltage/Temp Monitor

Platform Management Unit
- Power
- System Management

System Control
- DMA, Timers, WDT, Resets, Clocking and Debug

General Connectivity
- Gigabit Ethernet
- CAN
- I2C
- UART
- USB 2.0
- SPI
- Quad SPI NOR
- NAND
- SD/eMMC

Programmable Logic

Storage and Signal Processing
- Block RAM
- UltraRAM
- DSP

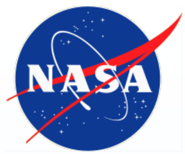
General Purpose IO
- High-Performance HPIO
- High Density HDIO

High Speed Connectivity
- GTH
- 100G EMAC
- GTY
- PCIe Gen4
- Interlaken

Video Codec
- H.265/H.264
- AMS

Xilinx Zynq UltraScale+

- New Entry into the Aerospace Market with COTS Expectation
  - 16nm vertical process (TSMC)
- Multi-Processor System on a Chip (MPSoC) family.
- Prototype evaluation board will be purchased for early design development and early latch-up testing.
- Planning to receive parts in fall of 2016.
- Custom daughter (DUT) cards will be built (date TBD).
- Phase I tests (date TBD):
  - Evaluation board latch-up investigation.
- Phase II tests (date TBD):
  - Shift registers, counters, PLLs, and DSPs.
  - Use of Synopsis tool for mitigation insertion.
- Phase III tests (TBD):
  - High speed serial interfaces (TBD), embedded processors.



Altera Stratix-10 Figure

Figure is compliments of Altera

Package Substrate

Transceiver Tile (24 Channels) | PCIe Gen3 Hard IP | EMIB

Transceiver Tile (24 Channels) | PCIe Gen3 Hard IP | EMIB

Transceiver Tile (24 Channels) | PCIe Gen3 Hard IP | EMIB

Variable-Precision, Hard Floating-Point DSP Blocks

M20K Embedded Memory Blocks

Hard Memory Controllers, I/O PLLs General-Purpose I/O Cells, LVDS

HPS

HyperFlex Core Logic Fabric

Variable-Precision, Hard Floating-Point DSP Blocks

M20K Embedded Memory Blocks

HyperFlex Core Logic Fabric

SDM

Hard Memory Controllers, I/O PLLs General-Purpose I/O Cells, LVDS

Variable-Precision, Hard Floating-Point DSP Blocks

M20K Embedded Memory Blocks

EMIB | PCIe Gen3 Hard IP | Transceiver Tile (24 Channels)

EMIB | PCIe Gen3 Hard IP | Transceiver Tile (24 Channels)

EMIB | PCIe Gen3 Hard IP | Transceiver Tile (24 Channels)

Quad-Core ARM Cortex-A53-Based Hard Processor System

ARM Cortex-A53: NEON; FPU; 32 KB I-Cache with Parity; 32 KB D-Cache with ECC

ARM Cortex-A53: NEON; FPU; 32 KB I-Cache with Parity; 32 KB D -Cache with ECC

ARM Cortex-A53: NEON; FPU; 32 KB I-Cache with Parity; 32 KB D-Cache with ECC

ARM Cortex-A53: NEON; FPU; 32 KB I-Cache with Parity; 32 KB D-Cache with ECC

1 MB L2 Cache

System MMU | Cache Coherency Unit

JTAG Debug or Trace | 256 KB RAM | Timers (x11)

LW HPS to CORE | HPS to CORE BRIDGE | CORE to HPS BRIDGE

QSPI FLASH | SD/SDIO/ MMC[1]

USB OTG (x2)[1] | DMA (8 Channel)

UART (x2) | HPS IO

I^2C (x5) | NAND Flash[1,2]

EMAC with DMA(x3)[1] | SPI (x5)

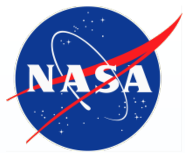
MPFE[3] | Configuration

To be presented by Melanie Berg at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 13-16, 2016.

Altera Stratix-10

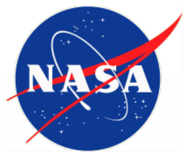
- **New Entry into the Aerospace Market with COTS Expectation**
  - **Intel 14 nm Tri-Gate** process**.**
- **Integrated quad-core 64 bit ARM Cortex-A53 hard processor system.**
- **Prototype evaluation board will be purchased for early design development and early latch-up testing.**
- **Planning to receive parts (TBD).**
- **Custom daughter (DUT) cards will be built (date TBD).**
- **Phase I tests (date TBD):**
  - **Evaluation board latch-up investigation.**
- **Phase II tests (date TBD):**
  - **Shift registers, counters, PLLs, and DSPs.**
  - **Use of Synopsis tool for mitigation insertion.**
- **Phase III tests (TBD):**
  - **High speed serial interfaces (TBD), embedded processors.**

Conclusions



- NEPP has provided and will continue to investigate:
  - New accelerated-radiation test methodologies for FPGA devices and embedded hard-IP (e.g., processors).
  - Mitigation strategies specific to FPGA types and how to measure their efficacy for meeting project requirements.
- NEPP continues independent investigation of various FPGA devices:
  - Destructive mechanisms and SEL.
  - SEU characterization.
  - Total Ionizing Dose (TID) characterization.

Acknowledgements



- **Supporters:**
  - Defense Threat Reduction Agency (DTRA)
  - NASA Electronics Parts and Packaging (NEPP) Program
- **Current Collaborators:**
  - Xilinx,
  - Microsemi,
  - Altera,
  - Synopsis,
  - Cobham,
  - Harris,
  - Honeywell,
  - Aerospace Corporation,
  - NASA Space Launch System (SLS) mission, and
  - NASA Transiting Exoplanet Survey Satellite (TESS) mission.