

Detector control and data acquisition for the Wide-Field Infrared Survey Telescope (WFIRST) with a custom ASIC

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ABSTRACT

The Wide-Field Infrared Survey Telescope (WFIRST) will have the largest near-IR focal plane ever flown by NASA, a total of 18 4K x 4K devices. The project has adopted a system-level approach to detector control and data acquisition where 1) control and processing intelligence is pushed into components closer to the detector to maximize signal integrity, 2) functions are performed at the highest allowable temperatures, and 3) the electronics are designed to ensure that the intrinsic detector noise is the limiting factor for system performance. For WFIRST, the detector arrays operate at 90 to 100 K, the detector control and data acquisition functions are performed by a custom ASIC at 150 to 180 K, and the main data processing electronics are at the ambient temperature of the spacecraft, notionally ~300 K. The new ASIC is the main interface between the cryogenic detectors and the warm instrument electronics. Its single-chip design provides basic clocking for most types of hybrid detectors with CMOS ROICs. It includes a flexible but simple-to-program sequencer, with the option of microprocessor control for more elaborate readout schemes that may be data-dependent. All analog biases, digital clocks, and analog-to-digital conversion functions are incorporated and are connected to the nearby detectors with a short cable that can provide thermal isolation. The interface to the warm electronics is simple and robust through multiple LVDS channels. It also includes features that support parallel operation of multiple ASICs to control detectors that may have more capability or requirements than can be supported by a single chip.

Keywords: data acquisition, mixed-signal ASIC, sensor control, sensor digitization, cryogenic ASIC

1. INTRODUCTION

Modern generation large astronomy focal plane arrays (FPAs) place stringent demands on the control and data acquisition electronic support systems. Most of the detectors used in these FPAs require cryogenic operation, and present interesting signal integrity and thermal isolation trades and challenges. At one extreme, a solution for hybrid detectors is to incorporate ever-increasing functions into the Read-Out Integrated Circuit (ROIC). Using modern CMOS designs, these ROICs can be made to include all control and even data acquisition (analog-to-digital conversion, ADC) functions, providing a true photons-to-bits capability in a single device. However, the additional power dissipation at the cold detector may present an undesirable system-level thermal trade. At the other extreme, for small numbers of detectors, it is possible to use only electronics at the warm ambient temperature of the instrument with a relatively simple and low-power ROIC. However, this approach requires extreme care in interconnect design since the main thermal isolation needs to ensure signal integrity for very low-level analog signals over potentially large distances.

The Wide-Field Infrared Survey Telescope (WFIRST), which NASA is planning to launch in the early 2020's, is the next large space astrophysical observatory after the James Webb Space Telescope (JWST). WFIRST entered Phase A of

development in early 2016. The main imaging camera, the Wide-Field Instrument (WFI) will use a mosaic of 18 4K x 4K format near-IR detectors to conduct the surveys required for cosmology and exoplanet (microlensing) studies¹. This will be the largest infrared focal plane flown on a NASA mission, and presents interesting engineering challenges in material selection, thermal design, and electrical architecture. The material for the mosaic plate and the detector packages is currently Sandvik Osprey CE6, chosen for its low mass, high thermal conductivity, and mechanical stability. The detector operating temperature of 90 to 100 K is maintained by an ultra-low vibration reverse-Brayton cycle mechanical cryocooler. The electrical architecture is discussed further in the body of the paper, with a focus on the custom ASIC (Application-Specific Integrated Circuit).

There are a few additional detectors planned for the mission in the Auxiliary Guider and the Integral Field Channel within the WFI. These may or may not use the same architecture, depending on the result of on-going trades. A second scientific instrument, the exoplanet coronagraph, will have a silicon-based detector and will likely use a different architecture¹.

1.1 Electrical Architecture Design

For the electrical architecture, we want to maximize signal integrity while simultaneously minimizing the load to the thermal system. The adopted approach is based on two driving principles: 1) control and analog-to-digital conversion is pushed into components close to the detector to maximize signal integrity, and 2) processing functions are performed at the highest allowable temperatures, simplifying the system-level thermal design by not cooling components that do not require such cooling to function. Performance wise, the overall system shall not degrade the performance of the basic detectors by more than 10%. This is obviously dependent on the detectors used, and the baseline for the design is the Teledyne Imaging Sensors H4RG-10 ROIC with a 2.5 μm cutoff HgCdTe material. The thermal design provides ample margin for the 90 to 100 K operating temperature of the detectors while still supporting an operating temperature of 150 to 180 K for the cold electronics. The bulk of the processing will occur in the instrument (warm) Focal Plane Electronics which are at the ambient instrument temperature of ~ 300 K.

The cold electronics control and acquire data from the detectors. This design choice minimizes the number of wires (and thus the parasitic thermal loading) between the detectors and the warm electronics. More importantly, low noise video signals do not need to be transmitted over large distances and through several thermal zones.

The warm electronics control higher-level focal plane operation. It is responsible for configuring the ASICs as well as overall focal plane synchronization and commanding of the 18 distinct detectors and their cold electronics. Communication between the cold and warm electronics uses multiple LVDS (Low-Voltage Differential Signaling) lines. Conditioned power for the ASICs is also provided by the warm electronics.

We are aware of two other ASICs that could perform similar functions to those required for WFIRST. We elected to create a new design based on our perception of the shortcomings of these other devices.

The Teledyne Imaging Systems SIDECAR ASIC² has been in use in astronomy for some time and has been flown on the Hubble Space Telescope (for the Advanced Camera for Surveys Repair mission), Landsat Data Continuity Mission (Thermal Infrared Sensor), and planned for the James Webb Space Telescope. This design has served the previous generation of instruments very well, but suffers from shortcomings in performance. One example is well documented from the JWST NIRSpec project³. The main performance shortcomings relate to analog-to-digital conversion noise and low-frequency noise on the internally generated biases.

We understand that ESA/Caeleste has been developing a similar device based on discussions at the 2013 Scientific Detector Workshop⁴. This device has some architectural choices that make it more difficult to use for WFIRST. In particular, it supports 16 analog inputs, which is half of what we need for the WFIRST detectors. It would add system complexity to require two ASICs per detector. In addition, the digital interfaces to the warm electronics are fairly advanced (*e.g.*, SpaceWire). This feature is not required for performance but will likely increase power dissipation. For small numbers of detectors this could be a very good choice, but for WFIRST, further optimization was justified.

1.2 Custom ASIC Design Drivers

One of the driving principles for the ASIC functional design is that it should be made as “user friendly” as possible. In the case of a flight project, simplicity facilitates flight firmware/software validation and verification. With this in mind, the design of the ASIC was guided by three benchmark cases. All these cases used a notional Teledyne Imaging Sensors

H4RG-10 ROIC for the design study. The typical operating configuration is 100 or 200 kHz pixel rate, 32 or 64 video outputs, and continuous frame readout (sampling up the ramp).

Benchmark I: Operate the detector in a basic scientific mode readout (sample up the ramp for a fixed number of readout frames) without the need for extensive programming.

Benchmark II: Operate as in Benchmark I, but with at least one guide window readout at ~ 20 Hz CDS, again without the need for extensive programming. Guide windows are implemented as special clocking patterns to the detector that are dependent on the location and size of the guide window.

Benchmark III: Support immediate dynamic resets of pixels based on the video signal output.

These benchmark cases were used to define the target specification and basic architectural features, which then drove the detailed design. Highlights of the target specification include:

Detector Biases:

- 24 individually programmable bias channels configurable as current or voltage biases
- 12-bit resolution, < 2 mV (voltage mode) or 2% of maximum current setting
- Noise < 10 μ V rms (for current mode assumes 1 k Ω load)

Detector Clocks:

- 32 programmable clock inputs/outputs
- All channels synchronous to system clock, selectable routing, programmable delay and polarity
- Selectable output voltage and drive strength
- Ability to synchronize multiple ASICs

ASIC Operation:

- Basic operation with a sequencer, support more complex functions (like amplitude dependent pixel level dynamic reset) with an on-chip microcontroller
- Compatible with large format CMOS analog detectors
- < 300 mW at 100 kHz with 32 channels ADC
- Compatible with spacecraft environment (launch, radiation, etc.) and cryogenic operation to < 90 K
- Provide basic math functions on ADC outputs (see text)

Detector Pixel Data:

- 40 analog input channels with adjustable gain (0 – 24 dB) and offset
- 16 bits resolution up to 200 kHz, 14 bit resolution at 3 MHz
- Noise < 15 μ V at 400 mV swing
- DNL < 0.5 LSB, INL < 2 LSB

Scientific Data Outputs:

- Up to 16 LVDS channels (32 in CMOS mode) for science data communication to warm electronics

Key detailed design drivers are 1) minimize power dissipation (to more easily support cryogenic operation), 2) “normal” die/package size (to enable efficient packaging for flight and to optimize yield), 3) radiation hardened implementation (to support operation in the space environment).

2. DEVELOPMENT PLAN

The WFIRST Project implemented a three-phase development plan in order to minimize the risk of developing the custom ASIC hardware. This effort started in early 2013 with the initial planning. As of the presentation of this paper, the first two phases have been completed, and the third phase, the full ASIC, has completed design and layout with silicon manufacturing about to begin. These phases are summarized here, and the hardware/results are described in the following sections.

2.1 Phase 1 - Test Structures Chip

This initial phase focused on ensuring that all the device parameters are known for modeling cryogenic performance, and that key fundamental building blocks are optimized.

2.2 Phase 2 - Analog-to-Digital Converter Test Chip

This second phase retired key risks in the analog-to-digital converter design, which we determined was the highest risk element in the design.

2.3 Phase 3 - Full ASIC

The final ASIC design is completed using components and tools developed during the first two phases. Additional architectural digital logic and processing features were implemented in parallel while the hardware for Phases 1 and 2 was being developed.

3. TEST STRUCTURES CHIP

3.1 Overview

From the start of this project, we had a concern about our ability to simulate and understand the circuit behavior at cryogenic temperatures. This concern applies at the level of the individual transistor types (*e.g.*, I/V curves and speed) as well as higher-level performance achieved in the basic analog amplifier/buffer building blocks (most notably, noise and stability). Some data is available in the literature and from the foundries, but much of the low temperature behavior is foundry-specific. Thus, the process used to build our ASIC was determined early on and we designed test structures to validate the models. The Test Structures Chip was implemented as a multi-project wafer run to minimize cost.

In the end, two versions of the Test Structures Chip were created. The primary motivation was to evaluate lot-to-lot performance variations. In addition, a minor adjustment to the band-gap reference voltage generator was implemented in the second iteration.

The single transistors in this chip also provide a range of test devices to explore long-term reliability at cryogenic temperatures. In particular, we plan to test for hot electron degradation at a range of temperatures, and to use this data in our future flight reliability models.

3.2 Design

The design of the Test Structures Chip includes isolated transistors and resistors and few building blocks for the analog section of the full ASIC. The specific device types are:

- Thin oxide PMOS and NMOS (1.8V) transistors: 6 types of various geometries
- Thick oxide NMOS (3.3V) transistors: 6 types of various geometries
- Thick oxide PMOS (3.3V) transistors: 6 types of various geometries
- Zero threshold NMOS (native 3.3V) transistors: 6 types of various geometries
- Resistors: low resistance poly, high resistance poly, Nwell, metal
- Dual 2.5V bandgap references
- Single-stage cascaded operational transimpedance amplifier
- Two-stage class AB amplifier with dual differential pair inputs
- Two-stage class AB amplifier with PFET folded cascade input
- Chopper-stabilized two-stage class AB amplifier
- 4-bit digital-to-analog converter to test the R2R design
- NFET 10x gain current source

- PFET 10x gain current source
- NFET/PFET 100x gain current source

3.3 Results

The test configuration for the Test Structures Chip is shown in Figure 1 with its test packaging and supporting test electronics board, all located on the cold plate in the test cryostat.

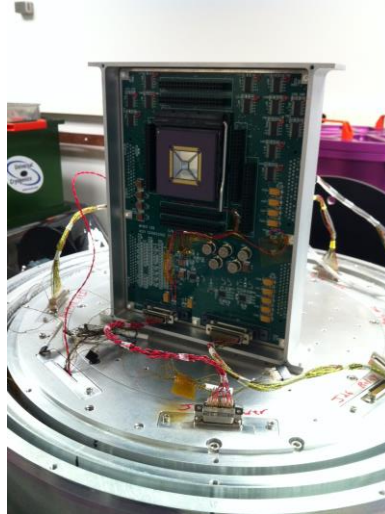


Figure 1. Test Structures Chip Test Configuration.

For basic transistor characterization, the $I_{DS}-V_{DS}$ and $I_{DS}-V_{GS}$ I/V curves were measured for each transistor type and geometry at 295 K, 200 K, 150 K, and 80 K. The measured curves were found to match the models provided by the foundry within 10% over the temperature range.

The DAC test circuit consists of a 4-bit R-2R ladder plus range selection bit, internal filter, and output amplifier that buffers the output for the 0 to 2 V range (non-inverting) or for the 2 to 4 V range (inverting). The 2 V reference used for testing the DAC was generated externally. The DAC circuitry was characterized for application as internal and external (detector) biases in the ASIC. The total noise (15 mHz – 100 kHz) on the DAC output between 0 to 2 V is 8.5 μV_{rms} at 295K and 4.8 μV_{rms} at 80K. Due to the inverting amplifier configuration with an additional feedback resistor in the upper range (2-4V), the noise is slightly higher. The DAC noise spectrum at 295 K and 80 K for the 0 to 2 V range and with internal CMOS filter capacitor switched on and off is shown in Figure 2. An instability driving capacitive loads in the 100 nF to 5 μF range was found in the DAC output amplifier. Programmable compensation capacitances in subsequent phases of the ASIC design controls this instability.

The CMOS bandgap reference was also characterized between 295 K and 80 K with noise and stability measured at the two temperature extremes. With an external 10 μF ceramic bypass capacitor on the unbuffered bandgap node, total noise (15 mHz – 100 kHz) on the buffered reference output is 5.8 μV_{rms} at 295 K and 5.0 μV_{rms} at 80 K. The reference is stable to +/- 45 ppm over a 200-hour period. The bandgap reference voltage over the operating temperature range is shown in Figure 3. A hysteresis in the voltage was discovered, where the voltage during cooldown is lower than when warming up. The behavior appears to be the result of a hysteresis in the strain induced on the silicon by the epoxy used to bond the silicon to the ceramic package⁵. The magnitude of the voltage hysteresis is a function of the local minima and maxima temperatures that the device has been exposed to. For a 295 to 80 K swing, the hysteresis amplitude is 5 mV; 2 mV for a 115 K swing; and undetectable for a +/- 10 K temperature swing around a fixed operating temperature. At a stable temperature, there is no settling or transition between the two curves in the hysteresis plot. Initially, the bandgap reference displayed a cold-start anomaly where it would not turn on at temperatures below 150 K, even when pulled up externally to try and jump start the circuit. The second spin of the test structures chip solved this issue with an internal “jump-start” bypass transistor that enables the bandgap reference to turn on consistently down to the lowest tested temperature of 80 K.

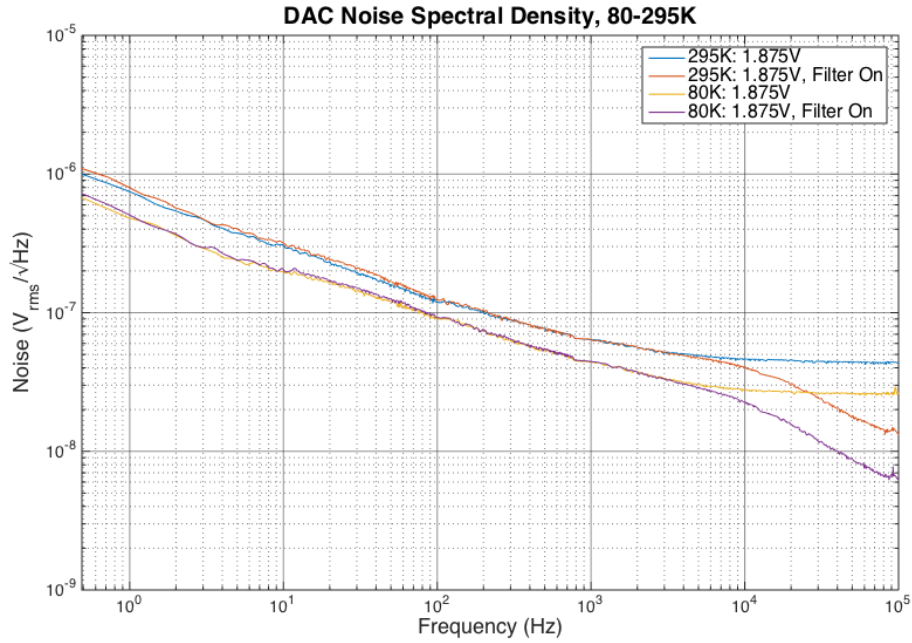


Figure 2. DAC noise spectral density in the 0 to 2 V range at 295 K and 80 K with the internal CMOS filter capacitor switched on and off.

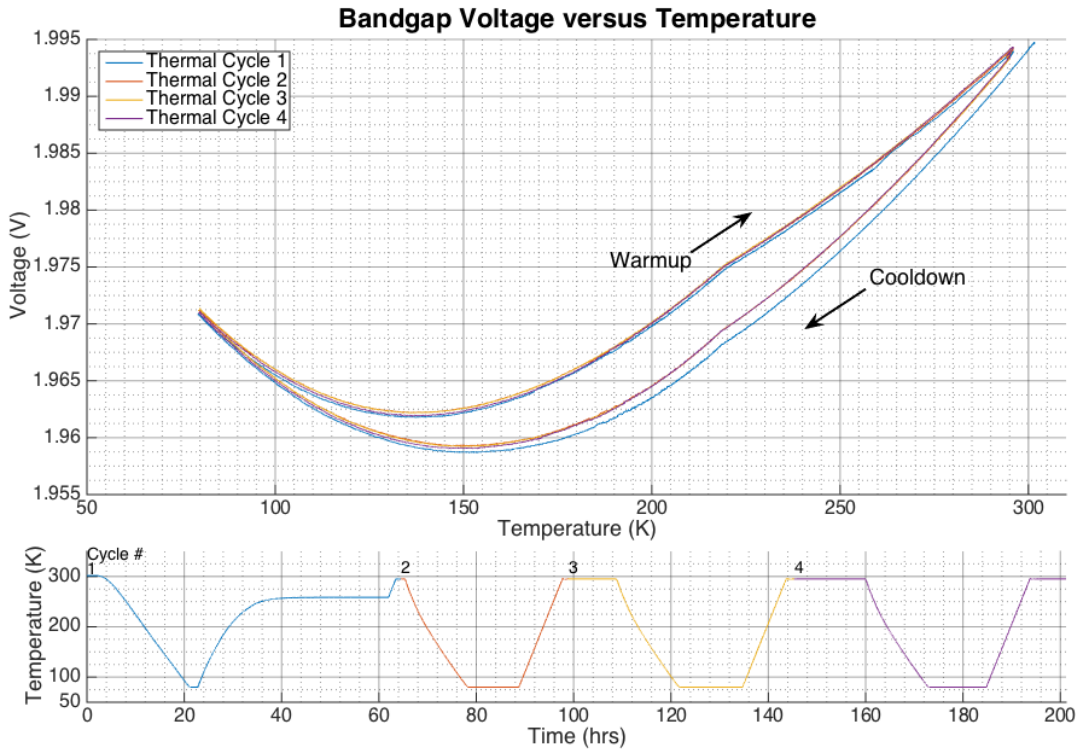


Figure 3. Bandgap reference voltage during cool down (lower curve) and warm up (upper curve). The bandgap reference displays some hysteresis attributed to strain in the epoxy used in packaging the silicon die.

Cryogenic operability and performance of the current source and amplifiers were also measured. All performed well across the operating temperature range, with the current source displaying 160 pArms input referred noise at 295 K and 250 pArms at 80 K, while amplifiers demonstrated total noise from 4.7 μ Vrms to 6.5 μ Vrms at 295 K depending on topology and 5.1 μ Vrms to 6.2 μ Vrms noise at 80 K (bandwidth of 15 mHz to 100 kHz).

4. ADC TEST CHIP

4.1 Overview

The next phase focused on a demonstration of the analog-to-digital converter (ADC) design. This included the full analog front-end including signal routing with various preamp configurations. The intent is to create a cryogenic analog-to-digital data acquisition module that both validated the design for the full ASIC as well as providing a potentially useful device for other purposes.

The first version of the ADC Test Chip was largely successful but resulted in a device with three identified shortcomings.

1. Power dissipation was higher than expected because of a communication problem with the foundry on the type of resistive ladder to use.
2. A differential nonlinearity problem (sporadic code-dependent glitches) that was traced to a race condition.
3. A strong nonlinearity at the very end of the conversion range that was traced to a logic error.

These shortcomings as well as some minor optimizations were addressed in the final design.

A second version of the ADC Test Chip will be created after the tape-out of the full ASIC to provide the fully functional device as a smaller-scale test platform for the ADC conversion function. Design features in the ADC Test Chip allow for more complete probing of the internal function of the ADCs compared with the more embedded implementation for the full ASIC.

4.2 Design

The ADC Test Chip implements an 8-channel data conversion system with selectable resistive or capacitive preamplifiers. Control uses a simple SPI interface to read and write internal registers. The 8 ADC outputs are multiplexed into a 16-bit parallel bus. The configuration registers and timing generators are much more flexible than would be required or desirable for the full ASIC design but the intent here is to be able to adjust almost all the timing parameters to help understand how to optimize the design. Figure 4 shows the ADC Test Chip block diagram and the floor plan of the die.

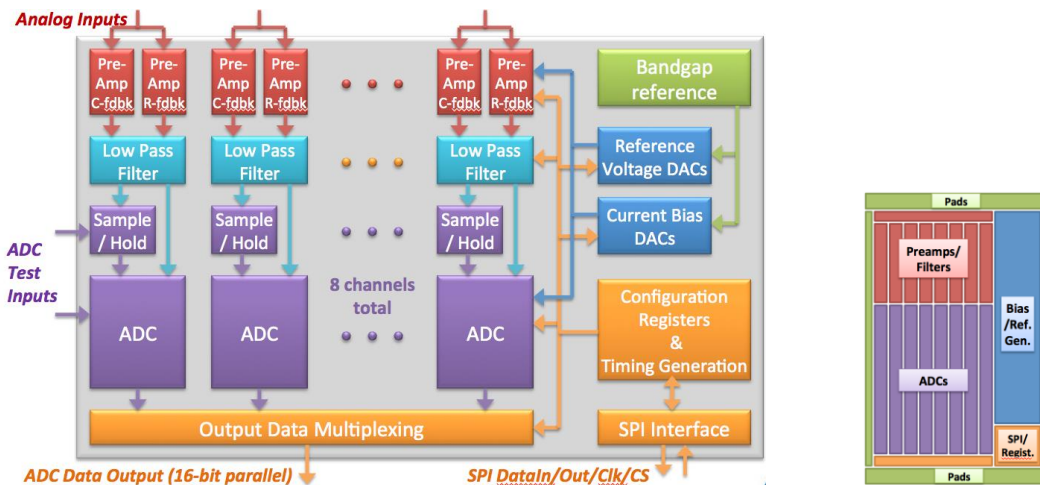


Figure 4. ADC Test Chip Block Diagram and Floorplan.

The requirements for the ADC are based on the requirements for the full ASIC design as captured above. The key ADC-level requirements are summarized in Table 1.

Table 1. ADC Key Requirements.

Parameter	Units	Specification	Measured (@100 Ksps)	Comments
ADC Resolution	bits	16	16	Up to 2 Msps min.
Noise	bits	< 1	0.75	
Differential Nonlinearity (DNL)	bits	< +/- 0.5	+1.5/-1	High DNL due to clock race condition in ADC timing.
Integral Nonlinearity (INL)	bits	< +/- 2	+/- 3 (295K) +/- 6.5 (80K)	
Power (per ADC @ 100 kHz)	mW	< 3	4 (295K) 12 (80K)	The large measured value is related to the fabrication error in the resistor ladder which is expected to be corrected in the next revision.
Power (per ADC @ 200 kHz)	mW	< 5		
Power Specification Temperature	K	< 140		
Maximum conversion speed (goal)	Msps	10		At 14-bit resolution.
Operating Temperature	K	80 to 300	80 to 300	
Pitch	μm	400		To fit into full ASIC floor plan.

A configurable preamp section provides signal conditioning of the detector video signals before digitization. Its purpose is to provide gain, noise filtering, and sufficiently low impedance to drive the ADC. Two different preamp options are available for each channel: resistive feedback or capacitive feedback. When using the resistive feedback option, continuous mode operation is enabled that does not require any clocking or resetting. The amplifier can be configured as a single-ended, or fully differential, or instrumentation amplifier (two high impedance inputs). When using the capacitive feedback option, some clocking is required to perform periodic resets of the capacitive feedback network. A correlated double sampling mode is provided that removes possible kTC noise introduced by the amplifier reset. The capacitive feedback mode offers somewhat lower noise and higher linearity, but the resistive feedback mode is attractive due to its simplicity in operation (no clocking) and uninterrupted amplification (no reset).

A fully differential sample and hold amplifier (SHA) has been incorporated between the preamp and the ADC to condition the preamp output for the ADC. The ADC has a large input capacitance and it requires the input to settle within a fraction of the cycle time. Since the preamplifier needs to gain up small detector signals, it has a high gain bandwidth product requirement, making it power-inefficient for driving the large ADC load. The unity-gain SHA efficiently drives the ADC and also helps to convert the preamp output common mode voltage to one that is better matched with the ADC input common mode requirement. The SHA also has a CDS mode where it can sequentially sample two inputs from the preamp and provide the difference to the ADC. This mode attenuates the low frequency correlated noise components such as the preamp kTC and 1/f noise.

The ADC is a multi-sample conversion architecture using a 2-step 5-bit flash conversion followed by an 8-bit successive approximation conversion. First the ADC samples the SHA output with a 5-bit flash stage to estimate the coarse range of the inputs (the 5 most significant bits, or MSBs) within the full-scale of the ADC. The ADC full scale can be programmed to be as large as +/- 2 V fully differential range (*i.e.*, a 4 V peak-to-peak single-ended range). Once the coarse-range is determined, this value is subtracted from the input and new references that are closer to the input level

are generated for the flash. The flash re-samples this first residue and does a fine conversion within this smaller range, again subtracting this conversion from first residue to create the second step residue. Once this two-step flash conversion is over, the second step residue is re-sampled by an 8-bit successive approximation register (SAR) ADC stage. This stage gets an even finer reference, within a few mV of the input level, in order to determine the 8 LSBs of the 16-bit ADC. This stage takes 8 cycles to successively approximate the 8 bits, starting from the MSB, down to the LSB. Once the SAR conversion is over, the two 5-bit flash outputs and the 8 bit output from the SAR (total of 18 bits) are provided to a digital error correction block. This block uses the inherent overlap in the stages and generates the final 16 bits that are immune to each stage's saturation effects due to noise, offset, charge injection, or other causes. Effectively, the ADC successively approximates the 16 bits in 10 cycles. There are additional cycles provided for sampling and settling. Due to ADC's higher internal clock rate, the ADC is provided a sample clock as well as a fast oversampling clock from the clock generator. In the test chip several of internal clocks are fully programmable for evaluating detailed circuit performance.

The architecture converts a differential voltage input to 16 bits in an extremely power-efficient manner. The ADC incorporates several programmable functions that make the architecture scalable. The ADC biases and references are fully programmable, since the bias block generates them. Its internal clocks are programmable. In addition, each circuit element in the ADC has programmable bandwidth and programmable swing. This allows the power dissipation to be optimized from rates as low as 100 kHz to those as high as several MHz. The power can be optimized for the chosen bit resolution as well as for the operating temperature. This can range from cryogenic to room temperatures. The test chip has demonstrated the highly scalable power-efficient ADC architecture to be fully functional. The test chip iteration is incorporating an improved design that will demonstrate the desired power dissipation as well as linearity performance.

4.3 Results

The ADC test chip was characterized in a cryostat identical to the one used for testing the Test Structures chip. Performance of the ADC, signal conditioning front-end, and internal biases, was measured at 295 K, 180 K, and 80 K. A custom test platform, the Analog Source Board (ASB), was used to provide low-noise biases, programmable linear ramps, and arbitrary waveforms that are multiplexed onto any combination of the differential ADC analog inputs. The ASB is located inside the shielded test cryostat to reduce environmental noise. The ADC performed well at all temperatures tested, meeting or approaching the performance requirements. It should be noted that due to timing related issues discussed below, the ADC was not tested above 100 Ksps. The confirmed ADC performance characteristics are listed in Table 1.

Using the capacitive preamps configured with a gain of 16, the total input-referred noise is 8.5 μV rms at 295 K and 9.2 μV rms at 80 K (0.1 Hz to 160 kHz bandwidth). Using the resistive preamps with a gain of 16, the total input-referred noise is 12.5 μV rms at 295 K and 16.1 μV rms at 80 K over the same bandwidth. Using a per-sample correlated double sampling (CDS) mode in the sample and hold amplifier and an internal reference, we demonstrated removal of kTC reset noise and low frequency 1/f noise in the capacitive preamp, even at room temperature. The total input-referred noise with a gain of 16 in the capacitive preamps and the sample-and-hold amplifier in CDS mode is 7.6 μV rms at 295 K. There is a penalty as the bandwidth of the front-end needs to be doubled, but for 100 or 200 kHz operation this is a reasonable trade. Figure 5 shows images compiled of a single ADC channel readout using the capacitive preamp to sample a static reference at 100 Ksps and resetting the capacitors every 1024 samples due to the large drift in the capacitive preamps at room temperature. The image on the right uses CDS against an internal reference for every sample, while the image on the left is direct sampling. There is no post-processing on either image.

The biases derived by 12-bit DACs from the internal bandgap reference, intended for internal ADC operation and biasing the detector, perform well across the required temperature range. The biases have a total noise of 8.7 μVrms at 295 K and 6.8 μVrms at 80 K (0.1 Hz to 160 kHz bandwidth) and are stable driving capacitive loads. The 12-bit DACs span from 0 V to 3.3 V (V_{DDA}) and demonstrate a DNL $< \pm 0.5$ LSB and INL $< \pm 3$ LSB.

There are some shortcomings in the device performance that were identified during testing, all of which have been evaluated, reproduced in simulation, and corrected in the full ASIC design (and the ADC Test Chip respin). Power dissipation of the ADC is higher than anticipated, and increases by a factor of 3 at 80 K (See Table 1). This was due to a communication error with the foundry where silicided polysilicon was used in the ADC flash resistor ladder instead of non-silicided polysilicon. The silicided poly has a large temperature coefficient, while the resistance of the non-silicided poly is relatively stable with temperature. This results in the increased power dissipation that we measured as the device

cools. Additionally, the nominal resistance of the silicided poly resistor ladder was lower than designed, causing higher than expected power dissipation even at room temperature.

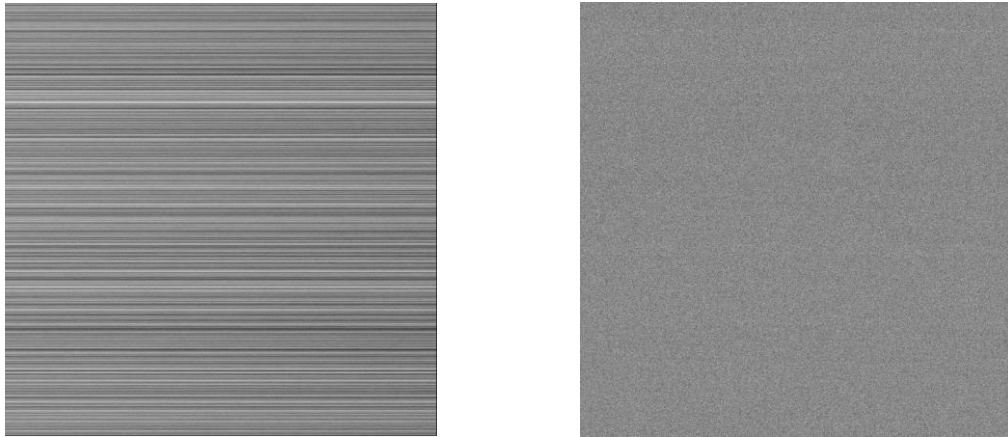


Figure 5. Direct sampling of a static bias using the capacitive preamp with reset every 1024 samples (left), sampling of the same bias using the capacitive preamp with reset every 1024 samples with correlated double sampling (CDS) performed in the sample and hold amplifier (right), both at 295 K. The per-sample CDS removes both kTC reset noise and drift in the capacitive preamp.

A second issue discovered during testing is sporadic code-dependent errors. These “glitches” were traced to parasitic capacitance on key clock signals producing a race condition in the SAR portion of the ADC. The result is a pile-up of codes near the ADC decision points, as can be seen in Figure 6. These glitches can be minimized in local regions of the ADC range through fine adjustments of the internal clock edges, but under most conditions the glitches cannot be tuned out over the entire span of the ADC. Because the root cause is understood, these code-dependent glitches were excluded when characterizing the noise and linearity of the ADC.

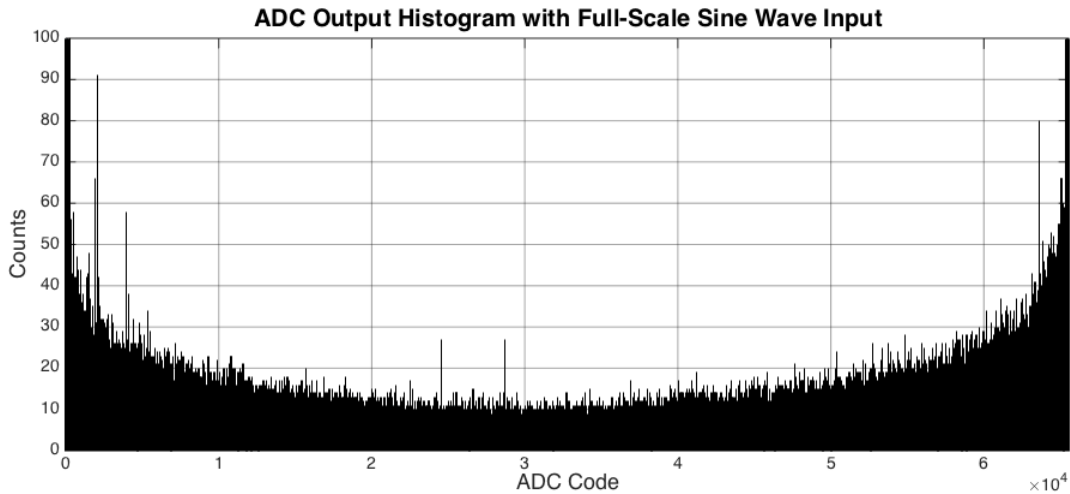


Figure 6. Histogram of ADC output codes with an overdriven sine wave input showing ADC code-dependent DNL glitches.

Another DNL issue was found to occur in the 256 codes at the two extremes of the ADC range. To achieve a full 4.0 V conversion range, these regions of the ADC are treated separately as a special case. Testing uncovered an error in the decision logic used for these top and bottom 256 codes, which is now understood and has been corrected. Our testing also identified several features in linearity, biasing, clocking, and debugging where we have been able to understand

limitations and adjust the circuit design to improve the analog performance of the ASIC. Having the opportunity to characterize and understand the standalone analog performance of the ADC, preamps, and biases and to fold that feedback into the full ASIC design should prove beneficial for the performance for the final full ASIC.

5. FULL ASIC

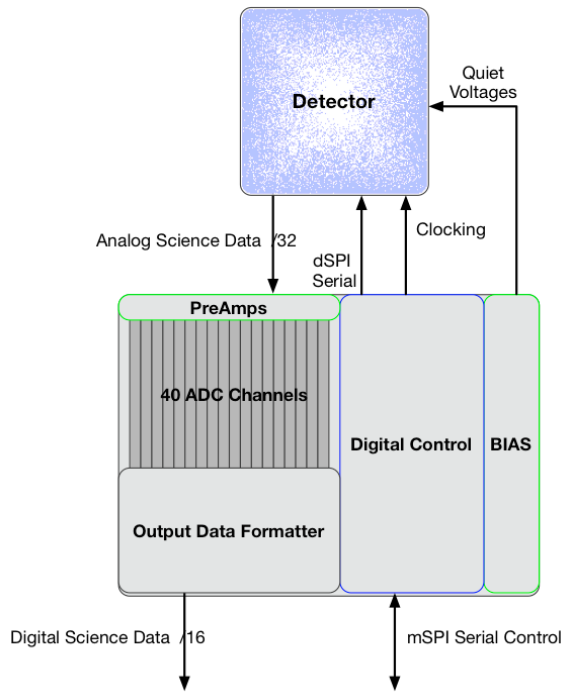
5.1 Overview

The full ASIC architecture was established in parallel during the previous phases of work. In particular, the design of the digital logic was taking place and the selection/implementation of the microcontroller was completed. For the final phase of development, the mixed-signal aspects of the design were finalized and the full ASIC layout completed. This is intended to be the first iteration design for the full ASIC. The Project schedule allows for at least one respin after extensive testing is completed before entering the flight production phase. We intend to hold the majority of the wafers from this first lot before metal processing in case minor adjustments are necessary after initial testing.

The key design drivers for the ASIC are to provide consistency, repeatability, and accuracy in detector timing control and conversion operations.

5.2 Design

The interfaces for the ASIC are shown in Figure 7. A generic detector at the top of the figure requires bias voltages and clocks to operate. The detector also produces analog data that will be digitized by the ASIC.



Feature	Design Intent
mSPI Serial Control	Primary control interface for the warm electronics. Provides ASIC memory and register access.
Clocking	Digital control of the detector from the pattern generator.
dSPI Serial Control	Detector configuration.
Quiet Voltages	Up to 24 biases provided to the detector.
Analog Science Data	32 channels plus 8 housekeeping.
Digital Science Data	Up to 16 LVDS outputs to the warm electronics.

Figure 7. ASIC Interface Diagram.

The block diagram of the full ASIC is shown in Figure 8. We briefly describe each of the blocks in the design, starting on the right side with the digital elements.

Basic operation is controlled by the mSPI interface working in concert with the ASIC internal Sequencer. For most applications, programming the Sequencer (loading up the EXEC and PGEN memories) provides sufficient control. The Sequencer controls a bank of biases and Detector Control (clock) Outputs directly through configuration registers and the Pattern Generator.

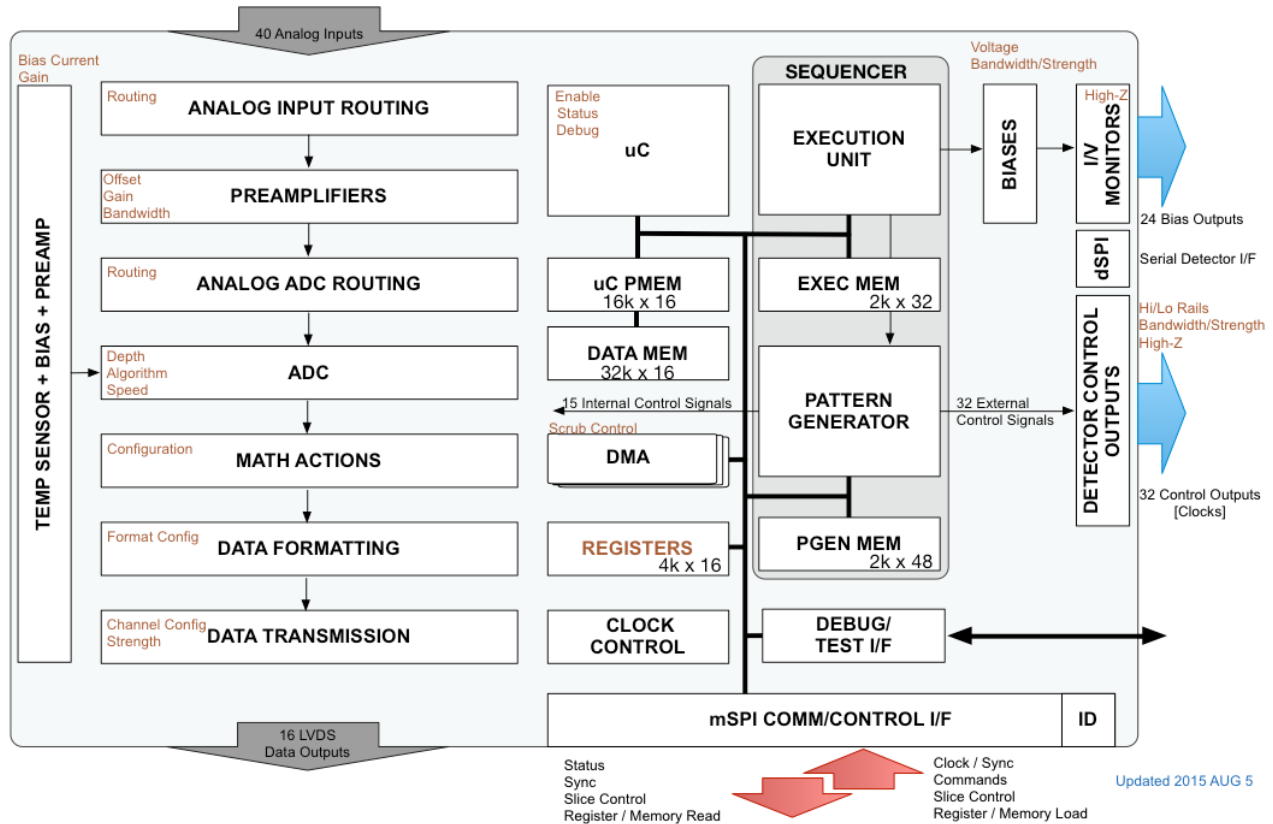


Figure 8. ASIC Block Diagram.

When the Sequencer provides sufficient flexibility for the application, the embedded microcontroller, based on an open source msp430 design, can be disabled. For more complicated applications, the microcontroller provides additional control functions through its ability to read and write all configuration registers and memories using direct memory access (DMA) design. The DMA controller can also provide automatic data scrubbing for the on-chip dynamic memories. The configuration registers are constructed from radiation-hardened designs for the basic flip-flops. All memories are protected from single-event upsets by error correction logic. One of the more challenging features of this architecture is to support deterministic multi-port access to these elements. The multi-port arbitration logic is configurable to provide flexibility as well as supporting debugging.

The state of the ASIC is monitored by 128 status bits, which can be read by the microcontroller or the Sequencer, and provides a way of mapping specific conditions to a set of actions. This includes certain conditions within the Math Blocks that provide efficient detection of certain conditions (*e.g.*, signals reaching a certain threshold value).

Referring to the top left of Figure 8 (above), the analog inputs are routed to preamplifiers and then to a set of ADCs. The outputs of the ADCs go through basic Math Blocks that provide the ability to perform configurable processing of the ADC output streams (see below for a more detailed description). If desired, the microcontroller has the ability to examine the results of that processing. This feature can be used to implement elaborate readout schemes to take data-dependent readout control based on real-time pixel values. The Math Block outputs then go to a Data Formatter and are

then transmitted to the warm electronics. An on-board temperature sensor is also available to feed into the data stream as needed.

The ADCs are essentially the same implementation as on the ADC Test Chip except that clocking is optimized and ASIC Clock Control now drives the ADC conversion. This conversion is strobed by an internal control signal that is initiated by the Sequencer.

A key architectural feature is the ability to synchronize multiple ASICs. For example, one of the detectors being considered for WFIRST could provide as many as 64 outputs. At least two ASICs would be required to support this mode of operation, and this can be accommodated by design. The “Slice Control” signals in the mSPI provide the detailed synchronization features that enable using the resources in multiple ASICs in this manner.

A diagram of the floor plan is provided in Figure 9. The die size is approximately 20 mm x 16 mm and there are ~400 pads.

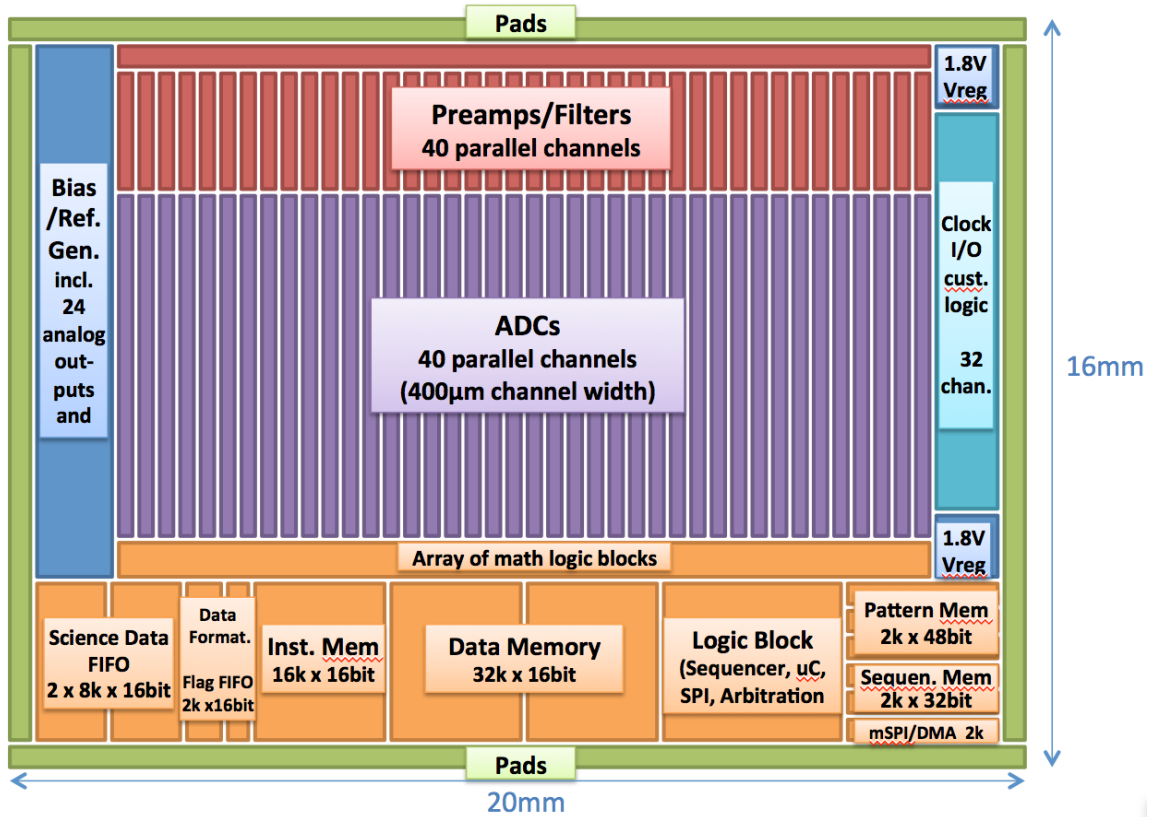


Figure 9. ASIC Floor Plan.

Compared to the ADC test chip, the preamp section has been enhanced with more linear switches and a flexible input signal routing network that supports a variety of configurable signal connections between different channels. In addition, programmable current sources have been included in each analog input pad that can act as source follower loads for buffered output operation of the ROIC video outputs.

The 12-bit DACs in the bias generator have also been improved over those in the ADC test chip by adding a second buffer amplifier that can optionally be used instead of the primary buffer. The second buffer offers lower output impedance and higher current drive at the cost of slightly increased noise.

Based on the desire to react to certain signal conditions in real time (*e.g.* resetting of saturated pixels during the acquisition ramp), special per channel Math Blocks have been included. Each block has the capability to add, multiply, shift, and compare the ADC data with configurable parameters, and to provide the collected comparison results to the microcontroller (or external user) in a time-efficient manner. Further action can then be taken to reset or otherwise manipulate the corresponding pixels in the detector.

Transmission of science data from the ASIC to the external electronics is carried out through a configurable digital interface that can use a configurable number of signals (1, 4, 8, 16, or 32), and that sends out science data in packetized form. Data from all enabled ADC channels is combined into a FIFO (First In – First Out) memory before transmission, and then all data is sent through the same interface. Collection of data from the ADC/Math Block outputs is controlled by the Data Gatherer, which sequentially inserts the ADC values into the science data FIFO. On the other end of the FIFO, the Data Formatter picks up the science data and generates the transfer block according to the selected interface mode. In addition to science data, the data block also contains customizable header information (*e.g.* telemetry) and a checksum at the end.

5.3 Results

As of this conference date (July 2016), the full ASIC design tape-out is anticipated to complete and the silicon manufacturing started. Our test plan projects that by the end of 2016, we will have the first test results from the full ASIC hardware.

6. TEST SUPPORT EQUIPMENT

6.1 Test Electronics

For the Test Structures Chip, we designed and implemented a custom cryogenic test card that interfaced to standard test equipment in the lab. The cryogenic test card and die packaging implemented Kelvin connections up to the silicon wire bond on all critical signal paths, allowing us to probe the different test structures using a large set of switches and use standard equipment to make the automated measurements (*e.g.*, I/V curves). The buffer amplifiers were also switched so we could change input and output configurations. The band gap references, DAC, and current sources had different load configurations that could also be selected during testing. Outputs for noise characterization were buffered and amplified by low-noise preamps on a second electronics card mounted inside the cryostat to minimize the effects of environmental noise.

For the ADC Test Chip, a custom test platform, the Analog Source Board (ASB), was mounted inside the cryostat to supply test stimulus to the ADC. The ASB includes 5 buffered and filtered 16-bit DACs for generating low-noise static biases, 2 20-bit DACs for generating ramps and arbitrary waveforms from look-up table memory in the warm electronics, and 2 coaxial inputs for analog pass-through from external instruments such as a low-distortion function generator. All of the generated signals can be multiplexed onto any combination of ADC channels or used to override internal ADC biases and references.

In planning for the infrastructure we would use to test the more integrated hardware, we settled on a test configuration that uses an interface we already have for reading out our imaging detectors. The warm electronics are based on the Markury Scientific Multi-ASIC Control Electronics (consisting of a MAICE and an ACE board), which are in general use in our labs at the NASA Goddard Space Flight Center for detector testing. A change of firmware is required to adapt to the test article, as well as to control the ASBs that provide the stimulus for the device under test.

6.2 Electronics Test Cryostats

One problem we have often faced in developing cryogenic electronics is having a cryostat that provides a convenient infrastructure to support the testing. Our standard cryostats for testing detectors are designed for testing under more static conditions than is desirable when trying to characterize electronics over a large temperature range.

We designed and built two identical cryostats with Universal Cryogenics in Tucson, AZ. They are cooled using single-stage Sumitomo RDK-400B cold heads. The closed-cycle system allows for very flexible operation at a wide range of temperature, from room temperature down to well below 80K, our minimum test temperature requirement. To allow for extremely low noise measurements, the cryostats are also outfitted with a liquid Nitrogen (LN2) cooling feature, where,

for short periods of time and with LN₂ flow-through, it is possible to maintain a cold operating temperature while turning off the mechanical cooling system.

The cryostats incorporate 8 ports for electrical interconnects. It is prewired for up to 150 differential signals for the test application. There are another 50 single-ended lines for power and relay control, as well as 99 single-ended lines dedicated to housekeeping and temperature control. This configuration is adequate for all the required testing.

There are two cryostats because we anticipated the need for parallel testing of different parts. For Phases 1 and 2, the two cryostats each held a Test Structures Chip and an ADC Test Chip. As we transition to the full ASIC, they will be configured for the ADC Test Chip and the full ASIC. Eventually, after development is complete and we enter the flight phase, they will both be used for the full ASIC. Figure 10 shows an exterior and interior view of these cryostats.

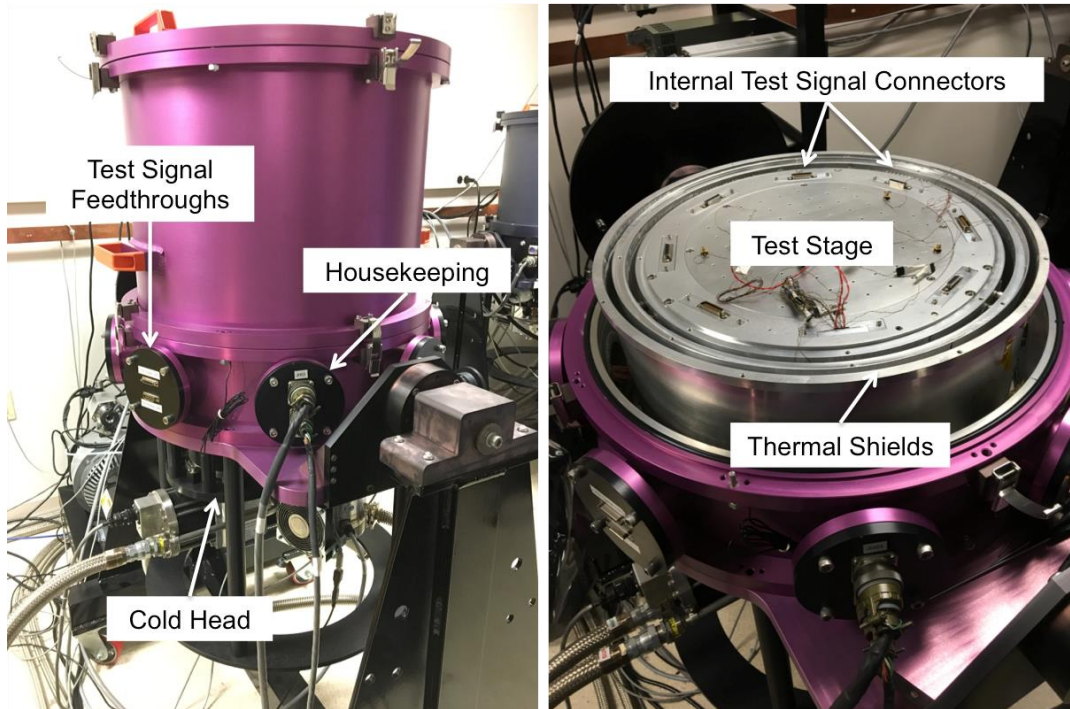


Figure 10. Electronics Test Cryostat Exterior and Interior Test Volume.

6.3 Cold Probe Station

Another problem that has plagued cryogenic electronics in the past is the inability to perform probe testing at or near the intended operating temperature. Most vendors and facilities take the strategy of room temperature probing, followed by die selection and packaging, and then the first cold testing on the packaged parts. The efficiency of this process depends on the yield going from warm to cold. This could be a major cost impact since rejected parts still need to be packaged before testing.

For this project we have constructed a cold probe station so that we can perform wafer-level testing at the intended operating temperature. This custom device is designed for use on up to 8" wafers (with expansion to 12" possible), and is cooled by a LN₂ flow-through system to avoid vibrations that could affect the precision motion stages. A high-resolution visible camera helps with alignment of the probe card to the die. Precision positioning of the probe card (in all axes and rotations) is controlled by a hexapod stage. Wiring from the probe card to the warm test electronics supports the ~400 pins for the full ASIC.

As of this conference, the cold probe station is starting its initial qualification tests using a dummy wafer and probe card designed to closely emulate the full ASIC configuration.

7. PACKAGING

For initial testing, the ASIC die will be packaged on an aluminum nitride fan out board that will be wire bonded to a standard PCB. The fan out board and an Invar baseplate serve mainly as the mechanical, thermal, and electrical interface between the silicon die and the standard PCB in order to accommodate the coefficient of thermal expansion mismatch and also match the supportable wire bond pitches. This is similar to what was previously done with the two test chip configurations (see Figure 11). The packaging will be performed at the NASA Goddard Space Flight Center Detector Development Laboratory (GSFC DDL), which has extensive experience with cryogenic packaging for sensor systems. The resulting PCB will be tested in the custom electronics test cryostat with the test electronics.

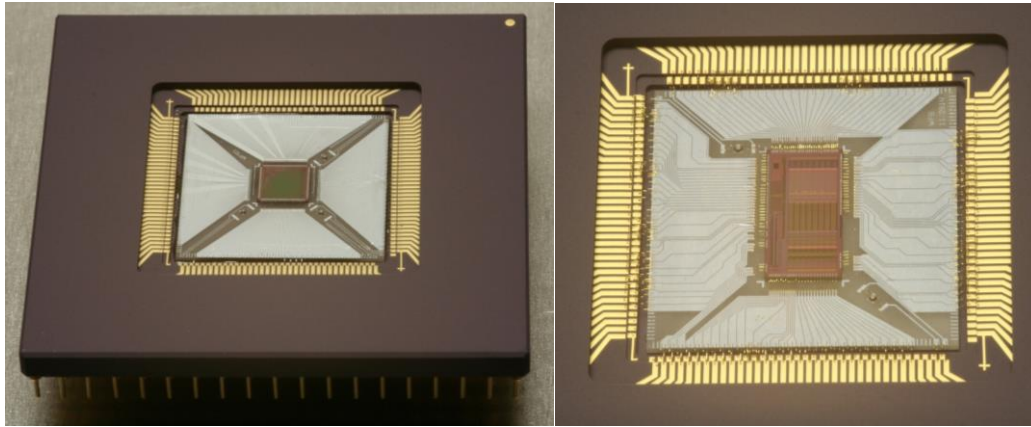


Figure 11. Test Packaging for the Test Structures Chip (left) and ADC Test Chip (right). Silicon die is epoxy bonded to an aluminum nitride fanout board, which is bonded into the cavity of a 280-pin ceramic PGA package.

For flight, the ASIC die will be packaged in a custom, hermetically sealed LGA ceramic package that will be attached to a flight PCB using solder columns. This packaging approach has been validated on previous missions^{6,7} and has been adapted for cryogenic operation by an earlier WFIRST activity and used for the ESA Euclid Near Infrared Spectrophotometer (NISP) instrument⁸. Our development team is designing the custom ceramic package in collaboration with the vendor, Kyocera. While initial packaging of the die can take place at the DDL, we anticipate using a commercial vendor for the flight parts to implement the Class K hybrid packaging requirements in volume. We anticipate that WFIRST will need approximately 45 flight-qualified parts.

8. LESSONS LEARNED AND COMPLETION PLAN

The development of this device has been a rewarding challenge for our small and dedicated team. During this work, several key points required a major concentration of effort.

While the goals for this device have been clear from the beginning, the formalization of these requirements took significant effort. In one sense, we knew too much. The user community that we consulted for these requirements included the NASA GSFC Detector Characterization Laboratory (DCL), which has experience with a wide range of detector technologies and implementation approaches. The harmonization of the collective needs and ambitions of this community was a continual work in progress, leading to some degree of requirements creep as the project moved forward. In the end, we believe that the architecture supports the guiding principles expressed above, and will result in a device that will serve the community well.

Some of these choices and desires are relatively straightforward. Items such as the type of preamps to implement (resistive or capacitive), and whether/how to implement a built-in correlated double-sampling (CDS) feature, can be

addressed with modern CMOS design by implementing the choice in hardware, thus deferring the decision. Items such as the number of video channels/biases/clocks are decided by the immediate need for WFIRST, with support for synchronization features to facilitate operating multiple ASICs in parallel to provide more resources, if necessary.

A system architecture trade that required significant discussion is whether or not a microcontroller is needed. Because a driving desire is to provide a simple operating mode, this ASIC will drive almost any existing readout integrated circuit (ROIC) using a simple sequencer with a small instruction set (without using the microcontroller). The Sequencer alone satisfies Benchmarks I and II described above. The need to support Benchmark III drove the decision to incorporate the microcontroller. An additional benefit is that there is now the flexibility to address any design shortcomings or unanticipated needs. The microcontroller selected is an open source design with the necessary tools for supporting the device.

An unanticipated challenge was in the choice of tools for silicon layout. We initially selected a tool that we believed would satisfy our needs at a cost consistent with a technology development project. As the development progressed, it became apparent that even at the scale of the ADC Test Chip, several shortcomings were apparent. This was further complicated by the fact that there was a change in ownership for the tool developer in the middle of our work. The vendor's support has generally been helpful, but they too had a learning curve after this transition. After a significant delay, we secured leased access to more established tools, especially for the place-and-route and clock optimization functions, and were able to complete the design.

The development part of this project is nearly complete, and we are looking forward to having the full ASIC under test in the later part of 2016. After validating the silicon and implementing the flight packaging, we will undergo a qualification program for the hermetic microcircuit as well as at the cold electronics module (PCB) level. This qualification program will start about a year after delivery of the first silicon. At that point, we enter the flight build phase for the cold electronics module.

9. ACKNOWLEDGEMENTS

The development team thanks the WFIRST Project for their support and continued patience during this effort. Its early support for the need for this device, during the pre-formulation phase of the project, which was severely resource constrained, provided the impetus for assembling our team and creating this opportunity. We also thank the members of the NASA GSFC DCL for their comments and criticisms, which have led to a better and more optimized device. In particular, we appreciate the assistance from Augustyn Waczynski and Yiting Wen. Barry Starr provided excellent comments in his independent review of this work and this paper.

We note with profound sadness the passing of our dear friend and colleague, Gerry Luppino. His boundless energy, enthusiasm, and creativity have been lost to us and to our entire community. He will be sorely missed.

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