National Aeronautics and Space Administration

Open Source Radiation Hardened by Design Technology

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HAT: 4.7.c-E **TA:** 4 autonomous systems **TRL:** start 2 / finish 4

ICA PROJECT OVERVIEW

The proposed technology allows use of the latest microcircuit technology with lowest power and fastest speed, with minimal delay and engineering costs, through new Radiation Hardened by Design (RHBD) techniques that do not require extensive process characterization, technique evaluation and re-design at each Moore's Law generation. The separation of critical node groups is explicitly parameterized so it can be increased as microcircuit technologies shrink. The technology will be open access to radiation tolerant circuit vendors.

INNOVATION

This technology would enhance computation intensive applications such as autonomy, robotics, advanced sensor and tracking processes, as well as low power applications such as wireless sensor networks.

OUTCOME / RESULTS

- Simulation analysis indicates feasibility.
- Compact voting latch 65 nanometer test chip designed and submitted for fabrication - 7/2016

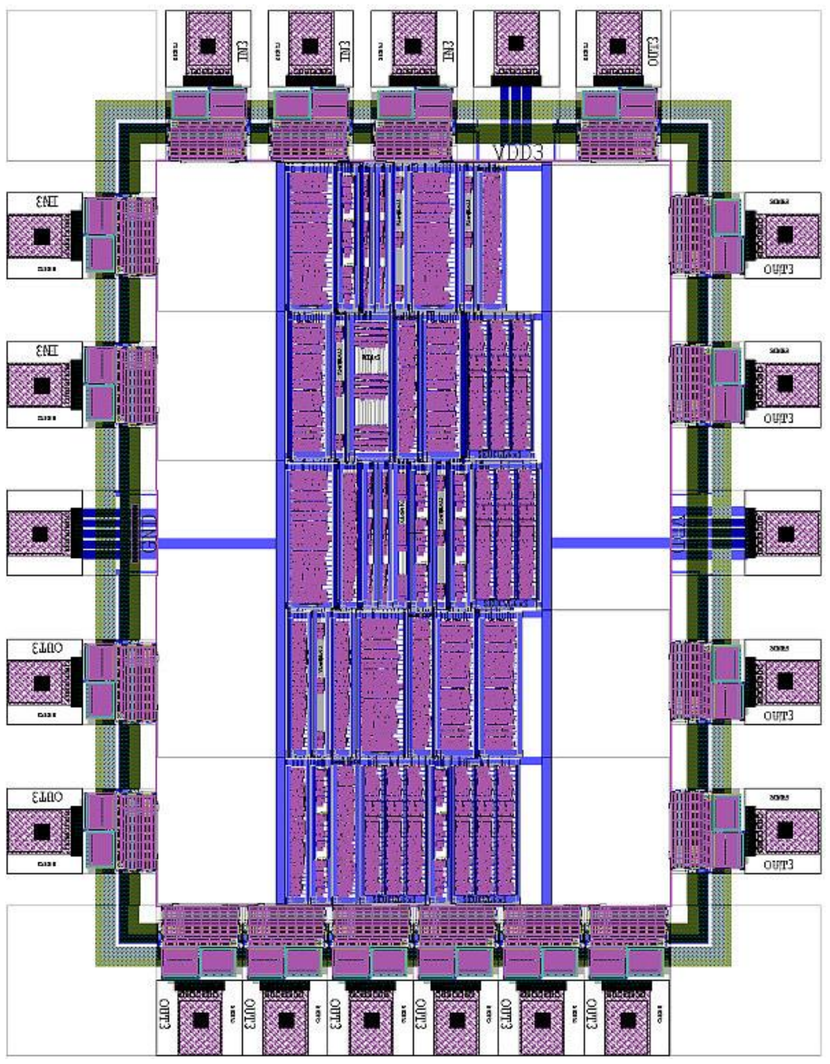
INFUSION FOR SPACE / EARTH

- This technology may be used in any digital integrated circuit in which a high level of resistance to Single Event Upsets is desired, and has the greatest benefit outside low earth orbit where cosmic rays are numerous.

PAPERS / PRESENTATIONS

"Porting and Scaling Strategies for Nanoscale CMOS RHBD," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, **62**, 12, pp. 2856 - 2863 (2015).

PICTURE OF ICA DEVELOPED PROTOTYPE



PARTNERSHIPS / COLLABORATIONS

The basic understanding of RHBD technology was acquired through long term collaborations with the University of New Mexico, University of Idaho and Vanderbilt University. The process expertise to design, simulate and fabricate nanoscale chips was acquired through collaborations with the University of Saskatchewan, including joint development of two 90 nanometer and one 65 nanometer test chips, the latter funded by a previous ICA grant.

FUTURE WORK

Test chips are expected 1/2017 and testing will be performed under a separate project