Experimental Durability Testing of 4H SiC JFET Integrated Circuit Technology at 727 °C

David Spry[1], Phil Neudeck[1], Liangyu Chen[2], Carl Chang[3], Dorothy Lukco[3], Glenn Beheim[1]

[1]NASA Glenn Research Center, 21000 Brookpark Road, M.S. 77-1, Cleveland, OH

[2]OAI, NASA Glenn, 21000 Brookpark Road, M.S. 77-1, Cleveland, OH

[3]Vantage Partners, LLC, NASA Glenn, 21000 Brookpark Road, M.S. 77-1, Cleveland, OH

Abstract

We have reported SiC integrated circuits (IC's) with two levels of metal interconnect that have demonstrated prolonged operation for thousands of hours at their intended peak ambient operational temperature of 500 °C [1, 2]. However, it is recognized that testing of semiconductor microelectronics at temperatures above their designed operating envelope is vital to qualification. Towards this end, we previously reported operation of a 4H-SiC JFET IC ring oscillator on an initial fast thermal ramp test through 727 °C [3]. However, this thermal ramp was not ended until a peak temperature of 880 °C (well beyond failure) was attained. Further experiments are necessary to better understand failure mechanisms and upper temperature limit of this extreme-temperature capable 4H-SiC IC technology.

Here we report on additional experimental testing of custom-packaged 4H-SiC JFET IC devices at temperatures above 500 °C. In one test, the temperature was ramped and then held at 727 °C, and the devices were periodically measured until electrical failure was observed. A 4H-SiC JFET on this chip electrically functioned with little change for around 25 hours at 727 °C before rapid increases in device resistance caused failure. In a second test, devices from our next generation 4H-SiC JFET ICs were ramped up and then held at 700 °C (which is below the maximum deposition temperature of the dielectrics). Three ring oscillators functioned for 8 hours at this temperature before degradation. In a third experiment, an alternative die attach of gold paste and package lid was used, and logic circuit operation was demonstrated for 143.5 hours at 700 °C.

1. Introduction

Space exploration, aeronautics, and energy production would benefit from integrated circuits (ICs) that could operate durably and reliably at temperatures as high as 500 °C [4-6]. Complex integrated circuits capable of operating at 500 °C, well beyond the limits of conventional silicon ICs, could enable uniquely capable smart sensors which could be directly placed without added cooling in turbine engine hot sections. Such enhanced sensing capabilities would allow for greater control of the combustion process, improved fuel efficiency, and better emission monitoring [4]. In space exploration, such electronics could be used for a long-term seismometer or weather station on the 460 °C surface of Venus or a deep atmospheric Jupiter probe [5]. In addition, such electronics could enable smart sensors for use in geothermal well drilling [6]. Previously, NASA Glenn Research Center has demonstrated long term 500° C operation of ICs with two levels of interconnects for thousands of hours using a 4H-silicon carbide (SiC) based junction field effect transistor (JFET) architecture [1, 2].

Customized ceramic packaging of ICs to endure 500° C operational testing is non-trivial, and testing for desired long operational durations (> 1000 hours) is time-consuming. In order to carry out accelerated age testing of 500 °C rated ICs, testing temperatures significantly higher than 500 °C are needed in order to more rapidly determine and understand durability/reliability limiting failure mechanisms. When there is a phase transition or change in physical properties of any of the materials used in the packaged ICs, that phase transition temperature dictates the practical upper temperature limit at which one can test. As described elsewhere [1], the SiC IC wafers are processed at 720° C for tens of hours during low-

pressure chemical vapor deposition (LPCVD) of stoichiometric silicon nitride and LPCVD of silicon dioxide using tetraethylorthosilicate (TEOS) precursor. The package, wires, and circuit boards are fired at 800 °C for many hours prior to chip die attach. In our initial report of $T \geq 700$ °C SiC JFET IC testing [3], chips were tested with a fast ramp (9 °C/min) to 877 °C. Discrete test devices on these chips (including a 3-stage ring oscillator) continued to work until 773 °C. We hypothesize that the majority of the extensive physical degradation noted in post-test inspection (including failed backside contact due to loss of platinum in the die attach paste) occurred after devices electrically failed as T exceeded 800 °C.

2. Experimental

In this study we conducted three further experiments. The first repeated the initial experiment of reference [3] with a chip diced from the same generation 8.1 4H-SiC JFET IC wafer, except the peak temperature was reduced to 720 °C. This was then followed by two similar additional experiments to peak T of 700 °C conducted on two chips diced from a newer 9.2 generation prototype 4H-SiC JFET IC wafer.

2.1 Nomenclature

The chip package used in the initial test (previously reported in reference [3]) was a pseudo-package of gold traces patterned on a sapphire substrate. All chips tested in this report were bonded into a new 32 pin ceramic package design described in [7]. The test numbers 6A2, 924, and 931 denote the three new experiments of this report that are summarized in Table 1. The fabrication of generation 8.1 chips as well as initial 500 °C electrical durability test results are described in references [1, 8], while corresponding documentation for generation 9.2 chips is presented in reference [2]. Both generations were fabricated with the same process sequence using the same lithographic masks, except for the following differences: (1) "gate notching" defects present in 8.1 JFETs were eliminated for 9.2 JFETs by reduced time delay and improved wafer storage between gate and mesa etches; (2) heavily-implanted SiC contact regions were formed using phosphorous implantation for 9.2 chips instead of nitrogen implantation used for 8.1 chips; (3) SiC ohmic contact for 9.2 chips was implemented using a 50 nm sputtered hafnium (Hf) layer instead of the 50 nm sputtered titanium (Ti) layer used for 8.1 chips; (4) the 9.2 process added a 67 nm Si_3N_4 layer between the top two SiO_2 passivation layers; and (5) extensive laboratory improvements to mitigate sodium contamination were implemented for 9.2 wafer processing.

Relevant experimental conditions for all three tests in this work are compared in Table I. While all three tests used the same 32-pin package design, it is important to note that different die attach processes were employed to bond chips into this package. Test 6A2 and 924 used the same lead oxide glass based Pt die attach paste and a 2-hour 500 °C cure as the reference [3] experiment, whereas 931 employed an Au-based paste (free of lead-oxide) and a 2-hour 600 °C cure. Furthermore, 931 also had a lid placed over the package during the oven-test; however, none of the packages were sealed. For all three tests, rates of heating and cooling were restricted to 3 °C/minute or less throughout the entire experiment. As shown in Table I, all three tests started with a 500 °C burn-in on the order of roughly 100 hours. The 931 chip was subjected directly to a ramp to 700 °C following burn-in while the chips for test 6A2 and 924 were cooled back to room temperature prior to ramping to peak testing temperature. A 727 °C peak test temperature was chosen for 6A2 because that was the failure temperature for the experiment reported in reference [3]. A test temperature of 700 °C was selected for the subsequent 924 experiment to determine if the migration of the lead oxide die attach paste would be less than that observed for 6A2. The same testing temperature of 700 °C was selected for 931 to compare the Au die attach paste against the lead oxide Pt die attach of 924. At maximum temperature, the chips were monitored periodically and the test concluded after failure of the last device.

2.2 Electrical testing

As reported in reference [9], the 4H-SiC JFET threshold voltages vary as a function of radial distance from wafer center, and also change slightly with device temperature. Therefore chip power supply voltages V_{SS} and V_{DD} were not the same for all tests, and were sometimes adjusted during the test to facilitate proper circuit operation. Chip backsides were always electrically biased to the V_{SS} negative power supply. Test 6A2 used V_{SS} = -20 V to -24 V for the burn-in which was adjusted to V_{SS} = -20V and V_{DD} = 20V for the ramp to peak temperature. For the entire duration of the tests, 924 used V_{SS} = -20V and V_{DD} = 25V, and test 931 employed V_{SS} = -25V and V_{DD} = 25V. Test 6A2 used a digitizing curve trace to measure the JFET and TLM devices, which provided for faster measurement cycles but poorer signal to noise quality than source-measure units that were used for tests 924 and 931. Logic gate and ring oscillator outputs drove 10 MΩ probes to

a digitizing oscilloscope. To facilitate uniform measurement and comparison of input voltage to output voltage transfer characteristics, all logic gate tests used input test voltages of 0V to -10V regardless of operational logic gate output voltages.

2.3 Test 6A2

Devices tested in 6A2 were as follows: a 4-input NOR gate, with inputs tied together to function as a 2-input NOR gate in order to test using fewer pulse generators; 4-input AND gate, inputs paired to function as 2-input AND; a discrete JFET of designed gate length $L_G = 6\mu m$ and gate width $W_G = 12\mu m$; a 0.5 mm^2 area metal-insulator-metal capacitor; a low frequency (LF) 3-stage ring oscillator; a Metal 1 to Metal 2 stitch pattern with 400 links; a Metal 1 to n-type 4H-SiC resistor stitch with 400 links; and two linear transmission line method (TLM) test structures for extraction of sheet resistance and specific contact resistivity. One TLM was patterned with n+ contact implant across the entire length of the device, while the other had n+ contact implant only in regions beneath the ohmic contact metal. A before-packaging image of the entire die of 6A2 is shown in figure 1(a), while the after testing image of the same die is shown in figure 1(b). The eight rectangular veneer structures in the middle of the die are alignment marks, and there are also small squares that are used as electrical test pads during processing. The three squares that are superimposed on the large capacitor near the right side of the die are mesas to test the effect of topology under the capacitor structure.

Test #	Design	Si$_3$N$_4$	Die Attach	Lid	Hrs @ 500 °C	# of Cycles	Test Temp °C	Hrs at Temp	Last Device Hrs
6A2	8.1	No	PbO$_x$ glass-Pt	No	94	2	727	45.45	27.45
924	9.2	Yes	PbO$_x$ glass-Pt	No	117	2	700	19.2	16.2
931	9.2	Yes	Au Paste	Yes	111	1	700	191.5	143.5

Table 1. Thermal history of tested die, design generation, and die attach used.

In figure 1(b) post-test image, after 45 hours at 727 °C, the lead oxide based die attach can be seen to have migrated in from the die edge to encompass all the bond pads, and in some areas it is observed to contact the device traces. There is a lot of debris on the chip surface and color changes of traces not encroached by die attach are also apparent. Figure 2 provides a more detailed look at the LF 3-stage ring oscillator (lower area of image, with output trace running
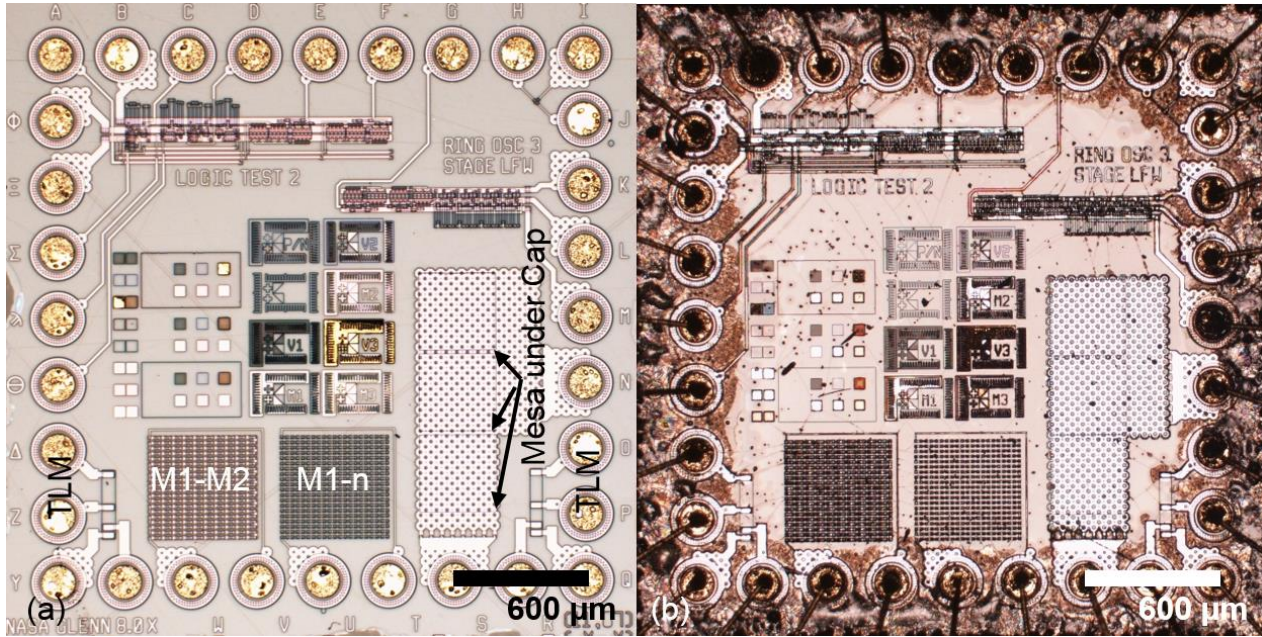

Figure 1. Optical micrograph sample 8.1-(11,7) test 6A2 before (a) and after (b) packaging and testing. Note where the lead oxide glass/platinum die attached has migrated to surround the bond pads. The small particles are debris fallout.
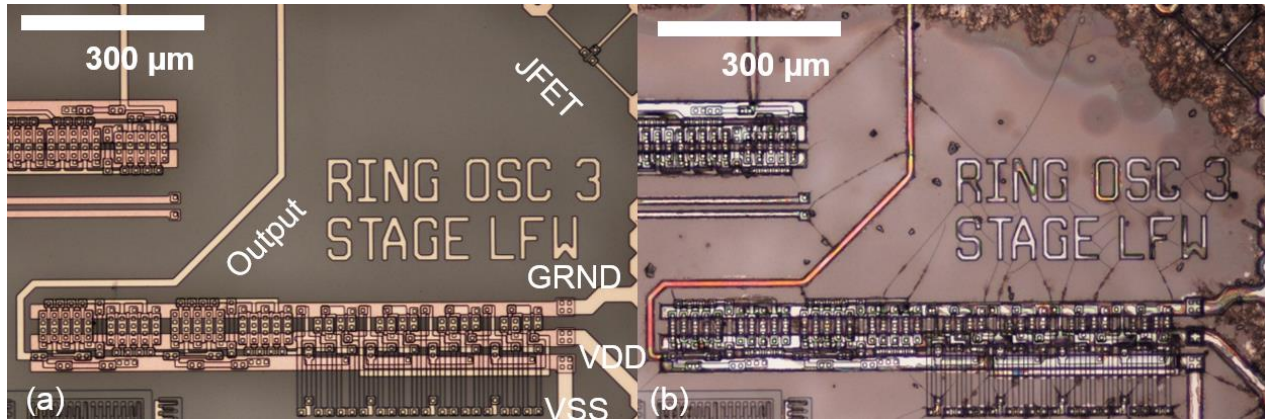
Figure 2. Optical micrograph of sample 8.1-11,7 test 6A2 before (a) and after (b) testing. Note the lead oxide glass/platinum die attach has migrated to surround the JFET in the upper right. There is also evidence of debris fallout and dielectric cracking. The output of the ring oscillator has changed color.

upwards off the top of the image) and JFET (upper right area of image) before (a) and after (b) the test. At this higher magnification, abundant cracks are evident in figure 2(b) after image. Note that the JFET in the upper right of figure 2(b) is completely covered in die attach. The oscillator output trace in figure 2(b) shows severe discoloration compared to its initial color in figure 2(a), and also compared to other metal traces (e.g., VSS, VDD, and GRND traces) in figure 2(b).

The electrical results for this test exhibited varying failure times. The NOR4 functioned for 60 hours and the AND4 functioned for 32 hours at 727 °C. The LF 3-stage ring oscillator failed prior to the beginning of the 727 °C test. Figure 3 plots key parameters of drain saturation current IDSS, drain-to-source resistance RDS, and off-state current IOFF extracted from JFET drain current-voltage (I-V) characteristics as a function of 727 °C testing time. The discrete JFET lasted 25 hours and was stable until sudden failure occurred, as seen in figure 3. The 0.5 mm^2 area metal-insulator-metal capacitor exhibited gradual leakage current increase from ~1-2 µA to 10-20 µA over the same 28 hours.

2.4 Test 924

Before discussing the behavior of 9.1 chips during 700 °C electrical tests 924 and 931, it is first necessary to discuss changes to the dielectric structure that occurred during processing of these chips. In order to minimize water
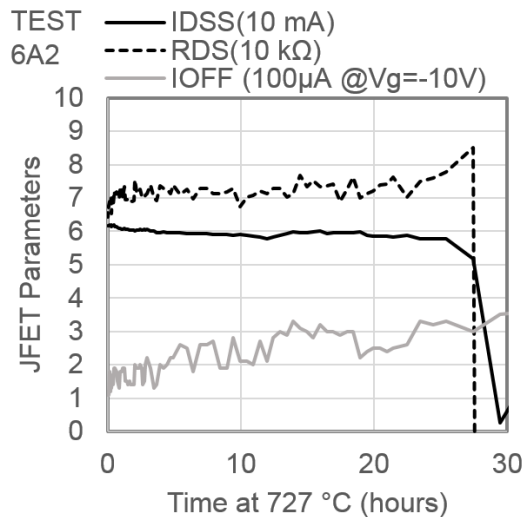

Figure 3. JFET parameters as a function of time. VSS=-20V and VDD=20V for test 6A2 during the 25 hours of operation at 727 ° C.
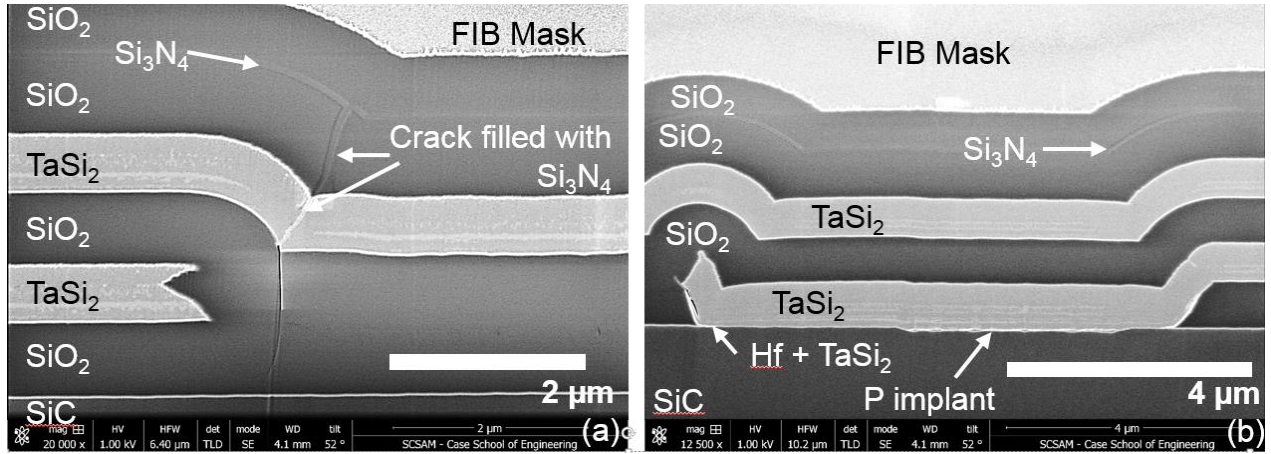
Figure 4. FESEM images of a FIB cross-section where a crack had developed during the temperature ramp of the stoichiometric LPCVD Si_3N_4 die (12, 11) (a) and a region of the same wafer (design version 9.2) where there was no cracking die (12,5) (b).

absorption into the SiO_2, stress-related cracking, and sodium contamination that all degraded the yield and durability of chips from wafer generation 8.1 [8], a 67nm thick Si_3N_4 layer was added between the third and fourth SiO_2 layers. While the thermal ramp rate was kept to 3 °C/min during the wafers ramp to 720 °C for the LPCVD Si_3N_4 deposition run, the ramp rate during boat-in was found to be greater than 30 °C/min, far above intended ramp rate limits. As a result, some places on the wafers had cracks form during the boat-in, and then fill with Si_3N_4 during deposition. Upon cooling, the Si_3N_4 held any $TaSi_2$ cracks together. An example of a resulting crack-filled dielectric structure is revealed by the field emission scanning electron microscopy (FESEM) cross-section shown in figure 4(a). Other regions of the wafer did not crack at all as seen in the figure 4(b) cross-sectional SEM image. Prior to 700 °C electrical testing, no Si_3N_4 filled cracks
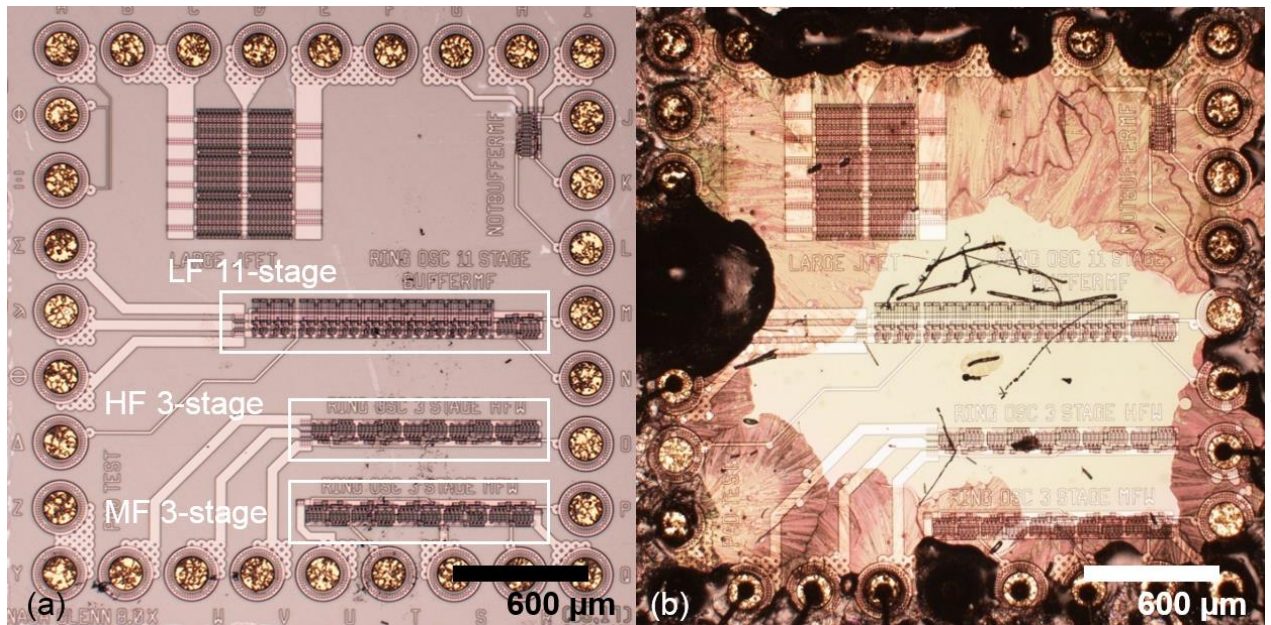

Figure 5. Optical micrograph sample 9.2-(9,17) test 924 before (a) and after (b) testing. Note the lead oxide glass/platinum die attach has migrated over most of the die and there is fibrous debris fallout.
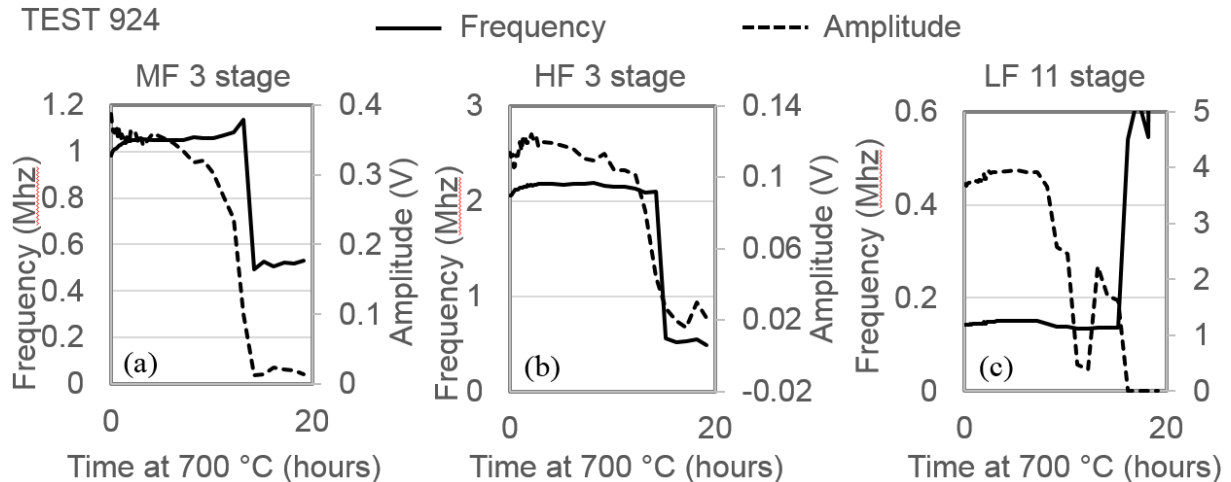
Figure 6. Plot of frequency and amplitude output of 3 different ring oscillator designs measured at 700 °C during test 924 with VSS=-20V and VDD=25V. (a) is a medium frequency 3-stage ring oscillator located at the bottom edge of the die, (b) is a high frequency 3 stage ring oscillator located between the other two devices, and (c) is a low frequency 11 stage ring oscillator located in the middle of the die; (b) lasted the longest possibly since it had the least lead oxide on it; (c) had an intermittent failure at 10 hours.

were observed in the field.   The Hf contact and the step resulting from the higher wet thermal oxidation rate of the phosphorus implant area can also be seen in figure 4(b).

Figure 5 (a) and (b) show chip images from before and after 700 °C electrical test 924. Despite the fact that this test was of shorter duration (19.2 hours) and lower temperature than test 6A2, the spreading of lead oxide die attach across the die's topside surface was the most severe. Some of the wire-bonds in figure 5(b) are completely engulfed in the die attach encroaching from the die edge. The chip also had some relatively large-fiber particle fallout from the oven. The only devices that were electrically biased during this test were the LF 11-stage, high frequency (HF) 3-stage, and the medium frequency (MF) 3-stage ring oscillators that are labeled in figure 5(a). The frequency and amplitude output, as functions of time at 700 °C, for all three ring oscillators are plotted in figure 6. All three oscillators started to show signs of electrical performance degradation at 8 hours. Although all three ring oscillators had their own bond pads for VSS, VDD, ground, and output, they shared power wires to the package in order to minimize the number of Au wires leaving the oven. Examination of the figure 6 failure data revealed that each oscillator demonstrated unique failure time and behavior, which indicates that the shared power wire was not the cause of failure. It is also important to note that dielectric cracking is not observable in figure 5(b).

2.5 Test 931

The most substantial change for this test was the use of Au paste, cured at 600 °C, instead of lead oxide glass based Pt die attach (designed for 500 °C applications), cured at 500 °C, and the use of an unsealed lid placed on the package to protect the chip from particle fallout. Figure 7 shows the before (a) and after (b) die images from test 931. In sharp contrast to 924 results shown in figure 5, the figure 7(b) after image shows no lead oxide glass migration or particle fallout. Despite the fact that 931 was tested at 700 °C for 10-times longer duration than the 924 chip, there is no visible evidence in figure 7(b) of die attach contamination around the edge of chip 931. However, the 931 chip did experience extensive crack formation. Figure 8 shows a higher magnification image of the top third of the 931 chip following 700 °C testing. While the intent was to test the NOR4 and AND4 circuits for more direct comparison with 6A2, a handling error resulted in a medium and a high frequency 2 input NOR gates (MFNOR and HFNOR) being wired instead.

An important feature to note in Figures 7 and 8 is the fact that some bond pads and traces appear nearly undamaged, significantly different from immediately neighboring similar features. In particular, note the figure 7(b) appearance of the three bond pads circled in figure 7(a). These bond pads are the V_{SS} bond pad on the logic test structures, the LF 3-stage ring oscillator, and the bond pad for the NOR4-AND4 input that was mistakenly not wired and seems to be
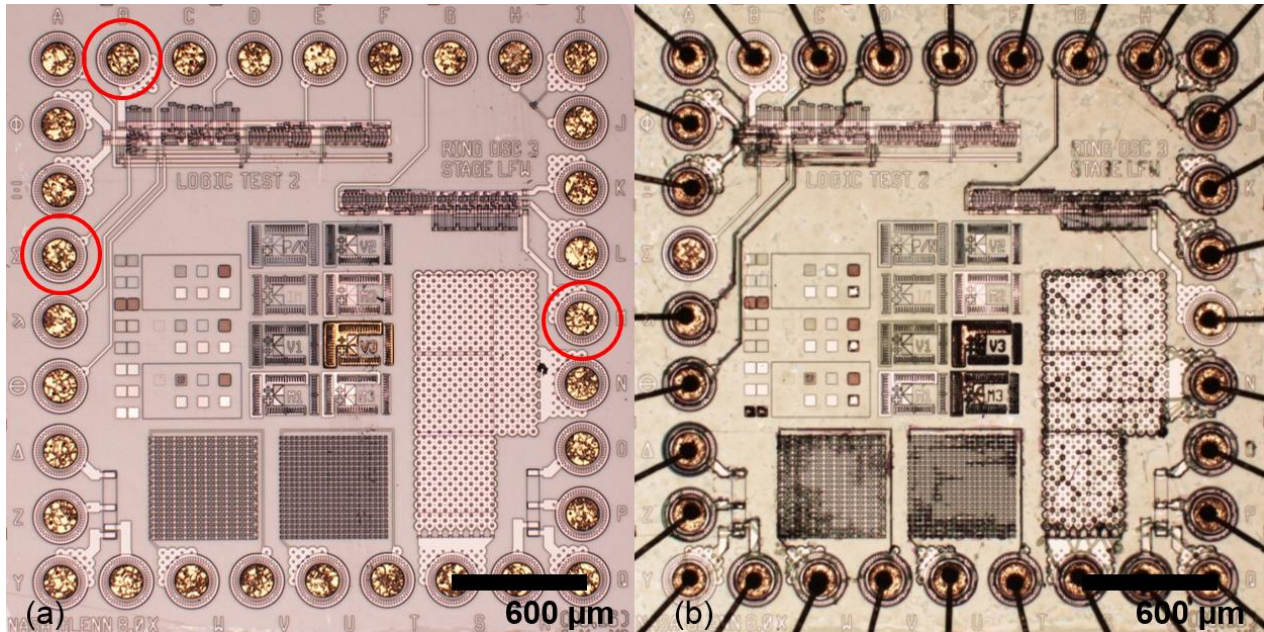
Figure 7. Optical micrograph sample 9.2-(8,16) test 931 before (a) and after (b) testing. Note there is no die attach migration or debris fallout since Au paste was used and lid covered the die. Only dielectric cracking and TaSi$_2$ oxidation are visible. Circle in red on image (a) are three bond pads that did not show any aging and only near other traces or device was there any cracking.

in nearly perfect shape after the test. During the test, the VSS pads were biased at the same potential as the underlying substrate, while the unwired NOR4-AND4 input was completely unbiased. These above observations provide evidence that electrical bias impacts physical degradation of circuit interconnects at these temperatures.

Close inspection of the figure 8 post-test MFNOR and HFNOR logic gates reveals that only the output traces running to the bond pads appear damaged, whereas the logic circuitry itself optically appears undamaged/unchanged. An even higher magnification optical microscope image of the discrete JFET is shown in figure 9(a). From this image, it is readily apparent that post-test metal discoloration corresponds to where cracks are present in the overlying dielectric. A dielectric crack over a TaSi$_2$ trace allows oxygen to reach and oxidize the top surface of the TaSi$_2$ interconnect. This is seen in cross-section in the figure 9b FESEM, which was focus ion beam (FIB) milled along the red line in figure 9a. It is
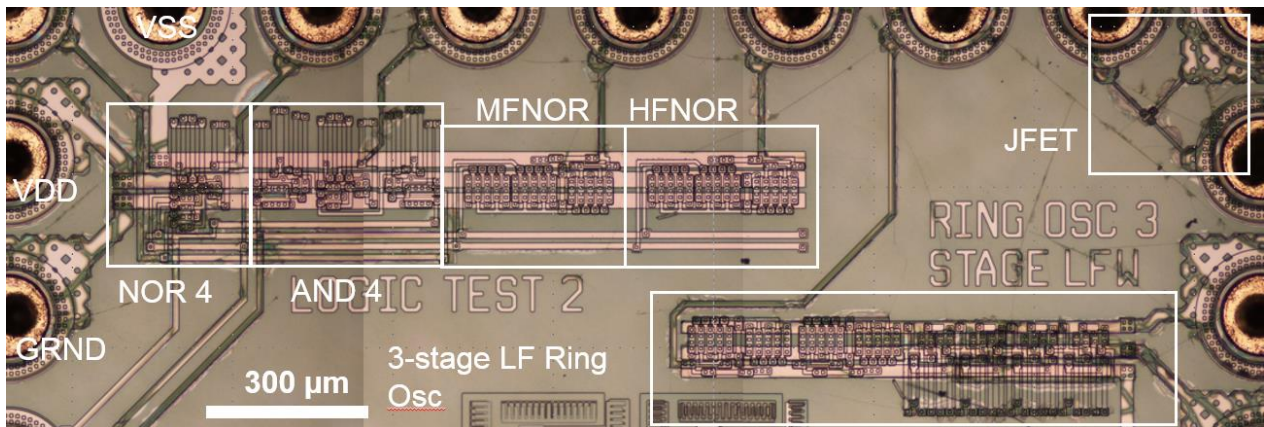

Figure 8. A higher magnification optical micrograph of the top part of die (8,16) in test 931 after electrical testing for 191.5 hours at 700 °C. Note the absence of die attach migration or debris fallout since Au paste was used and lid covered the die. Only dielectric cracking and TaSi$_2$ oxidation are evident. An even larger view of the JFET area can be seen in figure 9.
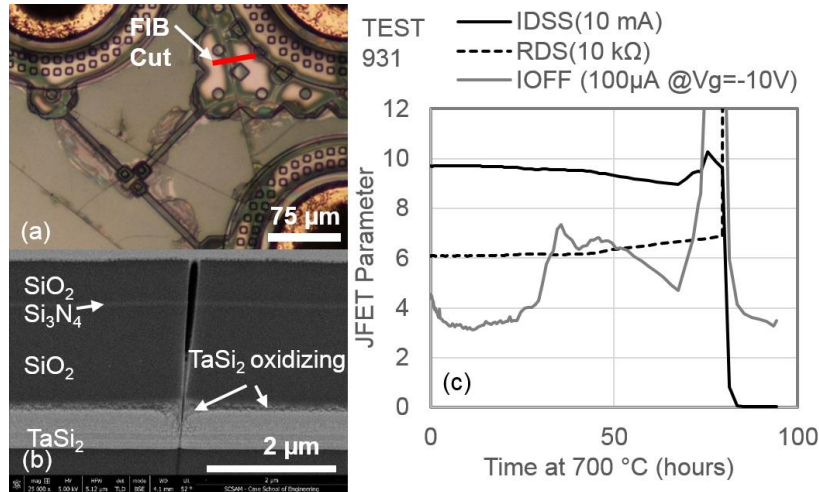
Figure 9. (a) Optical micrograph of the discrete JFET of test 931. (b) FESEM image of a FIB prepared cross-section of a crack. The crack allowed the TaSi$_2$ to oxidize. (c) JFET parameters as a function of time at 700 ℃.

important to note, however, that no correlation was observed between cracks that developed during 700 ℃ electrical testing and Si$_3$N$_4$ filled cracks formed by the wafer boat-in thermal ramp during processing. Our proposed interpretation of the observed crack patterns is that cracks initiated at larger-area power bus metal traces or bond pads, and then propagated into field regions from device to device.

Figures 9(c), 10, and 11 summarize the electrical results of the 931 test. Figure 9(c) shows the time evolution of key I$_{DSS}$, R$_{DS}$, and I$_{OFF}$ parameters for the W$_G$=12μm/L$_G$=6μm JFET shown in figure 9(a). In figure 9(c), the 931 JFET I$_{OFF}$ started to show drift at 23 hours (similar to 25 hours for the 6A2 JFET), but the device did not fail until 70 hours. Figure 10 shows the 700 ℃ test time evolution of the LF 3-stage ring oscillator frequency and amplitude output. This oscillator, similar to the three from test 924, also started to fail at 8 hours and its gradual failure behavior exhibits similarities to the 924 LF 11 stage failure of figure 6(c). The MFNOR and HFNOR logic gates both functioned for a surprisingly long time
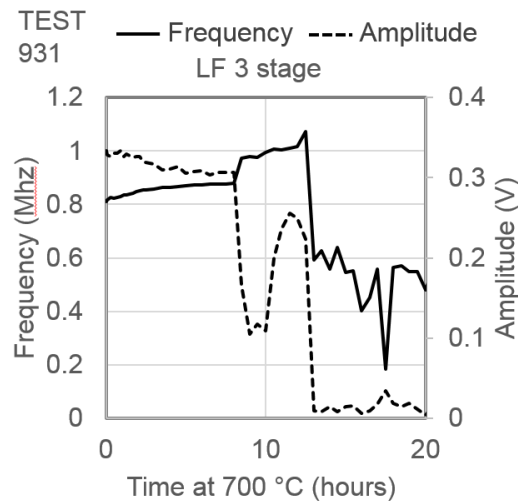

Figure 10. Test 931 LF 3-stage ring oscillator frequency and output amplitude as a function of time at 700 ℃. This device also started to fail intermittently at 8 hours, similar to the 11 stage from 924. VSS=-25V and VDD=25V.
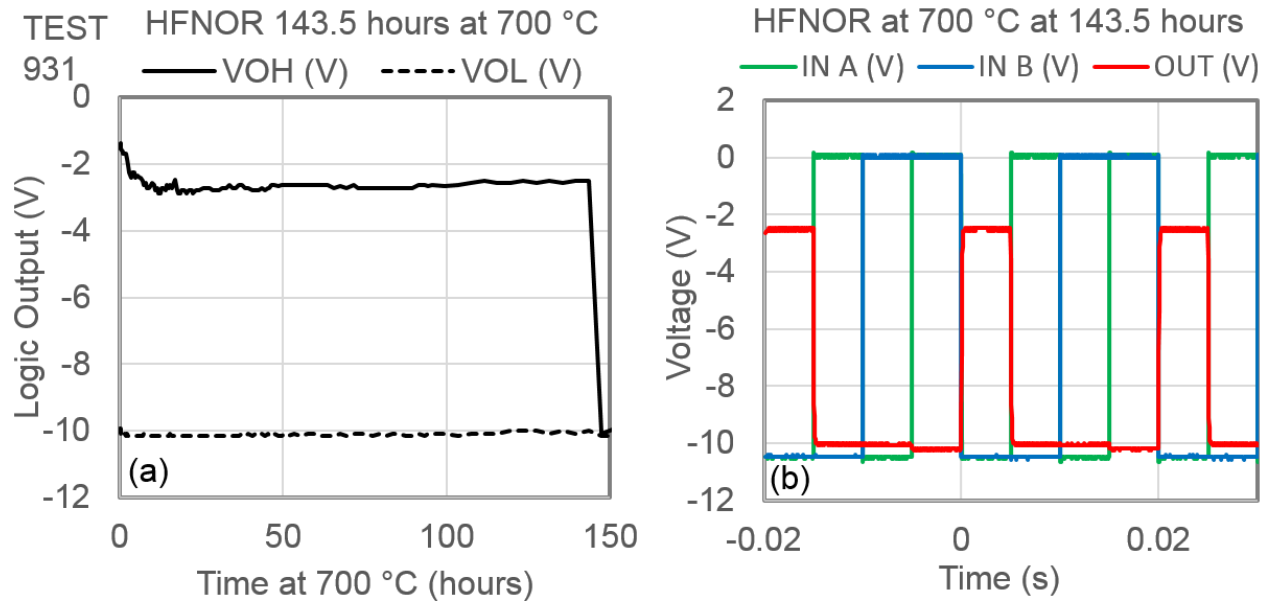
Figure 11. (a) Output high and output low values as functions of time at 700 °C. (b) The input and output wave forms for the high frequency NOR. The MFNOR on 931 lasted 143.5 hours at temperature with VSS=-25V and VDD=25V.

of 143.5 hours at 700 °C. The time evolution of HFNOR voltage output high (VOH) and voltage output low (VOL) are plotted in figure 11(a). The input and output functional test waveforms recorded from HFNOR gate at 143.5 hours into the 700 °C test is shown in figure 11(b).

3. Discussion

Based upon the results of these experiments, it appears that the observed 700+ °C cracking of the dielectric is affected by time, circuit geometry, and electrical bias. Both discrete JFETs started to change at about the same time (25 hours for 6A2 and 23 hours for 931) possibly from similar cracks that form under the same layout design and bias condition, but 6A2 JFET results are also affected by strong encroachment of die attach contamination. The 931 JFET did not suffer from die attach encroachment, but it was clearly impacted by crack-related tantalum silicide ($TaSi_2$) oxidation. The fact that 931 IOFF changed sooner than RDS and IDSS suggests that interconnect leading to the gate contact failed (due to dielectric crack formation followed by oxidation) prior to failure of this JFET's source and drain interconnect traces.

The fact that the three ring oscillators of test 924 and the ring oscillator of test 931 all exhibited a shift in amplitude 8 hours into 700 °C testing suggests a possibly common mode/location of failure for these integrated circuits. Additionally, both V_{SS} bond pads and metal traces on chip 931 exhibit far less visible aging than other pads. When comparing this to the pronounced visible degradation of V_{DD} bus traces closest to the V_{DD} bond pads, the fact that VDD circuit elements have the highest DC potential difference compared to the underlying VSS substrate bias seems significant. However, the power bus bond pads for test 924 could not be similarly inspected due to the excessive lead oxide glass die attach migration. It is also somewhat surprising that 924 had more lead oxide glass migration than 6A2 given that 924 was tested at a 27 °C lower temperature and for less than half the time of 6A2. Also, it is interesting that the lead oxide glass migration in covered 924 devices that were not biased (top half of the die) was faster than it was in biased devices (bottom half of the die).

In order to continue the development of extreme temperature durable 4H-SiC JFET IC technology, future work will include making more complex circuits, correcting the Si_3N_4 wafer loading to prevent wafer temperatures from ramping at more than 3°C /min, and more directly testing the effect of various biases (DC, AC, pulse) on traces and dielectric crack formation. It is technically desired to construct time-to-failure Weibull plots and Arrhenius plots from larger datasets, however this needs packaging capable of $T \geq 500$ °C measurements. The data of this report importantly provides initial

significant evidence that unbiased thermal soak experiments will not accurately reflect the durability of electrically operational ICs.

4. Conclusion

Preliminary accelerated IC testing experiments at temperatures above 700 °C indicate that Au paste should be used for die attach instead of the lead oxide glass based Pt paste which had been designed for 500 °C operation. The formation of cracks in dielectric (SiO_2-Si_3N_4-SiO_2) overlying the IC interconnect, which induced oxidization and cracking of the $TaSi_2$ interconnect, was observed to be a limiting factor in our current 4H-SiC JFET IC process. Failure was not observed with $T \geq 700$ °C for the 32 pin package, the SiC 4H-JFET structure, the Hf ohmic contacts, or $TaSi_2$ in regions free of dielectric cracks. If process revisions can eliminate overlying dielectric crack formation, we believe that highly durable 4H-SiC JFET integrated circuits for temperatures as high as 700 °C may become achievable.

5. Acknowledgments

6. References

[1] Spry, D. J, Neudeck, P. G., Chen, L-Y., Lukco, D., Chang, C. W., Beheim, G. M., Krasowski, M. J., and Prokop, N. F., "Processing and Prolonged 500 °C Testing of 4H-SiC JFET Integrated Circuits with Two Levels of Metal Interconnect, accepted for publication in Materials Science Forum (2016).

[2] Spry, D.J, Neudeck, P. G. Chen, L-Y., Lukco, D., Chang, C. W., and Beheim, G. M., "Prolonged 500 °C Demonstration of 4H-SiC JFET ICs with Two-Level Interconnect," Accepted for publication in Electron Device Letters IEEE (2016).

[3] Spry, D. J, Neudeck, P. G., Chen, L-Y., Chang, C. W., Lukco, and D., Beheim, "4H-SiC JFET Multilayer Integrated Circuit Technologies Tested Up to 1000 K," D. J. Spry, P. G. Neudeck, L. Chen, C. W. Chang, D. Lukco, G. M. Beheim, Electrochemical Society Transactions (October 2015).

[4] D. Culley, "Propulsion Control and Diagnostics Workshop" (16-17 September 2015), http://www.grc.nasa.gov/WWW/cdtb/aboutus/workshop2015/DEC_1_Culley.pdf

[5] Cressler J. D. and Mantooth, H. A. [Extreme Environment Electronics], Boca Raton Florida, CRC Press, ch. 1-5, pp. 1-47 (2013).

[6] Neudeck, P. G., Okojie, R. S., and Chen, L–Y., High Temperature Electronics – A Role for Wide Bandgap Semiconductors? Proc. IEEE. 90(6) pp 1065-1076 (June 2002).

[7] L-Y. Chen, P. G. Neudeck, D. J. Spry, G. M. Beheim, and G. W. Hunter, "Electrical Performance of a High Temperature 32-I/O HTCC Alumina Package," abstract accepted for presentation at 2016 International Conference on High Temperature Electronics (HiTEC 2016).

[8] Spry, D. J, Neudeck, P. G., Chen, L-Y., Evans, L. J., Lukco, D., Chang, C. W., and Beheim, G. M., "Evidence of Processing Non-Idealities in 4H-SiC Integrated Circuits Fabricated with Two Levels of Metal Interconnect," accepted for publication in Materials Science Forum (2016).

[9] Neudeck, P. G., Spry, D. J., Chen, L-Y., "Experimental and Theoretical Study of 4H-SiC JFET Threshold Voltage Body Effect from 25 °C to 500 °C," accepted for publication in Materials Science Forum (2016).

7. Authors Biography

David J. Spry has a B.S. engineering physics with a specialty in material science from The Ohio State University. He has worked the past 16 years on silicon carbide for high temperature electronics used in aerospace sensors in at NASA Glenn Research Center in Cleveland, Ohio. His past research interests include diamond film chemical vapor deposition, cadmium telluride solar cells, and fabrication and testing of conjugated polymer-based light-emitting devices.