Electrical Performance of a High Temperature 32-I/O HTCC Alumina Package

Liang-Yu Chen[1,a], Philip G. Neudeck[2,b], David J. Spry[2,c], Glenn M. Beheim[2,d], and Gary W. Hunter[2,e]
[1] Ohio Aerospace Institute/NASA Glenn Research Center, 21000 Brookpark Road Cleveland, Ohio 44135
[2] NASA Glenn Research Center, 21000 Brookpark Road, Cleveland, Ohio 44135
[a] Email: Liangyu.chen-1@nasa.gov, [b] Email: Neudeck@nasa.gov, [c] Email: David.j.spry@nasa.gov, [d] Email: Glenn.m.beheim@nasa.gov, [e] Email: Gary.w.hunter@nasa.gov

Abstract

A high temperature co-fired ceramic (HTCC) alumina material was previously electrically tested at temperatures up to 550 °C, and demonstrated improved dielectric performance at high temperatures compared with the 96% alumina substrate that we used before, suggesting its potential use for high temperature packaging applications. This paper introduces a prototype 32-I/O (input/output) HTCC alumina package with platinum conductor for 500 °C low-power silicon carbide (SiC) integrated circuits. The design and electrical performance of this package including parasitic capacitance and parallel conductance of neighboring I/Os from 100 Hz to 1 MHz in a temperature range from room temperature to 550 °C are discussed in detail. The parasitic capacitance and parallel conductance of this package in the entire frequency and temperature ranges measured does not exceed 1.5 pF and 0.05 µS, respectively. SiC integrated circuits using this package and compatible printed circuit board have been successfully tested at 500 °C for over 3736 hours continuously, and at 700 °C for over 140 hours. Some test examples of SiC integrated circuits with this packaging system are presented. This package is the key to prolonged T ≥ 500 °C operational testing of the new generation of SiC high temperature integrated circuits and other devices currently under development at NASA Glenn Research Center.

Keywords: Packaging, high temperature, HTCC, alumina, SiC electronics.

1. Introduction

NASA space and aeronautical missions require high-temperature environment operable sensors and electronics for probing the inner solar planets, as well as for in situ monitoring and control of next - generation aeronautical engines [1]. Various SiC high-temperature sensors, actuators, and electronics have been demonstrated at temperatures near or above 500°C, but many of these demonstrations have been limited to short durations less than a few hours. The development of a systematic high-temperature packaging system is essential for both long term testing and beneficial applications of 500°C SiC sensors and integrated circuits. Previously, a 96% polycrystalline alumina (Al_2O_3) based prototype packaging system with Au thick-film metallization [2] successfully facilitated long term testing of high temperature silicon carbide (SiC) electronic devices for over 10,000 hours at 500 °C [3]. However, the 96% Al_2O_3 chip-level packages of this prototype system were not fabricated via an integrated commercial co-fired process, which is more suitable for large scale commercial production. A high temperature co-fired ceramic (HTCC) alumina material was previously electrically tested at temperatures up to 550 °C, and demonstrated better dielectric performance at high temperatures compared with the 96% alumina substrate used before, suggesting its suitability for high temperature packaging applications [4]. This paper introduces a prototype 32-I/O (input/output) HTCC alumina package with platinum conductor for 500 °C low power SiC electronics. Both the design and the electrical performance including DC insulation resistance and AC parasitic conductance and capacitance between neighboring I/Os of this package are discussed.

2. Material System

Compared with 96% alumina, the dielectric performance of experimentally tested HTCC alumina is superior at elevated temperatures [4]. Overall, the dielectric constant of the HTCC alumina is slightly lower and changes less with temperature. The AC

conductivity (dielectric loss) of this material is also lower than that of 96% alumina at temperatures above 200 °C, so it is suitable for high temperature applications. HTCC alumina material systems are usually co-fired with thick-film metallization at temperatures ~1550 °C in noble gas environments, and more often only metals with low CTE (coefficient of thermal expansion) such as tungsten and molymanganese are used with HTCC alumina. However, these conventional metals/alloys have relatively high electrical resistivity, and low oxidation resistance for long term operation in high temperature air ambient. Platinum (Pt) conductor materials designed for HTCC alumina substrates are more suitable for 500 °C packaging applications. Aluminum oxide is usually used as the binder for Pt conductors designed for HTCC alumina substrates. Alumina-alumina bonds at Pt/substrate interface are expected to be more thermodynamically stable over a wide temperature range compared with glass binder used in standard thick-film materials (usually fired at 850 °C). An over-layer of gold, either thin-film or thick-film, on Pt metallization surface was proposed to provide improved material compatibility for gold wire-bonding, as well as gold and gold alloy based die-attach [4].

There are several kinds of high temperature co-fired alumina materials available on the market. Based on the measured dielectric properties of previously tested HTCC alumina substrates, a high temperature co-fired material system of 92% alumina with compatible surface and via Pt conductors [5] was selected for the new 32-I/O prototype package. The relative dielectric constant of this material is 8.4 at room temperature and frequencies at and below 1MHz, it increases more with temperature at lower frequencies to peak value 14.1 at 120Hz and 550 °C. The measured AC conductivity of the HTCC alumina is less than 10^{-8} S/m at frequencies at and below 10kHz, and 10^{-7} S/m at frequencies between 100kHz to 1MHz at room temperature. The AC conductivity increases more at higher frequencies reaching 4.3×10^{-6} S/m at 1 MHz and 550 °C [4]. Testing of additional HTCC alumina material compounds is planned for future work in this direction to further optimize substrate/metallizations combination system for 500 °C applications.

3. Package Design

This new package is designed for low power low frequency SiC JFET based high temperature ICs intended for prolonged operation around 500 °C. It is a surface-mount package with 32 I/Os, it measures about 27.3 mm x 27.3 mm x 2.5 mm (1.07 in. x 1.07 in. x 0.1 in.), lid is 1.02 mm (40 mil) thick. The Pt surface metallization of the package floor is composed of a central square and four surrounding L-shaped patterns allowing multi-chip mixture with individual substrate bias of up to five separate IC dies in a single package. Pt pads for wire-bonding are electrically connected to the pads on the bottom side of the package through hermetic Pt via. One of the pads at

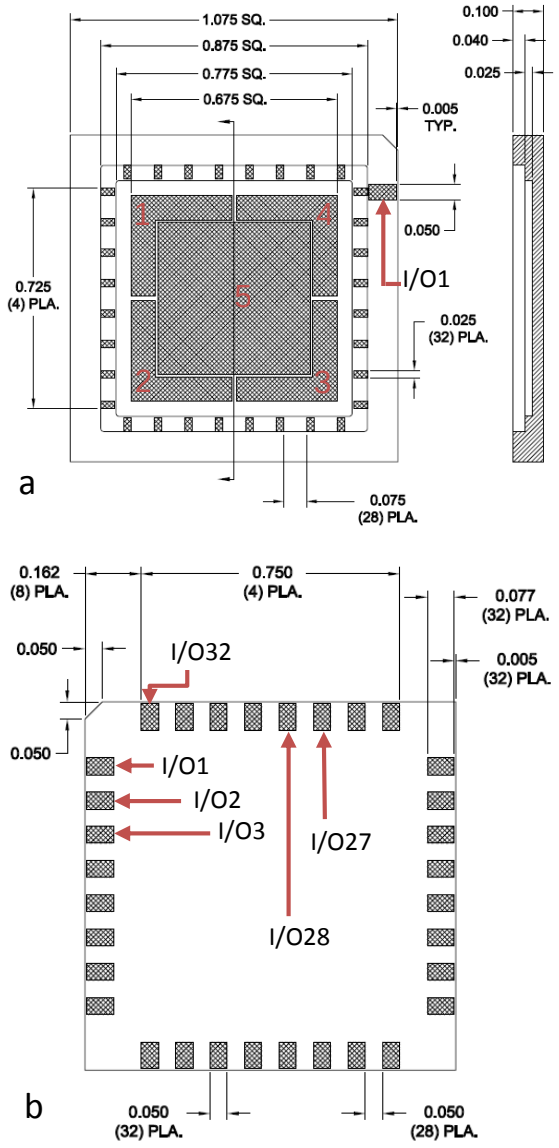

Figure 1: The drawings of 32-pin co-fired Pt/92% alumina package measured 27.3 mm x 27.3 mm x 2.54 mm. 1(a) is the top view of the package and 1(b) is the bottom view of the package. All the dimensions are in unit of inch (1 inch = 25.4mm). Fig. 1a shows five separate pads on the package floor.

the cut-corner is connected to the pad or ring (two different designs) for connection to the lid

metallization as the shield. The package design layout shown in Figure 1 has a Pt pad, instead of a ring (not shown), for connection to the lid. The pads on the bottom of the package for surface mount measure 1.27 mm x 2 mm, and the spacing between two neighboring pads at the same edge is 1.27 mm.

4. Package Characterization

Temperature dependent electrical parameters of the package, such as parasitic AC conductance and capacitance between the ground I/O (I/O1) and its nearest neighbor I/O2, as well as those between I/O2 and I/O3 were measured by AC impedance meters at frequencies of 100 Hz, 120 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz in a temperature range from room temperature to 550ºC. During the testing, the package was soaked in a temperature-controlled air ambient oven with electrical resistive heating coils embedded through two sidewalls of the chamber. The package was directly connected to 0.25mm diameter Au wires with lengths of approximately 15 cm which connected to 1 m long, 50 Ω RG 58C/U standard coaxial cables located outside of the oven. Agilent 4294A, Keithley 3322, and HP 4192A LCZ impedance meters/analyzer were used to measure the inter I/O AC conductance and capacitance based on a RC parallel circuit model. The AC conductance measures the dielectric loss in the substrate material, and the capacitance measures the dielectric polarization of the substrate materials. DC insulation resistance between two neighboring I/Os in a wide range of DC bias up to 50V was assessed by the slope of the measured current - voltage (I-V) curve using a Keithley 2400 source / measurement unit (SMU). The package was heated at 550 °C for 24 hours immediately preceding AC parameter measurements. Both DC and AC specs of the chip-level packages were measured without package lid. Since the AC parasitic parameters are small and comparable to the contributions from gold wires connecting the package inside the oven to coaxial cables outside the oven leading to the impedance meter/analyzer, the parallel RC parameters between gold wires (without a package) were measured separately and the values were subtracted from those with package for more precise measurement/ assessment of package AC parasitic parameters. At frequency of 1MHz, it became more difficult to compensate the parasitic effects of the wiring in the oven, especially under low package conductance, as shown in Table 1 and 2. For some frequency and temperature combinations, measured AC conductance is close to the measurement accuracy limit due to the combination of noise level and instrument calibration limit, especially since the part of the circuit wiring was not electro-magnetically shielded from oven heating elements. For these data points only upper limits of measured values are presented. The oven power was briefly switched off during the measurements of data at 120Hz to reduce AC interference from the filaments in the oven.

4.1 Parasitic AC Parameters

Table 1 shows the results of parasitic capacitance (upper number) in unit of pF and parallel AC conductance (lower number) in unit of µS between I/O1 and neighboring I/O2 (see Figure 1b) with I/O1 connected to all of five metallization pads on the package floor using wire-bonding. The measured parasitic capacitance is between 0.3pF and 1.4pF, generally trending higher at lower frequencies and higher temperatures with the peak capacitance at 120Hz and 500°C and 550°C. This trend is consistent with the dependence of dielectric constant of the alumina material on frequency and temperature reported earlier [4]. The capacitances measured at 120Hz and T ≤ 100°C seem slightly high. At these frequency and temperature combinations the total impedance is high so the measurement uncertainty of

Table 1: Parasitic capacitance (upper) in unit of pF and AC conductance (lower) in unit of µS between I/O1 and I/O2 without a lid on. I/O1 is connected to ground pads. Contributions of gold wires have been subtracted.

T (ºC) / f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550
120	1.0	0.7	0.6	0.4	0.3	0.5	0.4	0.6	0.7	1.4	1.4
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.001	<0.001
1K	0.4	0.2	0.5	0.5	0.3	0.4	0.5	0.5	0.5	0.5	0.4
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
10K	0.5	0.4	0.5	0.5	0.4	0.4	0.4	0.5	0.5	0.4	0.4
	<0.001	0.0013	<0.001	<0.001	<0.001	<0.001	<0.001	0.003	<0.003	<0.003	<0.003
100K	0.5	0.3	0.5	0.4	0.3	0.4	0.4	0.5	0.5	0.4	0.4
	0.01	0.016	0.014	0.016	0.016	0.011	0.014	0.029	0.035	0.026	0.045
1M	0.5	0.4	0.5	0.4	0.3	0.4	0.4	0.5	0.5	0.4	0.5
	<0.010	<0.010	0.013	0.012	0.011	0.006	0.009	0.018	0.021	0.022	0.026

the impedance meter is higher. Overall, the capacitances between I/O1 and I/O2 is low compared with the parasitic capacitance between the ground I/O and a neighboring I/O of the previously reported prototype packages based on 96% alumina with 8-I/O [2].

All the conductance measurements below 0.001µS are noted < 0.001µS in Table 2. Basically, at frequencies at and below 100 kHz the conductance is the highest at 100 kHz and 450 °C and 500 °C, basically consistent with conductivity data of the co-fired alumina material reported earlier [4]. However,

T (°C) / f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550
120	0.7	0.6	0.5	0.4	0.3	0.4	0.4	0.6	0.5	0.6	0.6
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
1K	0.3	0.3	0.4	0.4	0.2	0.4	0.3	0.5	0.3	0.5	0.5
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.0013	0.001	<0.001
10K	0.4	0.3	0.4	0.4	0.3	0.3	0.4	0.4	0.4	0.4	0.3
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
100K	0.3	0.3	0.4	0.4	0.2	0.3	0.3	0.4	0.4	0.4	0.3
	0.005	0.005	<0.005	<0.005	<0.005	0.005	0.013	<0.010	0.014	0.012	<0.010
1M	0.3	0.4	0.4	0.4	0.2	0.3	0.3	0.4	0.4	0.4	0.3
	<0.010	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020

Table 2: Parasitic capacitance (upper) in unit of pF and AC conductance (lower) in unit of µS between I/O2 and I/O3 without a lid on. Contributions of gold wires have been subtracted.

All the conductance measurements below 0.001µS are noted as < 0.001µS in Table 1. Basically, at 100 kHz the conductance increases more with temperature compared with lower frequencies, and reaches 0.045 µS at 100 kHz at 550 °C, consistent with material conductivity data of the alumina material reported earlier. However, the conductance at 1MHz are not higher than those at 100 kHz as we expected from the conductance data of the alumina material. One of the possible reasons for this could be that the device under measurement including the gold wires connecting the package to the coaxial cables can no longer be precisely approximated as a simple parallel RC circuit at 1 MHz since the impedance of the pair of I/Os is high. Overall, the parasitic conductance between I/O1 and I/O2 is lower than the conductance between Ground I/O and neighboring I/O of 96% alumina package previously used for high temperature SiC IC testing [2].

Table 2 shows the results of parasitic parallel capacitance (upper number) in unit of pF and AC conductance (lower number) in unit of µS between I/O2 and neighboring I/O3 (see Figure 1b). The parasitic capacitance is slightly higher at 1 kHz and 120 Hz and 500 °C and 550 °C compared with those at higher frequencies and lower temperatures. The relatively high capacitance at room temperature and 100 °C at 120 Hz could be due to the relative higher measurement uncertainty resulted from high impedance. Compared with parasitic capacitance between a regular pair of I/Os of 96% alumina package, the capacitance between I/O2 and I/O3 of this prototype package is also significantly lower.

the conductance data at 1 MHz does not show clear temperature dependence indicating the measuring accuracy limits were perhaps reached as discussed earlier. Overall, the parasitic conductance between I/O2 and I/O3 is lower than the conductance between Ground I/O and neighboring I/O of 96% alumina package with 8-I/O reported earlier.

4.2 Parasitic DC Leakage

The DC resistivity of ceramic materials usually decreases with temperature. The DC resistance of a pair of neighboring I/Os of the co-fired package was measured by I-V curves from 0 - 50V using a Keithley 2400 source-measurement unit (SMU). The integration time of the SMU was set at 16.67 msec and time delay between two voltage steps was set at 0.1 sec. The I-V curve was measured between I/O27 and I/O28, I/O28 was not electrically connected to the SiC die while I/O27 was connected to an electrically isolated two-terminal test structure on the SiC die. The package was mounted on a compatible PCB. Figure 2 shows the I-V curves measured initially at 500 °C (blue) and 69.4 hours (red) after the initial measurement. The slopes of linear fits of these I-V curves measure the DC resistances of the pair of neighboring I/Os: the insulation resistance initially at 500°C is approximately 7.6 GΩ, increasing to 9.7 GΩ after 69.4 hours at 500 °C. Since I/O27 was connected to a SiC chip and the package was mounted on a PCB, the DC resistance measurements can be expected to slightly underestimate the isolated package DC resistance between two neighboring I/Os.

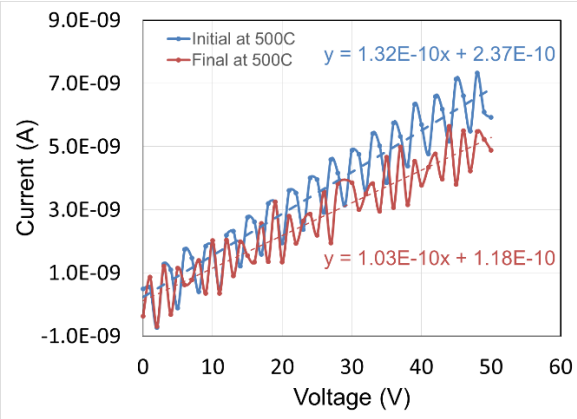

Figure 2: I-V curves measure between I/O27 –I/O28 of the co-fired package at initially at 500°C (blue) and 69.4 hours after (red). The noise was attributed to interference from the running oven. The dash lines are the linear fits.

5.0 Test Results of Packaged SiC ICs

This 32-I/O co-fired package has been tested with different kinds of SiC JFET based analog and digital integrated circuits at high temperatures. Figure 3 shows a packaged 3 mm x 3 mm SiC IC chip mounted on an alumina printed circuit board (PCB) before high temperature test. The compatible PCB was specifically designed for high temperature test of this 32-I/O package, it also uses co-fired Pt/92% alumina material system. The PCB measures 5.1 cm x 5.1 cm x 0.64 mm (2 in. x 2 in. x 25 mil).

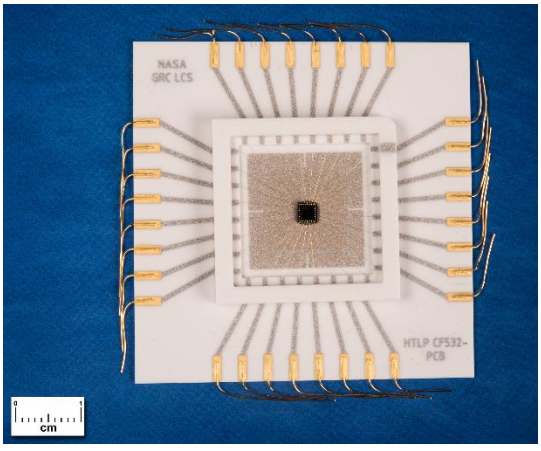

Figure 3: A test assembly of a packaged SiC JFET integrated circuit chip mounted on a co-fired Pt/92% alumina PCB.

A SiC die was attached to the package using either lead oxide based glass mixed with Pt particles or a gold thick-film material. The Pt/glass die attach was dried at 150°C for ten minutes then typically heat-treated at 500°C for two hours. Gold thick-film die-attach was also dried at 150 °C for ten minutes then heat-treated at 600 °C for two to three hours [6]. The temperature ramp rates were 3°C/min. Gold thick-film based die attach is more suitable for testing at temperature above 600°C. Both die attach methods are still under further development. 25.4 µm (1 mil) diameter doped Au wires were thermo-sonically ball/wedge-bonded to electrically connect the SiC die to the package. Cu and Pd doped Au wire was used to control electro-migration under DC bias at elevated

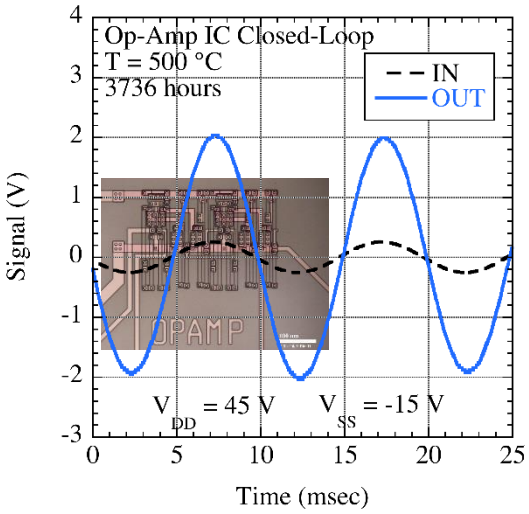

Figure 4: Input and output waveforms of a packaged OPAMP based on SiC JFETs developed at NASA GRC. The data was recorded at 500 °C after 3736 hours continuous test. The output signal was from the "-" output of the OPAMP.

temperature. Foot-long gold wires with 254 µm (10 mil) diameter and glass fiber insulation sleeves were used to connect the PCB in the oven to coaxial cables to measuring instruments.

This 32-I/O package has been used to facilitate long term tests of multiple SiC JFET integrated circuits at 500 °C. Figure 4 shows input and output waveforms of an operational amplifier (OPAMP) recorded at 500 °C after 3736 hours of continuous thermal and electrical tests [7]. The OPAMP was DC biased between -15V (V_{SS}) and 45V (V_{DD}). The waveform in dark is the input signal and the one in blue is the output signal. The OPAMP was tested in closed loop form in which the signal gain of the circuit is determined by two on-chip SiC epi-resistors of ratio

of 8 to 1. The SiC OPAMP for high temperature applications is still under development. After 3736 hours long term testing with SiC JFET based ICs at 500 °C in thermally-static air ambient, no observable failure or degradation of any packages have been detected.

In order to assess short term survivability of both SiC ICs and the packaging system at higher temperatures, packaged SiC ICs were electrically tested at temperatures up to 700 °C [7]. For this test, gold thick-film material was used to attach SiC die to the package. Figure 5 shows the input and output waveforms of a packaged 2-input NOR gate (4-input NOR gate with inputs tied together in order to test using fewer pulse generators) based on SiC JFETs recorded after 143.5 hours of continuous test at 700 °C. The logic "0" is -10.5V, and logic "1" is 0V for inputs [8]. This SiC logic gate lasted 143.5 hours at 700 °C [9]. No catastrophic packaging failure was visually observed or electrically detected during and after the test.

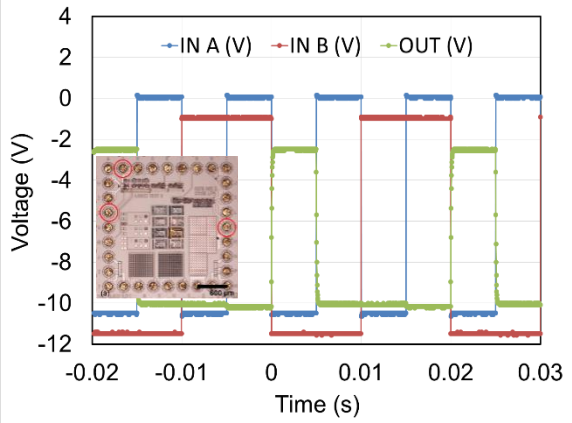

Figure 5: The inputs and output waveforms of a packaged two-inputs NOR logic gate based on SiC JFETs developed at NASA GRC. The data was recorded at 700 °C after 143.5 hours test [9]. The waveform of Input B is shifted -1 V to avoid overlapping with Input A.

6. Discussion and Conclusions

Based on the dielectric test results of a commercial HTCC alumina material at high temperatures, a prototype 32-I/O high temperature co-fired Pt/92% alumina package for low power high temperature ICs was designed, fabricated, electrically characterized. This package was tested with SiC integrated circuits at 500 °C, and 700°C for the first time. Both DC and AC electrical parasitic parameters of neighboring I/Os of this package have been characterized between room temperature and 500 °C. Even at 500 °C the DC resistance between neighboring I/Os is above 1 GΩ. The parasitic capacitance between neighboring I/Os at temperatures T≤ 500 °C in the frequency range from 120Hz and 1MHz is below 1.5pF, and parasitic AC resistance between neighboring I/Os at temperatures T ≤ 500 °C in the frequency range up to 1MHz is over 20 MΩ. A PCB based on co-fired Pt/92% alumina designed for test of this 32-I/O co-fired package has also been demonstrated. Compatible high temperature durable prototype die-attach schemes and thermo-sonic Au alloy wire-bonding have been demonstrated for packaging SiC JFETs based ICs using this packaging system, and packaged SiC ICs have been successfully tested at 500 °C for over 3736 hours. This packaging system can be used for many envisioned logic and signal conditioning high temperature ICs at temperatures up to 500 °C.

This package/PCB system is fabricated using standard packaging materials and processes currently available in industry, so it can be implemented for mass production when it is needed in the future. However, further development for even better overall electrical and mechanical performances is continuing. Even though excellent wire-bonding yields have been achieved, the reliability of gold wire-bonding on the package pads can be further improved by coating a gold over layer. Therefore, an optimal Au coating process needs to be developed. A high temperature durable hermetic sealing process for this packaging system is desired to provide ICs an inert and stable environment for optimal performance and long term reliability in harsh high temperature ambient.

More long term and thermal cycling tests of this packaging system with SiC ICs are planned to further evaluate the performance as well as the reliability of this package at temperatures of 500 °C and higher.

Acknowledgements

The authors wish to gratefully acknowledge the contributions of Drs. Lawrence G. Matus and Dawn C. Emerson at the NASA Glenn Research Center. This work is supported by the NASA Transformative Tools and Technologies (TTT) project, and the NASA Planetary Instrument Concepts for the Advancement of Solar System Observations (PICASSO) programs.

Reference

1a. F. P. McCluskey, R. Grzybowski, and T. Podlesak, High Temperature Electronics, CRC Press, New York, 1997.

1b. J. D. Cressler and H. A. Mantooth, Extreme Environment Electronics (Part I Introduction), CRC Press, Boca Raton, FL, 2013.

2. L.-Y. Chen and G. W. Hunter, "Al_2O_3 and AlN Ceramic Chip-level Packages for 500ºC Operation," in Proceedings of The International Conference on High Temperature Electronics (HITEN) 2005, Paris, France, September 6-8, 2005.

3. P. G. Neudeck, S. L. Garverick, D. J. Spry, L.-Y. Chen, G. M. Beheim, M. J. Krasowski, and M. Mehregany, "Extreme Temperature 6H-SiC JFET Integrated Circuit Technology," Phys. Status Solidi A, 1-17 (2009).

4. L.-Y. Chen, "Electrical Performance of Co-Fired Alumina Substrates at High Temperatures," in Proceedings of iMAPS International High Temperature Electronics Conference (HiTEC), Albuquerque, NM, May 8-10, 2012.

5. http://www.adtechceramics.com/materials

6. P. Zheng, P. Henson, R. W. Johnson, and L.-Y. Chen, "Metallurgy for SiC Die Attach for Operation at 500°C," Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT): January 2010, Vol. 2010, No. HITEC, pp. 000008-000017.

7. D. J. Spry, P. G. Neudeck, L.-Y. Chen, D. Lukco, C. W. Chang, G. M. Beheim, M. J. Krasowski, N. F. Prokop, "Processing and Characterization of Thousand-Hour 500 °C Durable 4H-SiC JFET Integrated Circuits," in Proceedings of 2016 iMAPS HiTEC, Albuquerque, NM, May 9-12, 2016.

8. Philip G. Neudeck, David J. Spry, and Liang-Yu Chen, "First-Order SPICE Modeling of Extreme-Temperature 4H-SiC JFET Integrated Circuits, " in Proceedings of 2016 iMAPS International Conference on High Temperature Electronics, Albuquerque, NM, May 9-12, 2016.

9. D. J. Spry, P. G. Neudeck, L.-Y. Chen, D. Lukco, C. W. Chang, G. M. Beheim, "Experimental Durability Testing of 4H SiC JFET Integrated Circuit Technology at 727 °C," in process.