

Processing and Characterization of Thousand-Hour 500 °C Durable 4H-SiC JFET Integrated Circuits

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Abstract

This work reports fabrication and testing of integrated circuits (ICs) with two levels of interconnect that consistently achieve greater than 1000 hours of stable electrical operation at 500 °C in air ambient. These ICs are based on 4H-SiC junction field effect transistor (JFET) technology that integrates hafnium ohmic contacts with TaSi₂ interconnects and SiO₂ and Si₃N₄ dielectric layers over ~ 1- μ m scale vertical topology. Following initial burn-in, important circuit parameters remain stable for more than 1000 hours of 500 °C operational testing. These results advance the technology foundation for realizing long-term durable 500 °C ICs with increased functional capability for sensing and control combustion engine, planetary, deep-well drilling, and other harsh-environment applications.

Keywords: SiC, JFET, Integrated Circuit

I. Introduction

Extension of the operating temperature envelope of transistor integrated circuits (ICs) well above the effective 300 °C limit of silicon-on-insulator technology is expected to enable important improvements to aerospace, automotive, energy production, and other industrial systems [1,2]. The emergence of wide bandgap semiconductors has enabled IC demonstrations at ambient temperature $T \geq 500$ °C using various device approaches [3-22]. *However, most envisioned applications require stable IC operation over time periods exceeding one thousand hours at extreme temperature.* Two NASA missions desiring such durability are: (1) advanced jet engine ground testing, which sometimes last on the

order of 1000 hours of engine run time, and (2) prolonged atmospheric and seismologic data return from the ~460 °C surface of Venus, far longer than the electronics-limited 2-hour mission of Venera 13[1]. Work demonstrating such prolonged stable IC operation at $T \geq 500$ °C has only been reported using SiC JFETs [3-8], and prior to [7,8] such results were confined to simple logic gates and amplifier stages with ≤ 3 transistors interconnected by a single level of patterned metal.

The implementation of durable extreme temperature ICs with orders of magnitude higher transistor count is needed for most applications. While modestly functional ICs can be implemented using single-level interconnect, multi-level interconnect is a cornerstone of modern $T \leq 125$ °C IC technology due

to the fact that it enables superior IC performance and complexity with smaller chip size.

This work reports further study of 4H-SiC JFET ICs implemented using two levels of interconnect demonstrating over 1000 hours of stable operation at 500 °C that were initially described in [23]. Unlike the prior multi-level interconnect wafer that suffered from highly inconsistent 500 °C durability and inferior yield [7,8], the revised-process ICs reported in [23] and here exhibit consistently good yield for both 25 °C wafer probing and packaged 1000+ hour 500 °C operation.

II. Experimental

A. IC Fabrication

Figure 1a shows an annotated cross-sectional micrograph from the experimental 4H-SiC JFET IC implemented with two levels of interconnect. This wafer was given the laboratory designation "Wafer 9.2". An epitaxial 6 μm gate length SiC JFET (p⁺ gate and n-channel SiC mesas), patterned TaSi₂ interconnect layers (Metal 1 and Metal 2), and via connections through SiO₂ dielectric layers are shown. These were fabricated as described for a preceding wafer process run (that was designated "Wafer 8.1", processed using the same lithographic masks) [7,8], except for the following differences: (1) "gate notching" defects were eliminated by reduced time delay and improved wafer storage between gate and mesa etches, (2) heavily-implanted SiC contact regions were formed using phosphorous implantation (0.39, 0.67, 0.6, & 1.2 x 10¹⁵ cm⁻² dose at 40, 80, 130, & 180 keV, respectively) instead of nitrogen implantation, (3) SiC ohmic contact was formed using a 50 nm sputtered hafnium (Hf) layer, instead of the previously employed titanium (Ti) layer, (4) a 67 nm Si₃N₄ layer was deposited between SiO₂ 3 and SiO₂ 4 layers (Figure 1a), and (5) extensive laboratory improvements to mitigate sodium contamination were implemented. The Si₃N₄ dielectric film inhibits high-temperature penetration of atmospheric oxygen that could undesirably oxidize underlying metals/interfaces over time at T ≥ 500 °C. Metal 1 and Metal 2 are 0.8 μm thick TaSi₂ layers (Figure 1a) [7]. An optical micrograph of the 11-stage ring oscillator IC that underwent prolonged 500 °C oven testing is shown in Figure 1b.

B. Room Temperature Wafer Probing

All devices and circuits were probe-tested on-wafer at 25 °C prior to dicing and packaging. Much more comprehensive 25 °C probe-test data as a function of position on this wafer is described in a

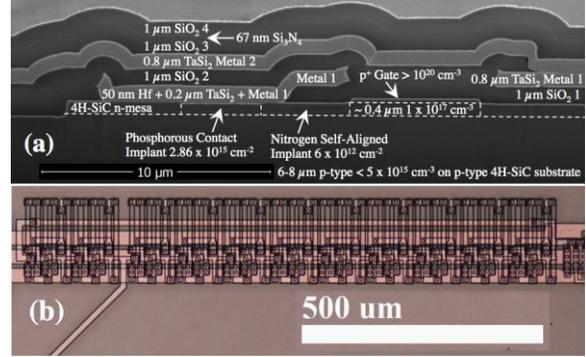


Figure 1. (a) Annotated cross sectional micrograph of 4H-SiC JFET and two-layer interconnect and dielectric stack. (b) Optical micrograph of 11-stage ring oscillator IC with 24 JFETs and 36 resistors implemented in 4H-SiC. Figure used from [23].

separate paper to this conference [24]. Due to epilayer non-uniformity, JFET threshold voltage (V_T) varied as a function of radial distance r from the 76mm diameter wafer center (from -7.9 V at wafer center to -13.8 V at wafer edge for substrate bias $V_S = -15$ V) consistent with a prior study that revealed epilayer thickness variation as the root mechanism [25]. For wafer regions where V_T fell within circuit-design limits ($r < 23$ mm for amplifiers, $r < 33$ mm for logic), wafer probe yields for all circuits of this report exceeded 80%. Table I summarizes the wafer map yield statistics for all the ICs of this paper of 10 or more transistors located within these r limits.

Table I. Wafer 9.2 IC Functional Yield at 25 °C

Integrated Circuit Designation	# FETs	# Good	# Tested	% Yield
MF Gate 3-Stage Ring Oscillator	10	36	39	92%
HF Gate 3-Stage Ring Oscillator	10	66	78	85%
Op Amp Design A	10	19	20	95%
Op Amp Design B	10	18	20	90%
LF Gate 3-Stage Ring Oscillator	12	35	41	85%
LF Gate 11-Stage Ring Oscillator	24	37	41	92%

LF, MF and HF = low, medium, and high frequency

C. Prolonged 500 °C Electrical Testing

Three chips (3 mm x 3 mm each featuring multiple test devices/circuits) were bonded into custom 32-pin Al₂O₃ ceramic packages [7,26] and wired for prolonged operational 500 °C testing in separate ovens. The oven testing setup is not suitable for low noise or high frequency AC measurements due

to large wiring/cabling capacitances and substantial electromagnetic coupling of oven heating element power to unshielded gold wires inside the oven [5,6]. Oven heating/cooling ramp rates were restricted to ≤ 3 $^{\circ}\text{C}/\text{minute}$, and testing started on different dates for each chip/oven.

1) Discrete Devices

Figure 2 plots measured current-voltage (I-V) characteristics of a $12\ \mu\text{m}$ gate width (W_G) by $6\ \mu\text{m}$ gate length (L_G) JFET under $-15\ \text{V}$ substrate bias (V_S) at 0, 96, and 3096 hours at $500\ ^{\circ}\text{C}$. The JFET on-state I-V characteristics (Figure 2a) change $< 5\%$ over the entire test ($< 2\%$ from 96 to 3096 hours). However, JFET off-state current in Figure 2b decreases nearly 2-fold during the first 96 hours at $500\ ^{\circ}\text{C}$. As described in [23], significant burn-in of IC contact and dielectric electrical properties occurs during the first approximately 100 hours of $500\ ^{\circ}\text{C}$ testing.

The time evolution of test devices that underwent prolonged $500\ ^{\circ}\text{C}$ oven testing is summarized in Figure 3. These test devices were implemented using only Metal 1 interconnect, with signal paths entirely free of any overlying Metal 2. The normalized JFET I_D at $V_G = -12\ \text{V}$ and $V_D = 20\ \text{V}$ (i.e., JFET I_{OFF}) is plotted vs. time for 3093 hours at $500\ ^{\circ}\text{C}$. JFET I_{OFF} and n-type 4H-SiC sheet resistance (R_{SheetN}) exhibit the most stable post burn-in behavior, reflective of the excellent stability of intrinsic SiC electrical properties.

Extrinsic properties associated with contacts and dielectrics are somewhat less stable. The dielectric test leakage current device (plotted in Figure 3 grey solid line) shows roughly 10-fold current increase near 3000 hours. This device consists of parallel $377\ \mu\text{m}$ long Metal 1 traces laterally separated by a $6\ \mu\text{m}$ dielectric gap measured with $20\ \text{V}$ applied DC bias between the traces. The sheet resistance of Metal 1 interconnect and specific n-contact resistivity (R_{SpecN})

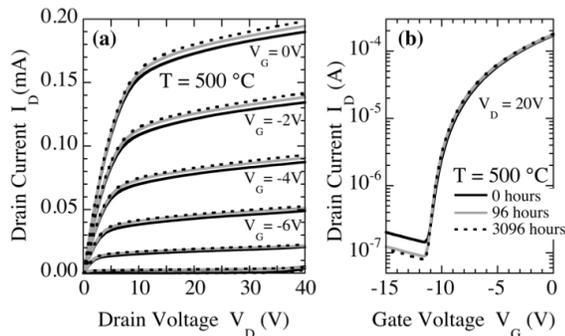


Figure 2. Measured $12\ \mu\text{m}/6\ \mu\text{m}$ JFET (a) I_D vs. V_D and (b) I_D vs. V_G at 0, 96, and 3096 hours of packaged $500\ ^{\circ}\text{C}$ testing with $V_S = -15\ \text{V}$. This JFET was from a chip $r = 23\ \text{mm}$ from the wafer center.

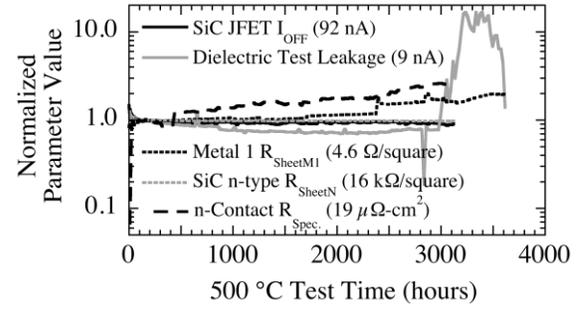


Figure 3. Selected process test device parameters for the 3615 hours at $500\ ^{\circ}\text{C}$, plotted normalized to each parameter's value 96 hours into the test (96 hour values shown in parenthesis).

show roughly 2-3 fold increase by 3000 hours. Despite this increase, these parasitic resistances remain small compared to the n-SiC channel resistances. The Metal 1 test structure is a $6\ \mu\text{m}$ wide by $574\ \mu\text{m}$ long by $0.8\ \mu\text{m}$ thick TaSi_2 trace. This trace was biased with $1\ \text{mA}$ current flow for the entire $500\ ^{\circ}\text{C}$ oven test, corresponding to a cross-sectional current density of $20.8\ \text{kA}/\text{cm}^2$

Figure 4 details the electrical and physical behavior of a linear transmission line method (TLM) device subjected to 3096 hours of $500\ ^{\circ}\text{C}$ oven-testing. Figures 4a and 4b compare optical microscope images of the TLM device before (prior to custom-packaging) and after the oven test, while Figure 4c shows the measured resistance of R_{12} , R_{23} , and R_{34} plotted vs time. Figure 4d shows a post-test close-up of contact 4, which exhibits cracking along the perimeter of Metal 1. Only contact 4 showed electrical failure and physical discoloration of the TaSi_2 , and cracking of the

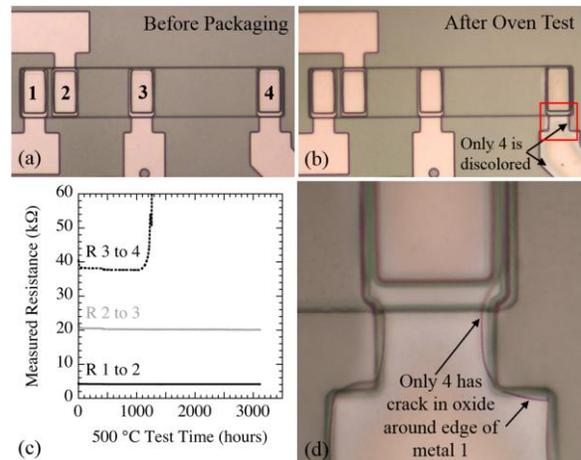


Figure 4. (a) Before packaging optical image. (b) After oven test image of the same TLM. Only contact 4 shows electrical failure as can be seen in the plot of R_{12} , R_{23} , and R_{34} in (c). A crack in the dielectrics that allowed for the oxidation of the TaSi_2 which causes discoloration can be seen in both (b) and (d).

dielectric. From the Figure 4 observations, it is hypothesized that dielectric cracking occurred first, leading to penetration of atmospheric oxygen to the underlying metallization followed by metal oxidation resulting in the documented open-circuit failure of the contact 4 conduction path. Regions free of dielectric cracks and metal discoloration (e.g., contacts 1-3) exhibited acceptable conduction throughout the 500 °C test.

While further failure analysis studies are needed, the basic dielectric cracking followed by metal oxidation failure mechanism seen in Figure 4 could be responsible for the majority of long-term 500 °C circuit failures for chips from this experimental wafer. It should be noted that extracted sheet resistance and contact resistance graphed in Figure 3 were calculated using only R_{12} and R_{23} measured data.

2) Logic Gates

All logic gates were implemented using the circuit approach of Krasowski [27,28] (e.g., Figure 5a NOT gate schematic) with negative signal voltages. Three different layout variants were implemented: high frequency “HF” gates with 4.5 square (i.e., 27 μm long by 6 μm wide) resistors and $W_G = 192 \mu\text{m}/L_G = 6 \mu\text{m}$ JFETs, medium frequency “MF” gates with 7.5 square resistors and 192 $\mu\text{m}/6 \mu\text{m}$ JFETs, and low frequency “LF” gates with 35 square SiC resistors and 24 $\mu\text{m}/6 \mu\text{m}$ SiC JFETs. Figure 5a plots voltage transfer characteristics of an MF series NOT gate at 0, 96, and 3615 hours at 500 °C. The time evolution of output high (V_{OH}) and low (V_{OL}) for all oven-tested simple logic gates are plotted in Figure 5b (driving outside-oven 10 M Ω probes with -10 V and 0 V input test signals). The initial upward drift of output voltages is qualitatively consistent with behavior expected from diminishing leakage current with time. V_{OL} sharply increases at 1496 hours for three gates that share common input pads. However, V_{OH} of the 4-input LF NOR gate (NOR4) fails independent of the other two shared-input gates just before 1916 hours of 500 °C operation. The MF NOT which had its own input pads continues to operate as of this writing beyond the graphed 3615 hours in Figure 5b. At 3400 hours the MF NOT had a small shift in both V_{OH} and V_{OL} but has not changed since.

3) Ring Oscillators

Figure 6a plots measured frequencies for all four oven-tested ring oscillator ICs (each normalized to its respective 96 hour value). The operating frequencies of these test ICs reflect the inherent speed/frequency of each logic gate layout variant at 500 °C. Figure 6b plots the output amplitude for the

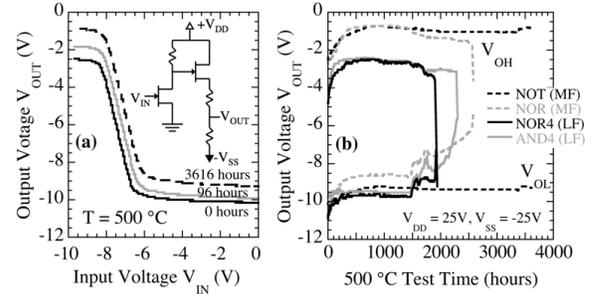


Figure 5. Measured 500 °C (a) MF NOT gate V_{OUT} vs. V_{IN} transfer characteristics at selected test times, and (b) V_{OH} and V_{OL} for all oven-tested logic gates vs. 500 °C test time (see text).

same devices. The 3-stage MF and 3-stage LF ring oscillators failed 1056 hours and 1656 hours into the test, respectively, while the 3-stage HF ring oscillator’s output amplitude drops abruptly at 1900 hours but does not fully fail until 2260 hours. The 11-stage LF ring oscillator output amplitude begins to change at 3400 hours and ceases at 3540 hours.

4) Amplifiers

One of the oven-tested chips contained two operational amplifiers (op-amps, each with 10 JFETs and two gain stages) and two differential amplifier (diff-amp) test circuits (one with output level shifters and one without, replicas of op-amp sub-circuits). Figure 7 shows a schematic of the diff-amp and level shifters. Figure 8 shows an optical image of the physical device with the diff-amp and level shifters

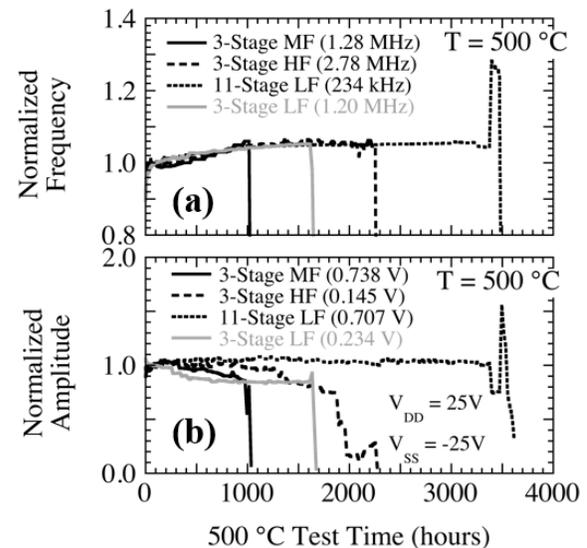


Figure 6. (a) Ring oscillator frequency and (b) ring oscillator amplitude vs. 500 °C testing time for all high temperature packaged oscillators, normalized to each oscillator’s frequency 96 hours into the 500 °C test (shown in parenthesis).

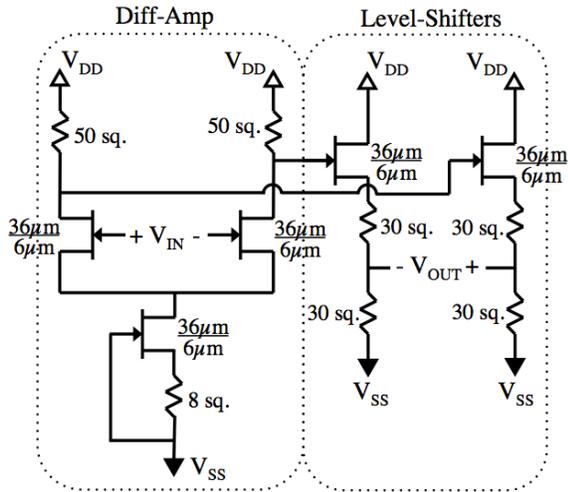


Figure 7. Schematic diagram of diff-amp and level shifters.

sections marked with a red dashed line and labeled, while the JFETs are highlighted in green. One of the op-amps did not function at 500 °C. Figure 9 plots measured 500 °C differential small signal voltage gains of the working amplifiers at 100 Hz driving outside-oven AC-coupled 10 MΩ oscilloscope probes. Figure 9 diff-amp gains change less than 10% following burn-in. The functional op-amp was initially tested open loop. The recorded open-loop differential gain data is plotted in the upper left of Figure 9. At 534 hours this op-amp was re-configured (by connecting wires outside the oven) for closed-loop operation using a 10-square SiC input resistor (R_i) and an 80-square SiC feedback resistor (R_f) on the amplifier chip and oscilloscope waveform averaging (off for all other measurements) was turned on to 4 samples. The measured closed-loop gain in Figure 9 tracks within 15% of expected $R_f/R_i = 8$ for over 3000 hours. All three Figure 9 amplifier circuits were still running past 3740 hours at 500 °C as of this writing.

D. Image of 650 °C Initial of Electrical Testing

A fourth die from this wafer was custom-packaged using gold paste as a die attach material for $T > 500$ °C testing. An imaging system with a focal length of 350mm and focal ratio $f/5.8$ was used with a 1.7cm Peltier cooled 5 mega pixel color CCD detector to acquire the images of the die and package glowing red hot. The focus was set after the initial 69.4 hour 500 °C burn-in of a die with 3 ring oscillators, a JFET (9.72 mm/6 μm), and an MF NOT logic gate. At this time the initial image of the packaged device shown in Figure 10a was recorded using only ambient room light. With all logic devices biased and operating, the oven was then taken to 650 °C. The JFET was forward

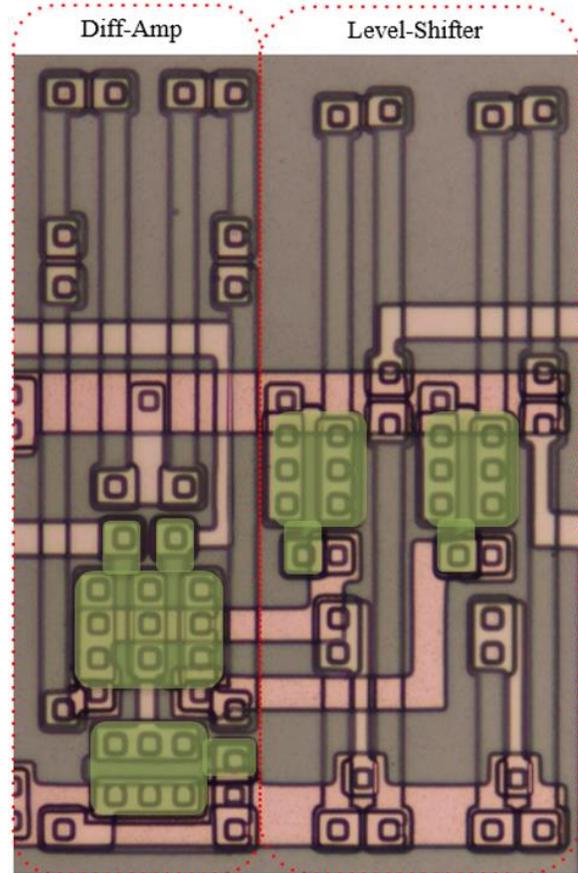


Figure 8. Optical image of diff-amp and level shifter. JFETs are highlighted in green.

biased across the gate-channel junction at 80 mA to emit blue light as seen in Figure 10b. The door to the oven was momentarily opened to record the glowing red-hot chip image. That is why the wires toward the front/bottom of the image are cooler. After a dozen images (opening and closing of the oven) the sample

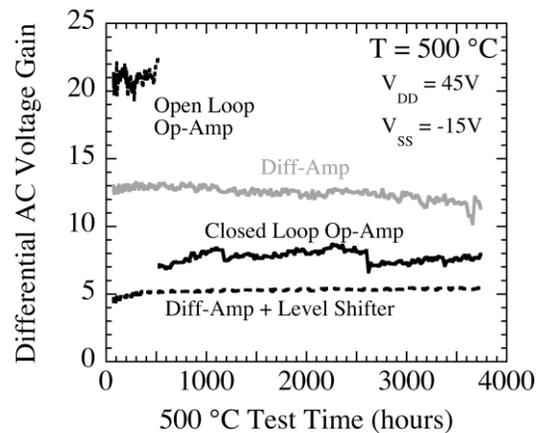


Figure 9. Measured differential small-signal voltage gain vs. 500 °C amplifier testing time (see text).

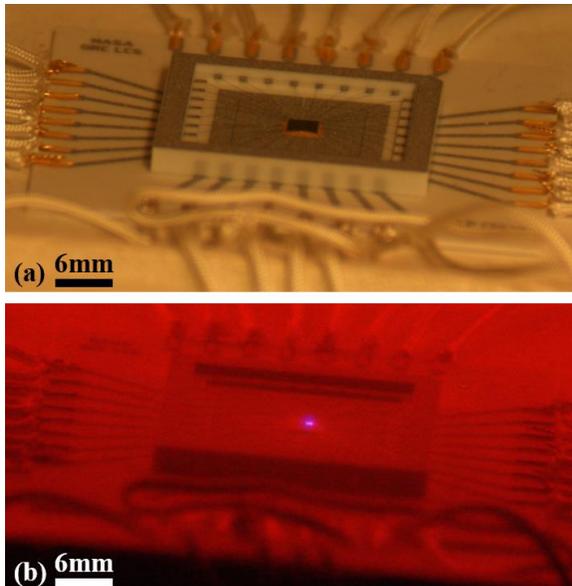


Fig. 10. (a) Optical image of packaged device with room light illumination. (b) Optical image of packaged device at 650 °C with a large JFET under forward bias of the gate-channel junction resulting in blue light emission. Three ring oscillators and a MF NOT were electrical test before and after the image was taken.

was bias tested at 650 °C for over 100 hours without any failures as of this writing.

III. Conclusion

This work has initially demonstrated two-level interconnect digital and analog integrated circuits consistently operating past 1000 hours at 500 °C with better than 80% yield. These results significantly advance prospects for realizing complex and 500 °C durable ICs for sensing and control circuits in combustion engine, planetary, deep-well drilling, and other extreme-environment applications. While further failure analysis studies are needed, the basic dielectric cracking followed by metal oxidation failure mechanism could be responsible for the majority of long-term 500 °C circuit failures for chips from this wafer. Continued temperature testing/analysis [28], degradation/failure analysis, and further up-scaling of IC transistor counts are planned.

Acknowledgements

The authors wish to gratefully acknowledge the assistance of K. Moses, J. Gonzalez, A. Avishai, M. Mrdenovich, G. Hunter, R. Buttler, L. Matus, R. Meredith, and C. Blaha.

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