National Aeronautics
and Space Administration

JESD57 Test Standard, *"Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy-Ion Irradiation"* Revision Update

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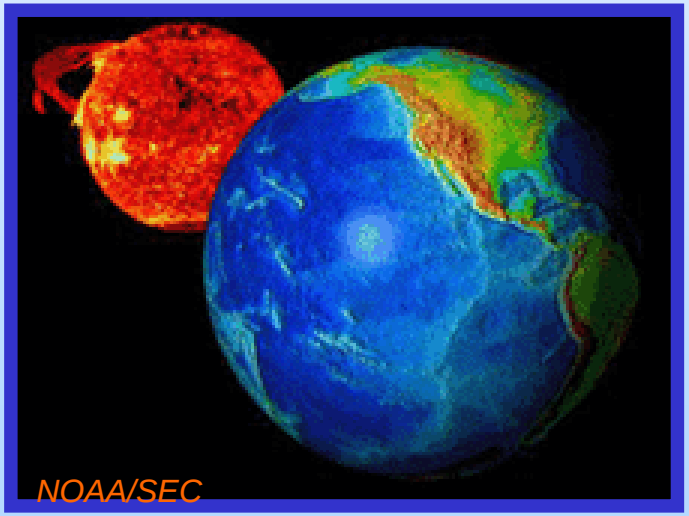
List of Acronyms

ASTM – (no longer an acronym)
DLA – Defense Logistics Agency
GSFC – Goddard Space Flight Center
IC – Integrated Circuit
JEDEC – (no longer an acronym)
JESD – JEDEC Standard
JPL – Jet Propulsion Laboratory
LET – Linear Energy Transfer
MBU – Multiple Bit Upset
MCU – Multiple Cell Upset
MIL-STD – US Military Standard
MOSFET – Metal Oxide Semiconductor Field Effect Transistor
NEPP – NASA Electronic Parts and Packaging program
SBU – Single Bit Upset
SEB – Single-Event Burnout
SEE – Single-Event Effect
SEFI – Single-Event Functional Interrupt
SEGR – Single-Event Gate Rupture
SEU – Single-Event Upset
SET – Single-Event Transient
SOA – Safe Operating Area
TM – Test Method
XS – Cross Section

Outline

- **Test Standards & Guidelines: Putting JESD57 into Context**
- **Motivation for Update**
- **Revision Highlights**
- **Challenge of New Technology**
- **Conclusions**



Standard Rationale

- **Standards & Guidelines are developed/revised to:**
  - **Ensure tests follow best practices**
  - **Ensure results from different vendors/testers are comparable**
  - **Minimize and bound systematic and random errors**

Data must be meaningful and must facilitate part selection and risk analysis

Best practices must be disseminated to new members of the test community

Key Space Radiation Test Standards

Standard	Title	Date
JEDEC JESD57	**Test Procedures for the Measurement of SEE in Semiconductor Devices from Heavy-Ion Irradiation**	**1996**
JEDEC JESD234	Test Standard for the Measurement of Proton Radiation SEE in Electronic Devices	2013
MIL-STD-750-1	Environmental Test Methods for Semiconductor Devices TM 1017: Neutron irradiation TM 1019: Steady-state total dose irradiation procedure TM 1080: SEB and SEGR	2014
MIL-STD-883	Microcircuits TM 1017: Neutron irradiation TM 1019: Ionizing radiation (total dose) test procedure	2014
ESA-ESCC-25100	SEE Test Method and Guidelines	2014
ESA-ESCC-22900	Total Dose Steady-state Irradiation Test Method	2010

(Prompt dose and terrestrial radiation standards not included)

**TM = Test Method*

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Space Radiation Test Guidelines

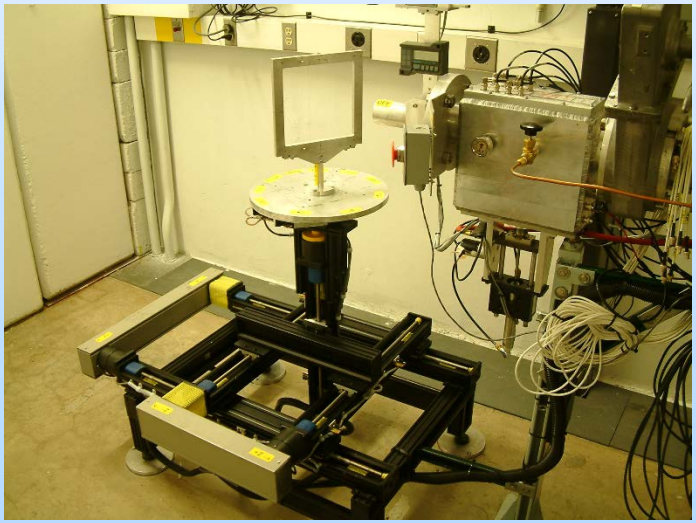
Standard	Title	Date
ASTM F1192	**Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices**	**2011**
ASTM F1892	Standard Guide for Ionizing Radiation (Total Dose) Effects Testing of Semiconductor Devices	2012
ASTM F1190	Practice for the Neutron Irradiation of Unbiased Electronic Components	2011
MIL-HDBK-814	Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuits and Semiconductor Devices	1994
Sandia Nat'l Lab. SAND 2008-6983P	**Radiation Hardness Assurance Testing of Microelectronic Devices and Integrated Circuits: Test Guideline for Proton and Heavy Ion SEE**	**2008**
Sandia Nat'l Lab. SAND 2008-6851P	Radiation Hardness Assurance Testing of Microelectronic Devices and Integrated Circuits: Radiation Environments, Physical Mechanisms, and Foundations for Hardness Assurance	2008
NASA/ DTRA	**Field Programmable Gate Array (FPGA) Single Event Effect (SEE) Radiation Testing**	**2012**

(See ASTM website for additional guidelines)

Motivation for JESD57 Update

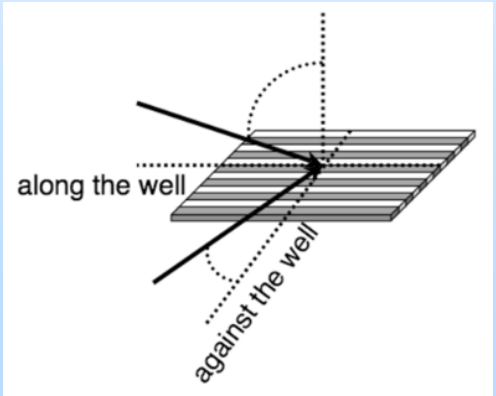
- **Review cycle for JESD57 is overdue**
  - Outdated elements include, among others, facility capabilities, beam angle of incidence methods and objectives, and even some of the definitions of various SEE.
  - Missing elements include:
    - "Modern" complex device test considerations
    - Single-event burnout testing
    - Single-event transient testing

Higher-energy (> 10 MeV/u) facilities explicitly NOT included in 1996 JESD57



http://cyclotron.tamu.edu/ref/in_air.php

Angle tests not just for effective LET: critical to reveal some SEE. Both tilt and roll angles can matter.



Tipton, IEEE TNS, 2008

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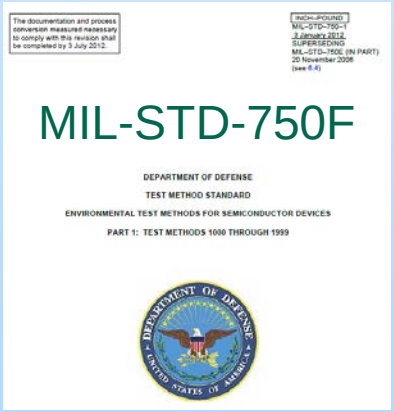
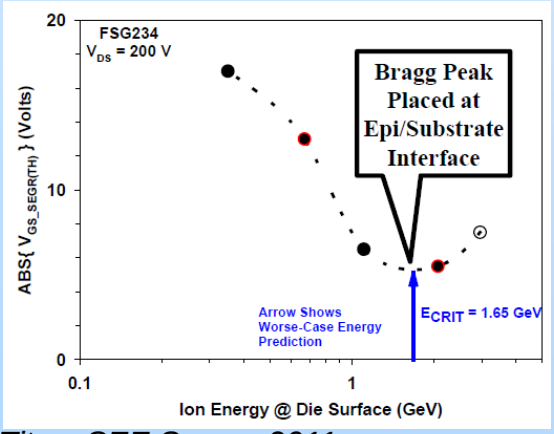
- **JESD57 SEGR method no longer in line with MIL-STD-750 TM1080**
  - 2012 major rewrite of TM1080, "Single-event Burnout and Single-event Gate Rupture"
    - LET metric was expanded to emphasize the impact of ion species & energy on SEGR susceptibility
    - Worst-case penetration range defined as yielding max energy deposition in the epilayer



Ion range matters for SEGR:
LET too simplistic as
a single metric



Titus, SEE Symp., 2011

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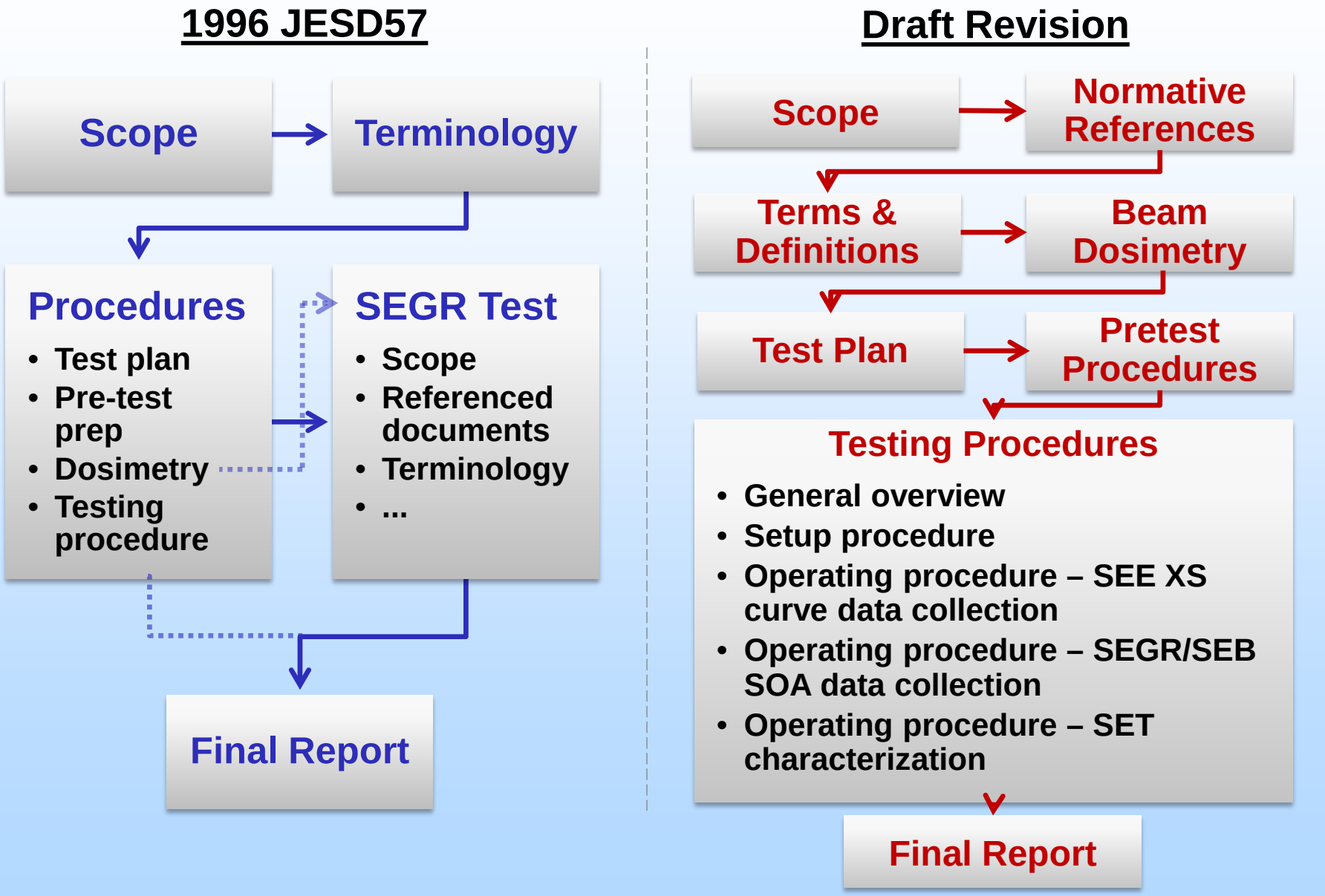
- **Update to JESD57 can form basis for DLA integration of SEGR/SEB test method into MIL-STD-883, *"Microcircuits"***
  - Both current JESD57 and MIL-STD-750 TM1080 standardize testing of discrete, planar-gate vertical power MOSFETs
  - Other discrete topologies and integrated components not explicitly addressed

Revision Highlights: Format



Revision Highlights: Definitions

- **Many terms added to definitions section:**
  - **Bragg curve, Bragg peak;**
  - **Multiple-bit upset; multiple-cell upset**
  - **SEGR Post-irradiation gate stress (PIGS) test**
  - **Single-event transient**
  - **Stuck bit**
- **Many definitions updated**
  - **Effort to stay consistent with other JEDEC documents:**
    - JESD88, "*JEDEC Dictionary of Terms for Solid-State Technology*"
    - JESD234, *"Test Standard for the Measurement of Proton Radiation Single Event Effects in Electronic Devices"*
    - JESD89-1A, *"Test Method for Real-Time Soft Error Rate"*
      - Including current draft revision
  - **Despite this effort, some definition revisions are new and will require JEDEC approval/adoption**

Terms & Definitions Highlight:
Single-Event Functional Interrupt (SEFI)

- **1996:**

The loss of functionality of the device that does not require cycling of the device's power to restore operability unlike SEL and does not result in permanent damage as in SEB.

NOTE — SEFI is typically caused by a device being cycled to a nongenerated test mode due to a heavy ion strike.

- **Draft Revision:**

A non-destructive interruption resulting from a single ion strike that causes the component to reset, hang, or enter a different operating condition or test mode.

NOTE 1 A SEFI is often associated with an SBU/MBU in a control bit or register.

NOTE 2 Changes in functionality may require a soft or hard reset of the device, reprogramming of the control registers, or power cycling.

NOTE 3 A SEFI can introduce a latent reliability issue due to a period of high current. SEFIs that result in permanent damage are designated as single-event hard errors.

Terms & Definitions Highlight: Single-Event Upset (SEU)

- **1996:**

A single latched logic state from one to zero, or vice versa.

NOTE The SEU is “soft” because the latch can be rewritten and behave normally thereafter.

- **Proposed:**

The change of a bi-stable node state from one to zero, or vice versa, due to the passage of a single energetic particle.

NOTE 1 SEU, including SBU, MBU, and MCU, is typically "soft" because the affected nodes can be rewritten and behave normally thereafter.

NOTE 2 An SEU that results in a change in device functionality requiring intervention is defined instead as a SEFI.

Revision Highlights: Expansion of SEE Test Procedures

- **SEB & SEGR:**
  - **SEB test procedure added;**
  - **SEGR & SEB procedures expanded to include both devices and integrated circuits (ICs)**
    - Accounts for inaccessible drain and/or gate nodes in ICs
- **SET:**
  - **New test procedure for characterizing SETs in analog parts**
    - SET magnitude/duration plots
    - SET cross-section vs. LET for rate determination
  - **Digital SETs out of scope for this revision**
    - References provided instead.

JESD57 Challenge: Advanced Electronics

- **How do we incorporate advanced electronics SEE testing into SEE test standards?**
  - Revision of JESD57 is an opportunity for inclusion of more established methods for testing advanced electronics
  - Highly complex technologies will benefit from specific guidelines
    - ex/ NASA FPGA test guideline
  - Complex devices incorporate many modes and functions
    - Test results depend on how we test the device
    - The bleeding edge of testing is generalizing application specific test results to bound flight performance at all stages of the mission

High-Speed Test Fixture

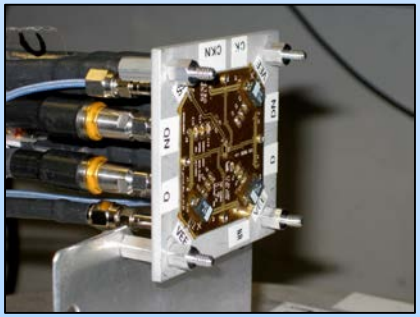
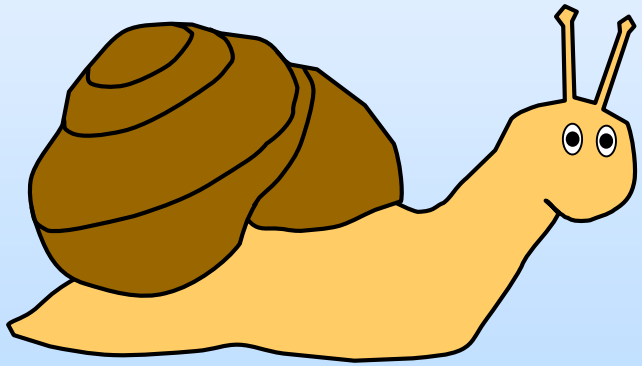


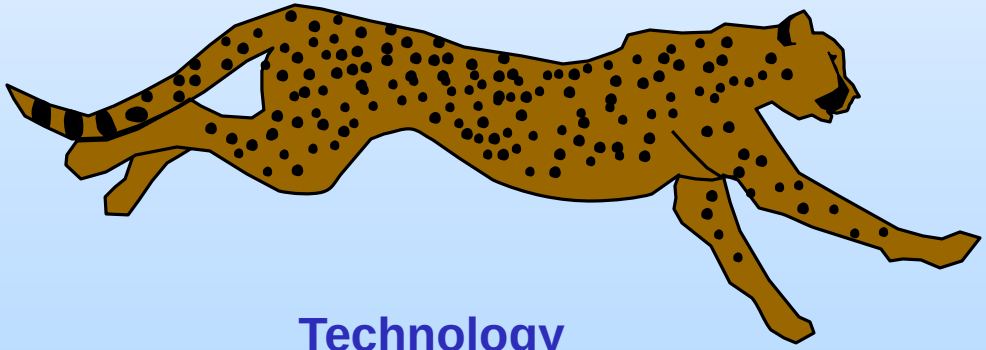
Photo credit: J. A. Pellish, 2013

The Time Lag

- **Test standards & guidelines can (and often do) take years to develop or revise**
  - Widespread compliance can take additional years
- **Technology & research continuously evolve**



Test Standards



Technology

The time lag is both useful and problematic

JESD57 and Test Guidelines

- **Draft Revision of JESD57 = True "Test Standard"**
  - **Guideline material not permitted and thus removed**
- **"Informative Annexes" can serve as repositories for guideline material**
  - **Document the "why" behind the standards**
  - **Allow inclusion of test considerations when methods have yet to be established**
    - For new technologies
    - For new failure modes

Informative annex contains information intended only to assist the understanding or use of the document.

Summary

- **JESD57 is the only U.S. test standard covering many of the heavy-ion induced single-event effects.**
- **Last updated in 1996, a new revision will soon be submitted for a vote.**
- **Advanced electronics and complex technologies present a continual challenge:**
  - **Solutions likely in the form of separate guidelines;**
  - **Informative Annexes may provide an initial step toward inclusion in JESD57.**

We must recall that:

- **Test standards are a compromise between technical rigor and economic realities**
  - **The goal is to be good enough to ensure success and cheap enough that the standards & guidelines will actually be used**

JESD57 Update: The "Who"

- **JESD57 ownership: JEDEC JC-13.4 Government Liaison Subcommittee on Radiation Hardness Assurance**
- **Committee meetings 3 times/year:**
  - **Both JC13.4 and G12 Radiation Hardness Assurance subcommittees have provided a platform to work with relevant industry and user communities to:**
    - Review major changes in content and format
    - Work toward consensus on more controversial or less established definitions, concepts, or methods

Jean-Marie Lauenstein's involvement in this update process is sponsored by the NASA Electronic Parts & Packaging Program.