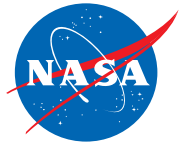


Experimental Durability Testing of 4H SiC JFET Integrated Circuit Technology at 727 °C

David J. Spry[1], Philip G. Neudeck[1], Liangyu Chen[2],
Carl W. Chang[3], Dorothy Lukco[3], Glenn M. Beheim[1]

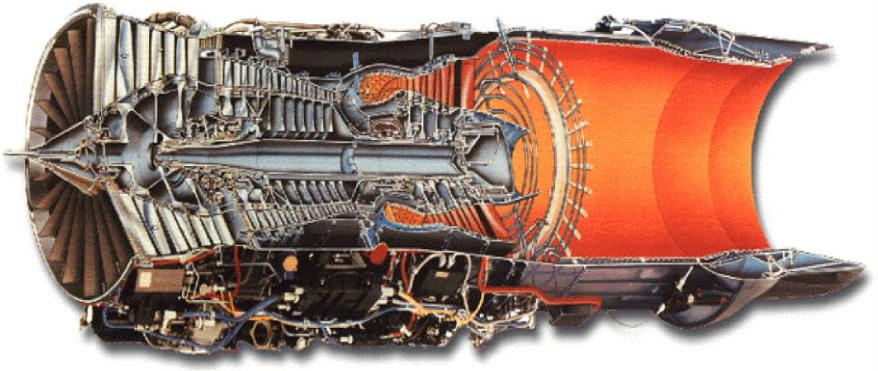
[1]NASA Glenn Research Center

[2]Ohio Aerospace Institute

[3]Vantage Partners LLC

SiC Electronics Benefits to NASA Missions

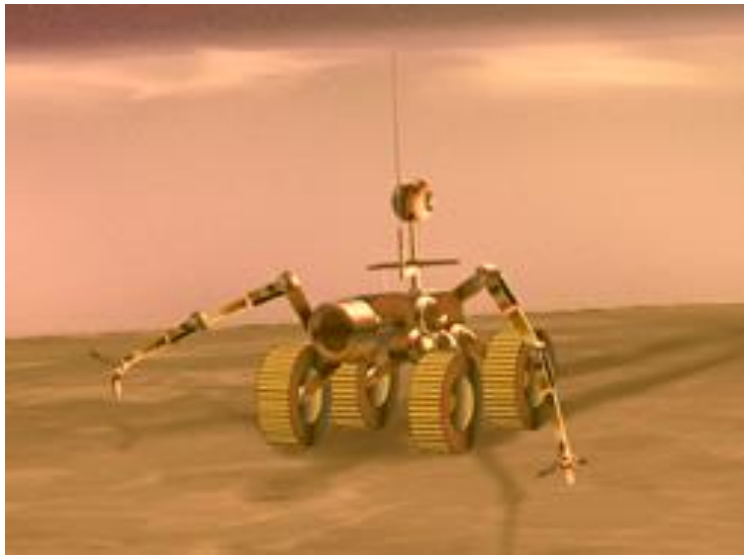
Intelligent Propulsion Systems



"GEER" Venus Test Chamber

Hybrid Electric Aircraft

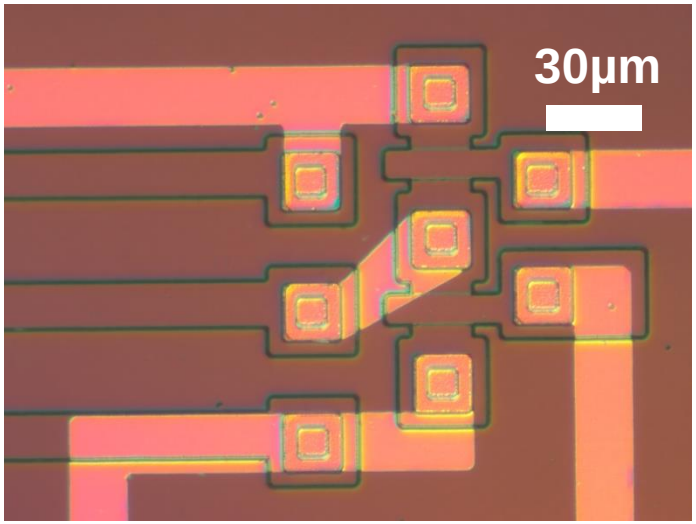
Venus Exploration

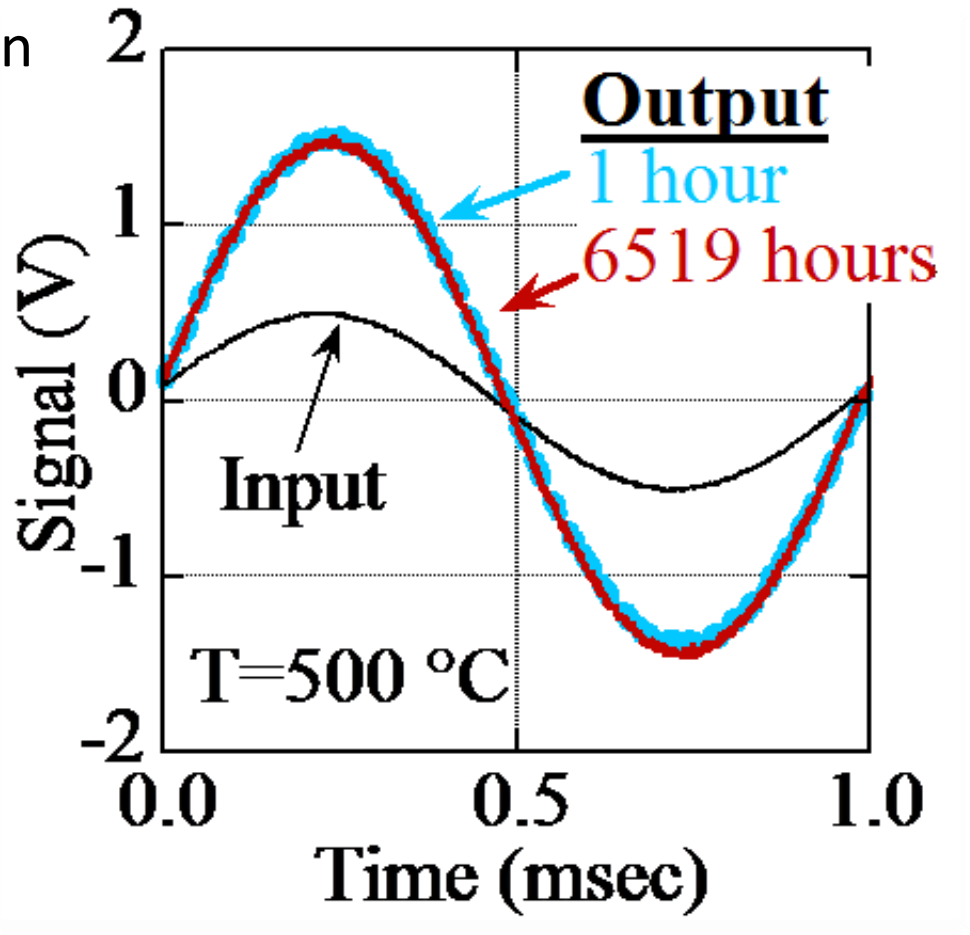


NASA GRC's internal research effort has been to focus on durable integrated circuits at 500 °C for > 3000 hrs.

Past work with single layer of interconnect

- Differential amplifier made in 6H-SiC operated 6519 hours at 500 °C in air ambient.
- Complexity limited. Only 2 transistors and 3 resistors.
- JFET approach good for minimizing gate leakage and durability at 500 °C.





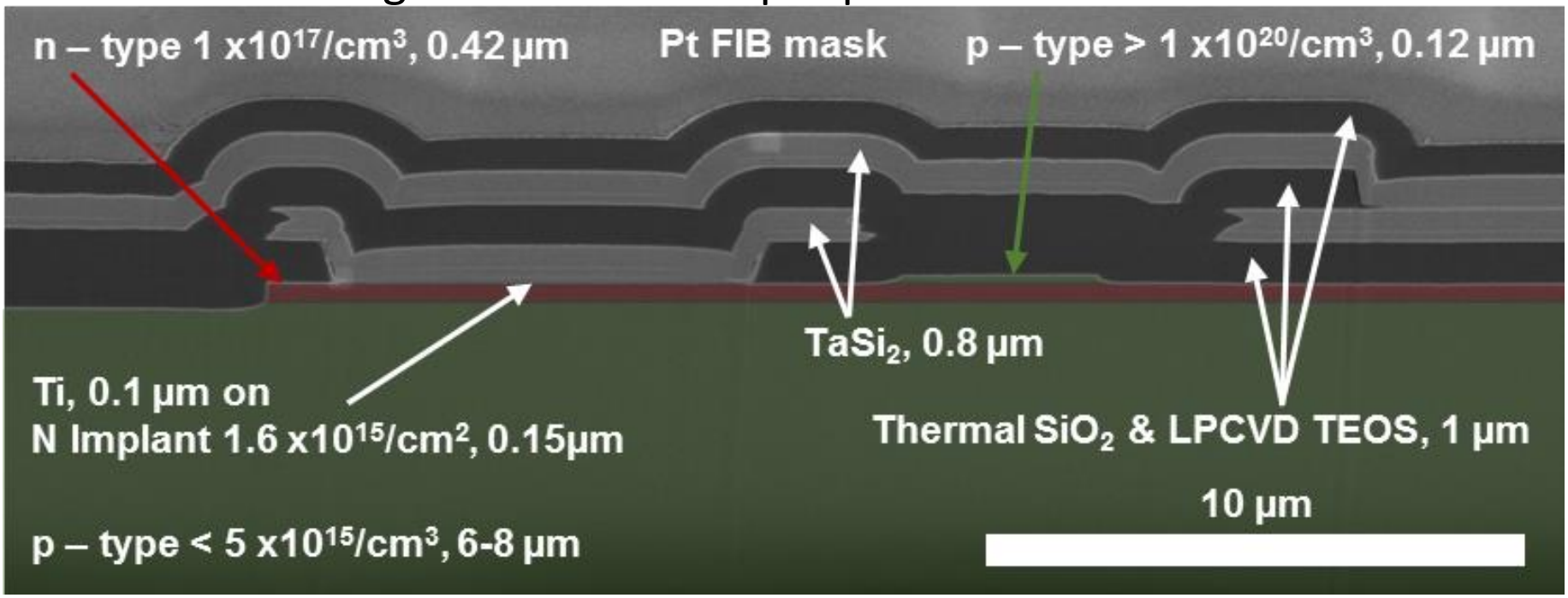
Phys. Status Solidi A **206**, No. 10, 2329–2345 (2009)

8.1 vs past work - Two levels of metal interconnect

Processing enhancements for conformal processing on topology.

- Proximity sputtering of $TaSi_2$ (21mm target to substrate spacing).
- LPCVD tetraethyl orthosilicate (TEOS) deposited 720 °C.
- Design rules for thick dielectrics and metal traces.

Enables crisscrossing traces and on chip capacitors. Now 4H not 6H



Materials Science Forum. 858, pp. 908-912 (2016)

8.1 Previous Results Overview

- 3-stage ring oscillator lasted 3000 hours at 500 °C.
- D to A (4-Bit) IC lasted 10 hours at 500 °C.
- Address decoder (4-bit) IC last 120 hours at 500 °C.
- SRAM Cell (3-3) lasted 9.5 hours at 500 °C.

- Initial "ramp" temperature test had JFET and 3 stage ring oscillator demonstrate short term operation to 727 °C as described at ECS 2015. Use a sapphire wafer for "package." The lead oxide glass based Pt paste die attach material which had been designed for 500 °C operation cause a lost of back side contact.

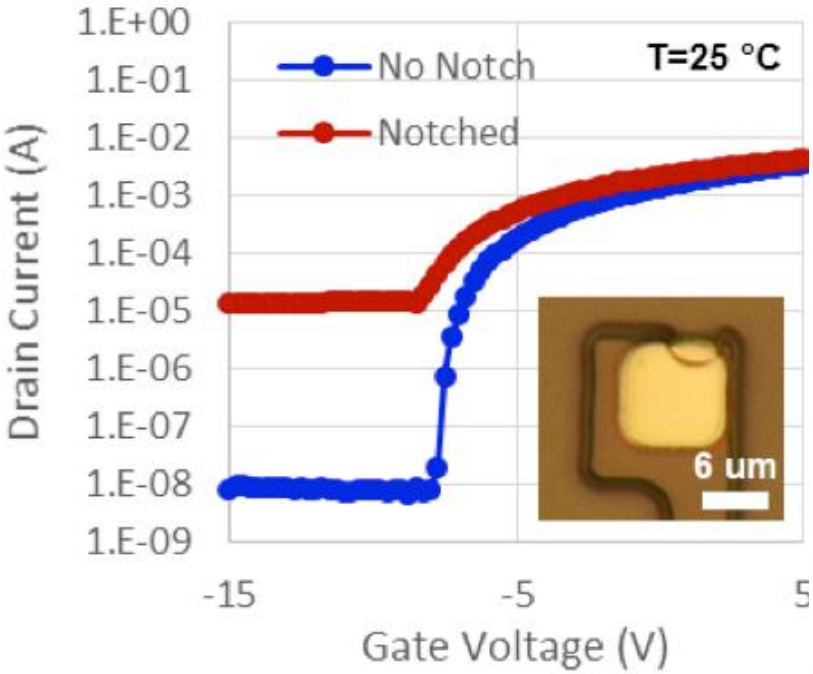
Materials Science Forum. 858, pp. 908-912 (2016)

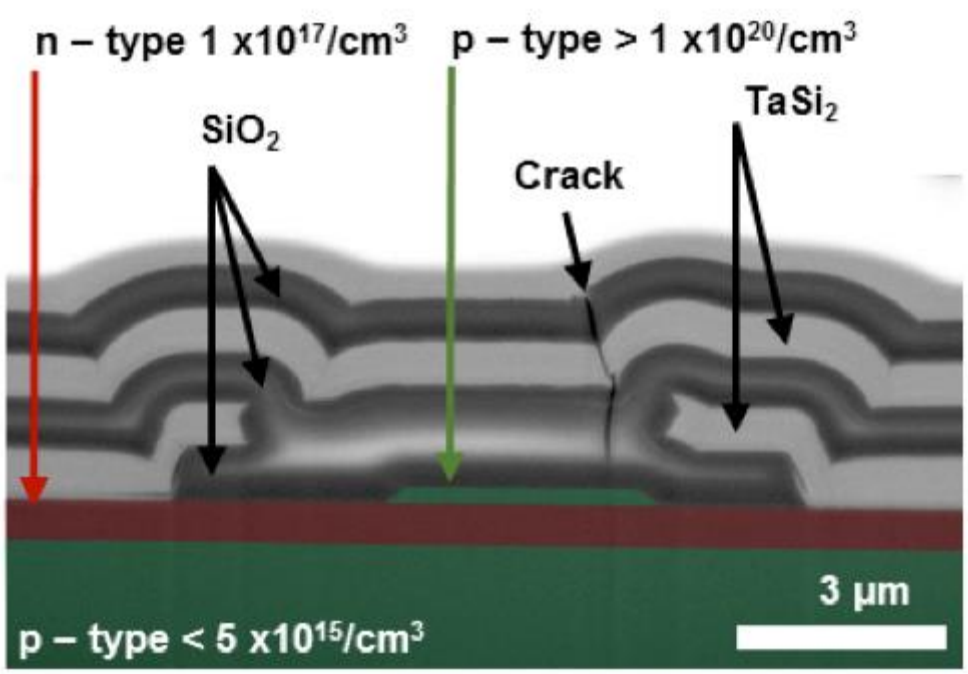
Materials Science Forum. 858, pp. 1112-1116 (2016)

Electrochem. Soc. Trans. [Online]. 69(11), pp. 113-121 (2015)

8.1 Deficiencies

- Crack formation induced fail-open of top metal interconnect.
- Device resistance degradation.
- Gate-to-channel leakage/short from notching of gate etch mask metal.
- Parasitic circuit imbalance induced by mobile ion contamination.



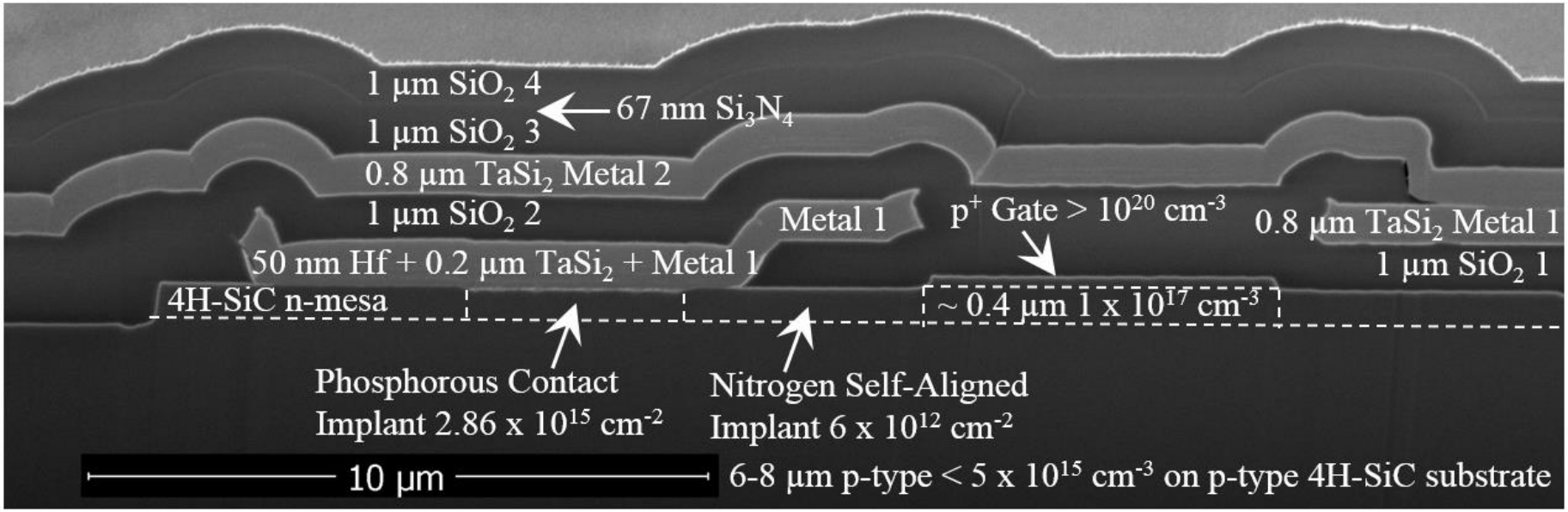


Materials Science Forum. 858, pp. 1112-1116 (2016)

8.1 vs 9.2

Both generations were fabricated with the same process sequence using the same lithographic masks, except for the following differences;

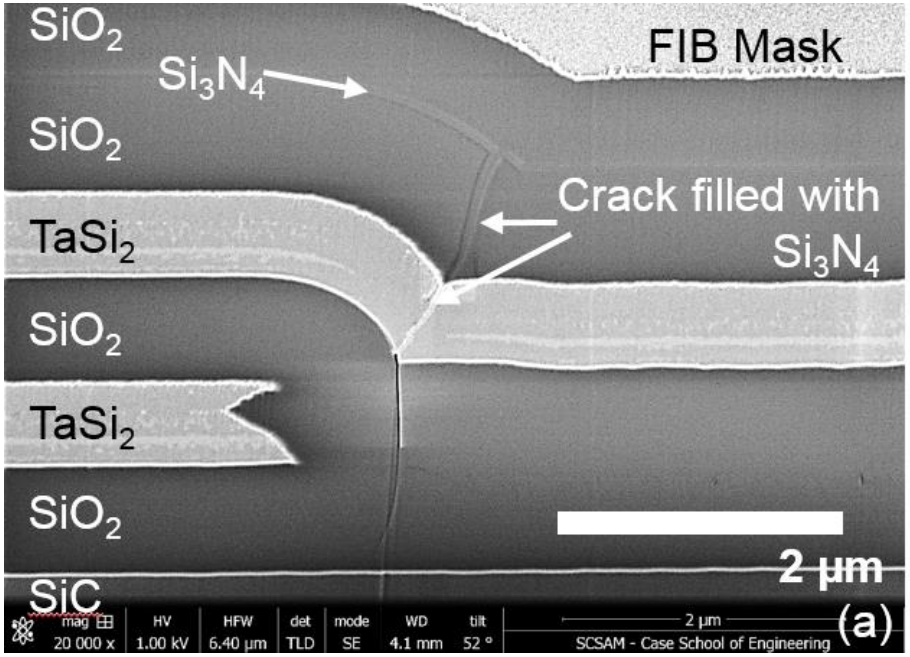
- "Gate notching" defects present in 8.1 JFETs were eliminated for 9.2 JFETs by reduced time delay and improved wafer storage between gate and mesa etches.
- Heavily-implanted SiC contact regions were formed using **P** implantation for 9.2 chips instead of **N** implantation used for 8.1 chips.
- SiC ohmic contact for 9.2 chips was implemented using a 50 nm sputtered **Hf** layer instead of the 50 nm sputtered **Ti** layer used for 8.1 chips.
- The 9.2 process added a **67 nm Si_3N_4** layer between the top two SiO_2 passivation layers.
- Extensive laboratory improvements to mitigate **Na** contamination were implemented for 9.2 wafer processing.



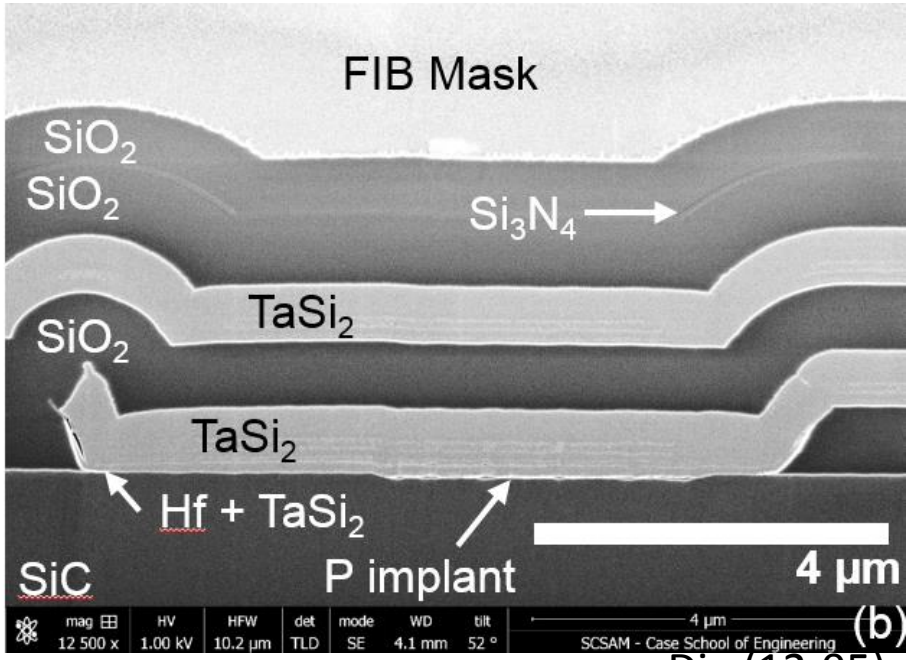
to appear in IEEE Electron Device Letters. (2016)

9.2 Limited Cracking During Si_3N_4 LPCVD

- 9.2 had cracks the formed from too fast of ramp during LPCVD of stoichiometric Si_3N_4.
- The deposited Si_3N_4 held the $TaSi_2$ from splitting upon cooling.
- Only very few paces had any cracks. Image right is example of crack free area on same sample.



Die (12,11)

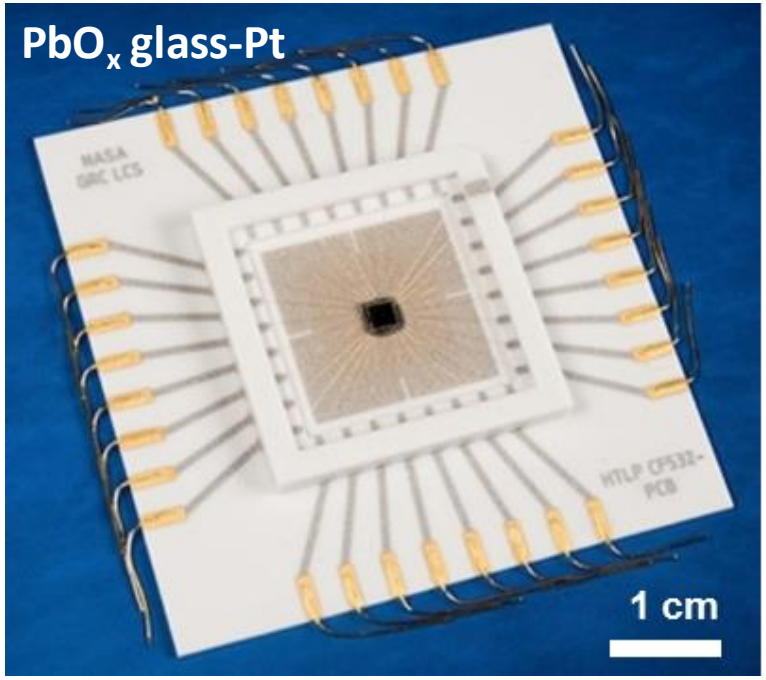


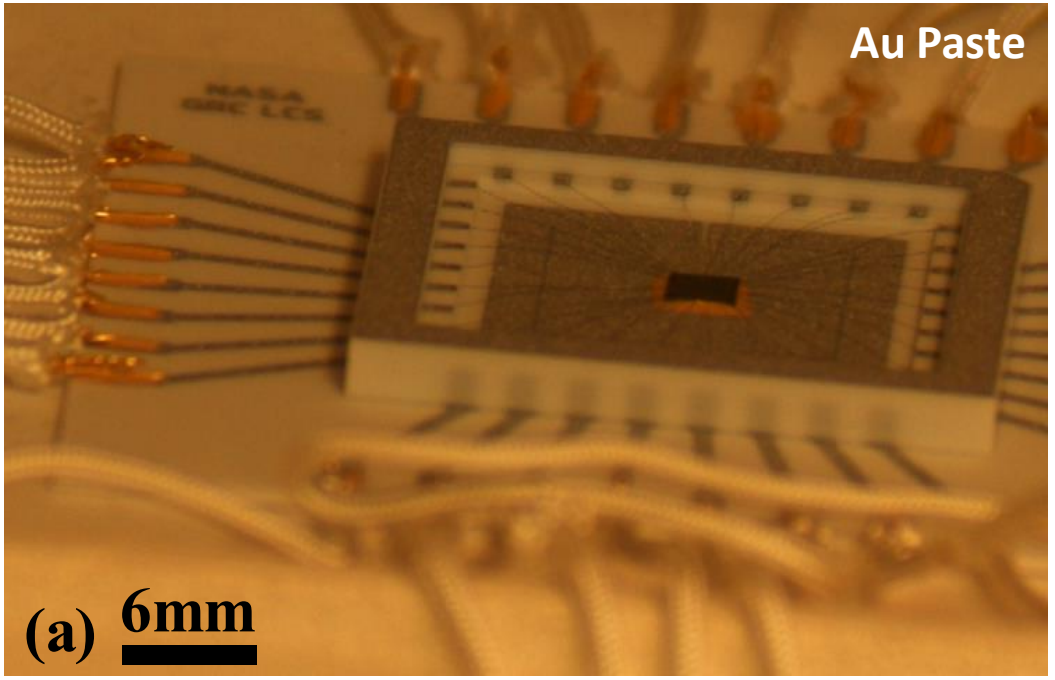
Die (12,05)

New high-T packaging (32 pins)

- All three tests started with a 500 °C burn-in on the order of roughly 100 hours.
- The 931 chip was subjected directly to a ramp to 700 °C following burn-in while the chips for test 6A2 and 924 were cooled back to room temperature prior to ramping to peak testing temperature.

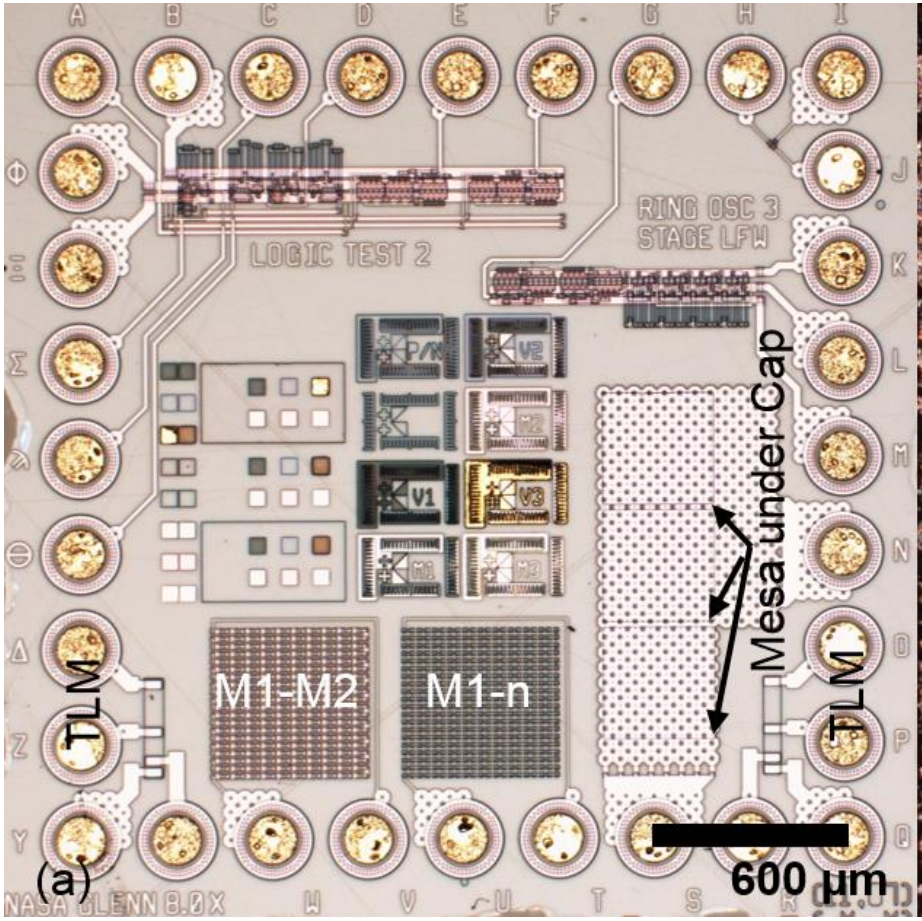
Test #	Design	Si_3N_4	Die Attach	Lid	Hrs @ 500 °C	# of Cycles	Test Temp °C	Hrs at Temp	Last Device Hrs
6A2	8.1	No	PbO_x glass-Pt	No	94	2	727	45.45	27.45
924	9.2	Yes	PbO_x glass-Pt	No	117	2	700	19.2	16.2
931	9.2	Yes	Au Paste	Yes	111	1	700	191.5	143.5

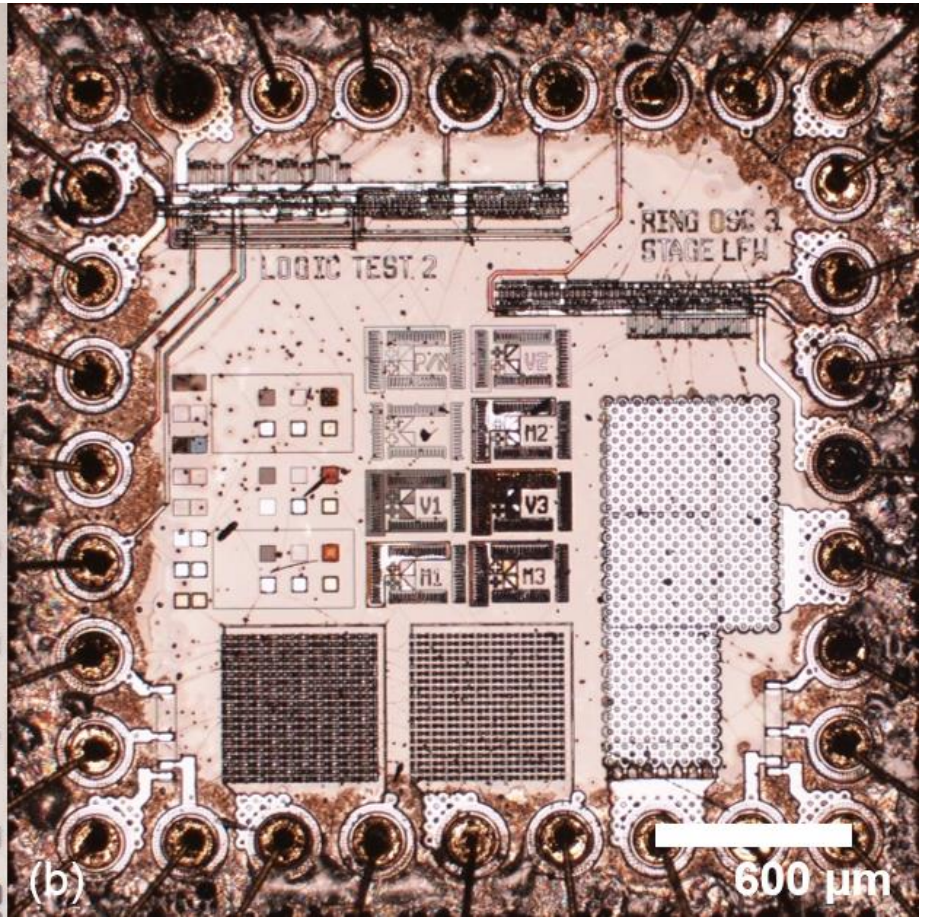




Test #	Design	Si_3N_4	Die Attach	Lid	Hrs @ 500 °C	# of Cycles	Test Temp °C	Hrs at Temp	Last Device Hrs
6A2	8.1	No	PbO_x glass-Pt	No	94	2	727	45.45	27.45

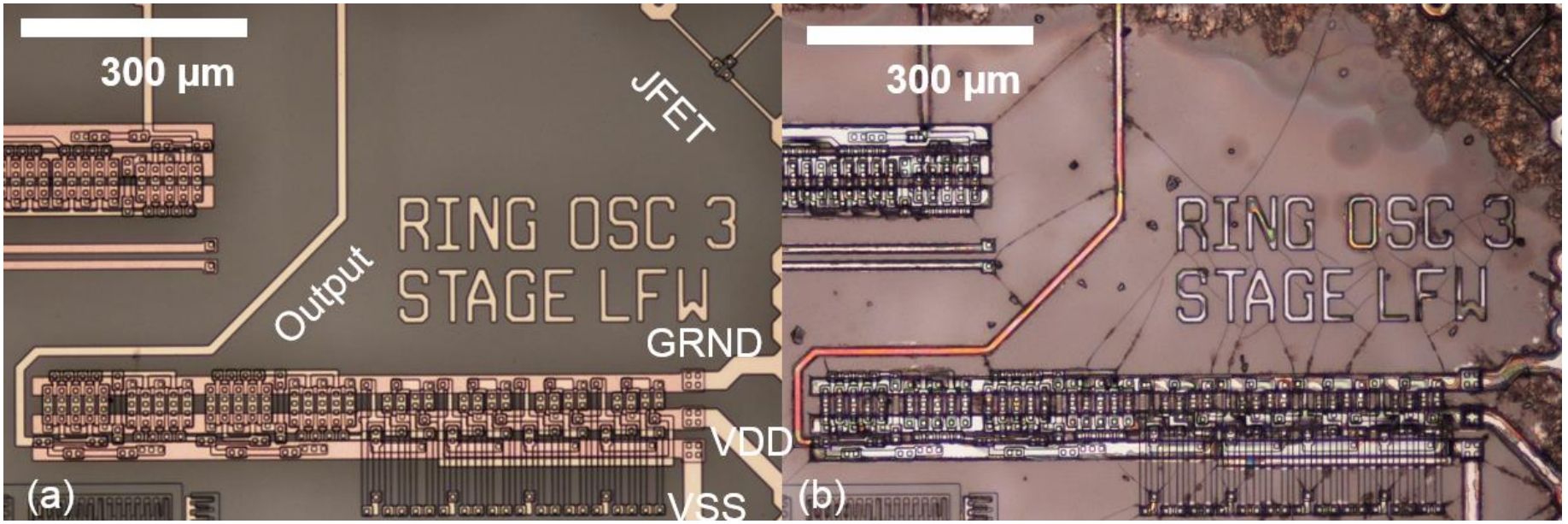
- Before packaging and after testing images of test 6A2.
- Note the amount of lead oxide glass/Pt die attach that has migrated to the area around the bond pads.
- Image (b) also has a lot of particle fallout.





Test #	Design	Si_3N_4	Die Attach	Lid	Hrs @ 500 °C	# of Cycles	Test Temp °C	Hrs at Temp	Last Device Hrs
6A2	8.1	No	PbO_x glass-Pt	No	94	2	727	45.45	27.45

- The lead oxide glass/Pt die attach had completely covered the JFET in the upper right corner of image (b).
- There is a cracking pattern that is more intense at the the label in Metal 1.
- The three stage ring oscillator output trace changed color.
- 3-stage ring oscillator failed before 727 °C testing started.

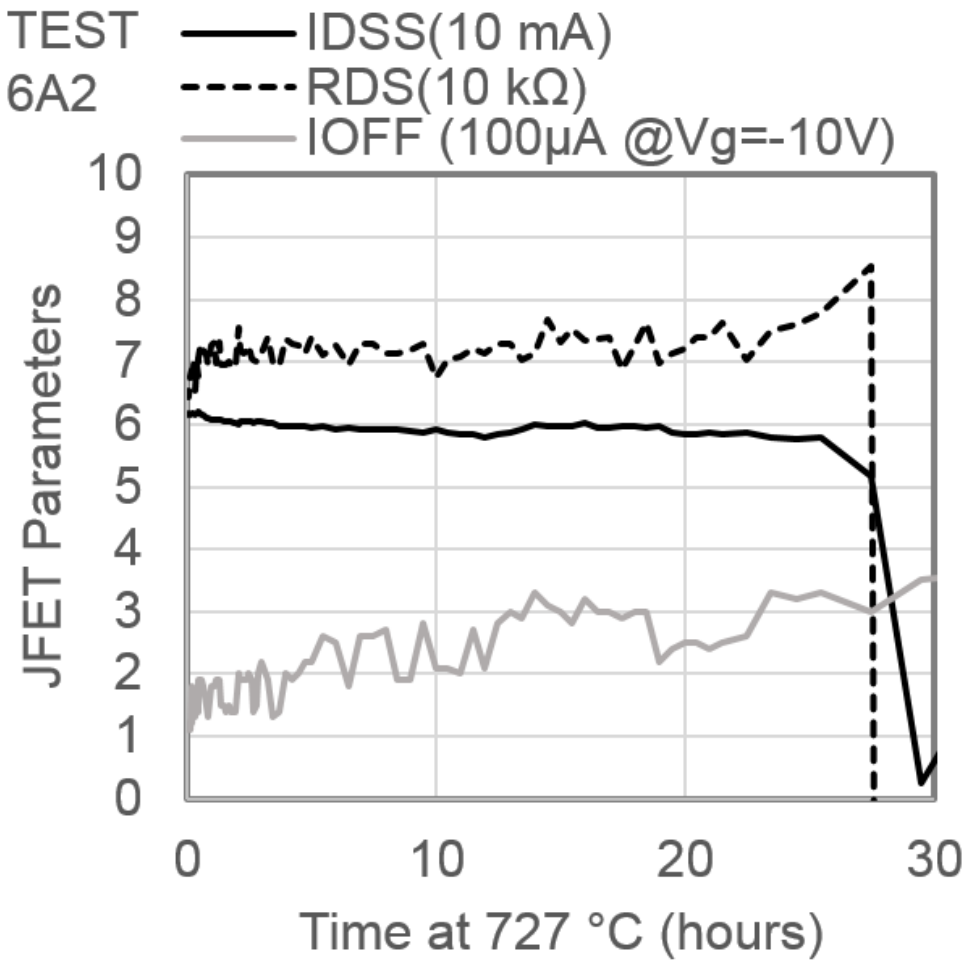


Test #	Design	Si_3N_4	Die Attach	Lid	Hrs @ 500 °C	# of Cycles	Test Temp °C	Hrs at Temp	Last Device Hrs
6A2	8.1	No	PbO_x glass-Pt	No	94	2	727	45.45	27.45

At 727 °C in air ambient

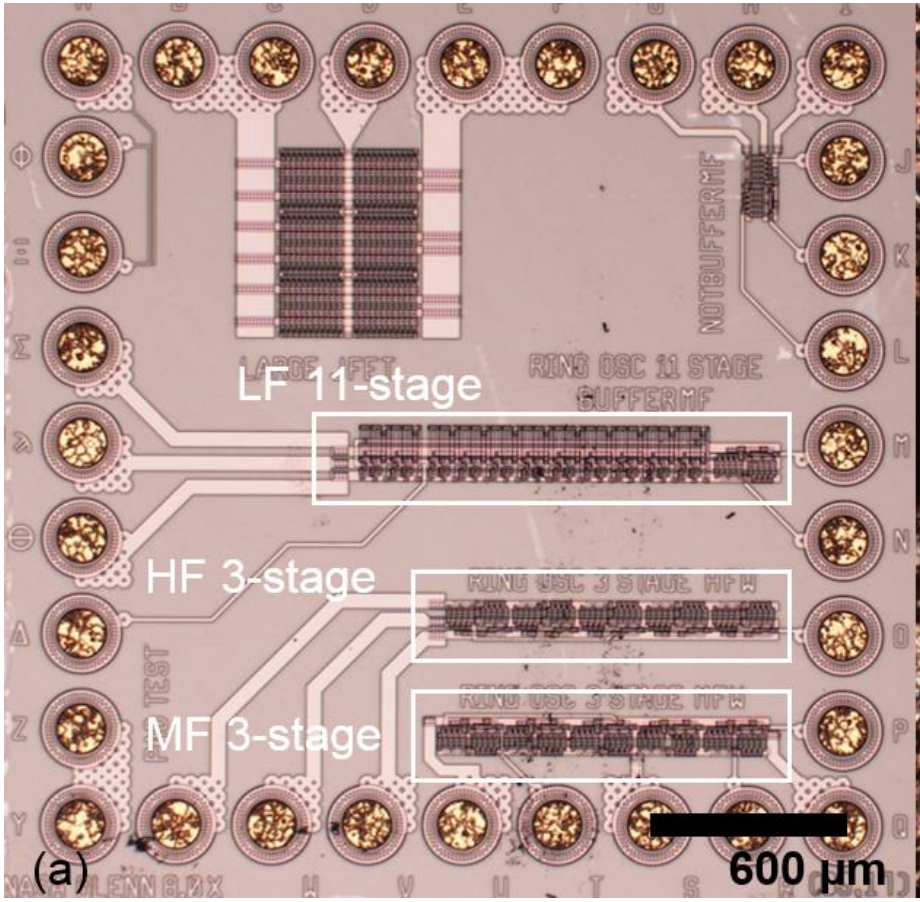
- NOR4 function 60 hrs.
- AND4 function 32 hrs.
- The JFET lasted 25 hrs.
- 0.5mm2 metal-insulator-metal capacitor increased in leakage from 1-2 µA to 10-20 µA gradually over 28 hours.

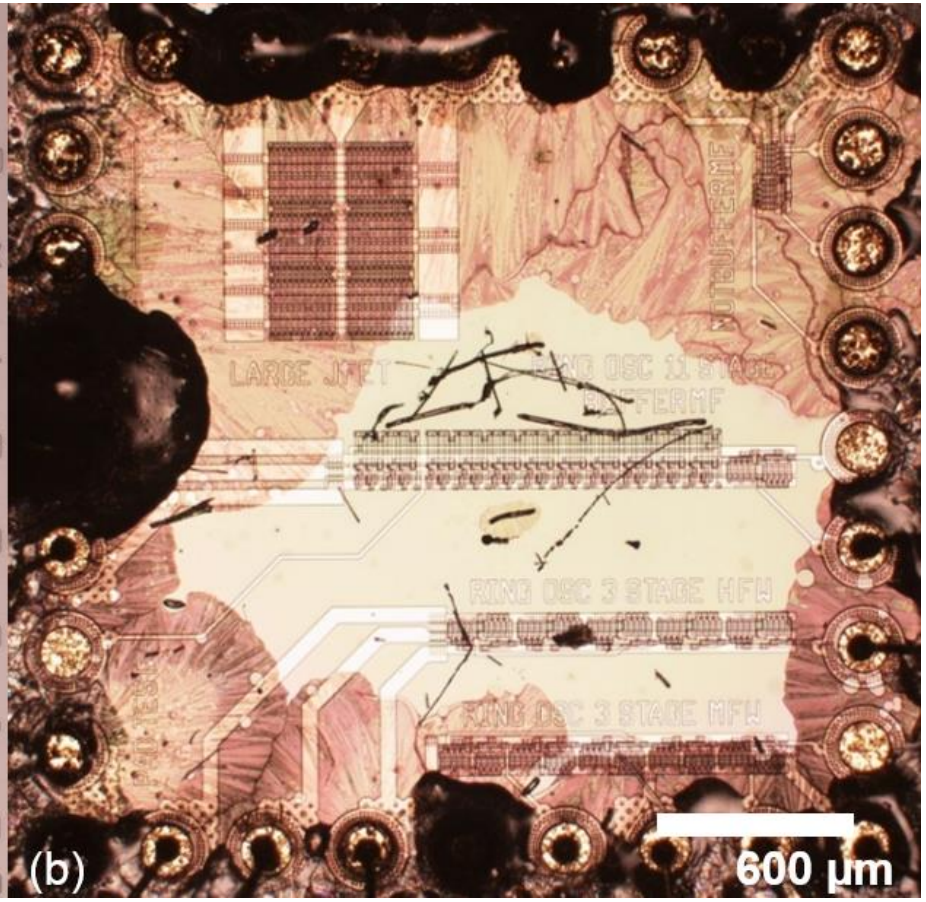
  VSS=-20V, VDD=20V



Test #	Design	Si_3N_4	Die Attach	Lid	Hrs @ 500 °C	# of Cycles	Test Temp °C	Hrs at Temp	Last Device Hrs
924	9.2	Yes	PbO_x glass-Pt	No	117	2	700	19.2	16.2

- Although the temperature was 27 °C lower and the time at test temperature was less, the amount of lead oxide glass/Pt die attach migration was much worse.
- LF, MF, and HF = low, medium, and high frequency. <u>NO CRACKING.</u>

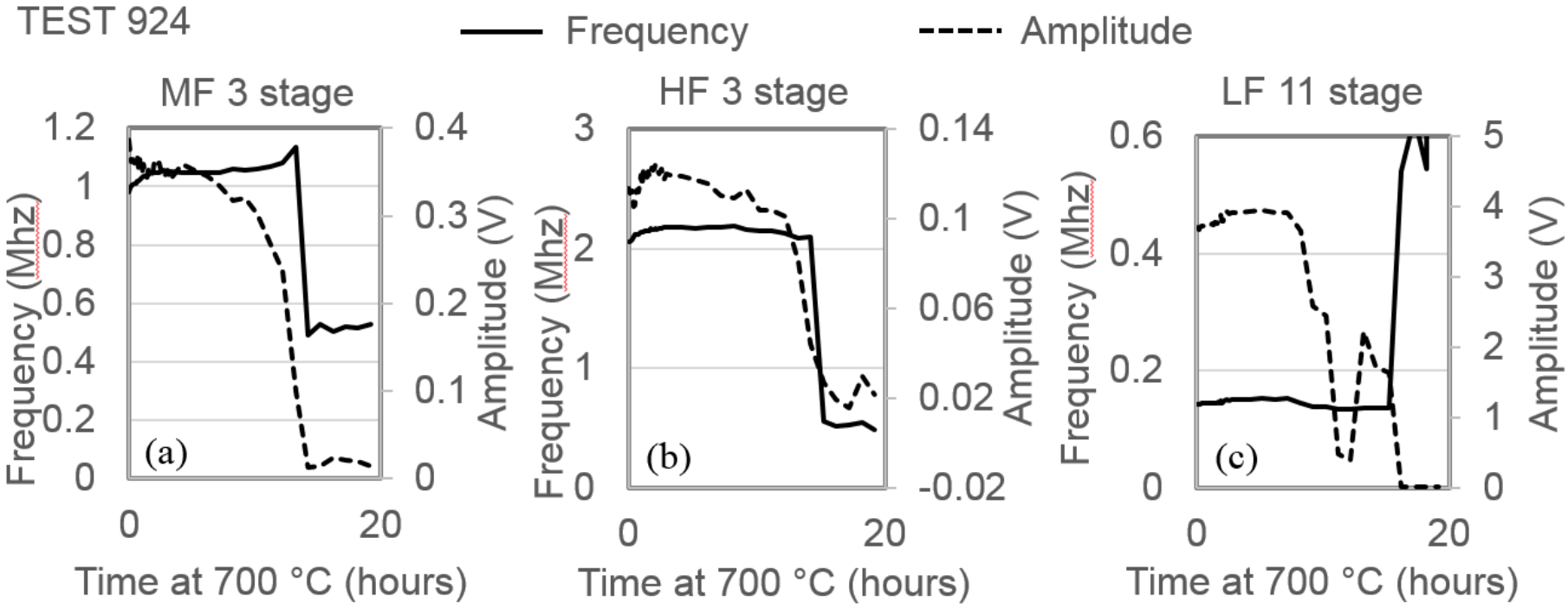




Test #	Design	Si_3N_4	Die Attach	Lid	Hrs @ 500 °C	# of Cycles	Test Temp °C	Hrs at Temp	Last Device Hrs
924	9.2	Yes	PbO_x glass-Pt	No	117	2	700	19.2	16.2

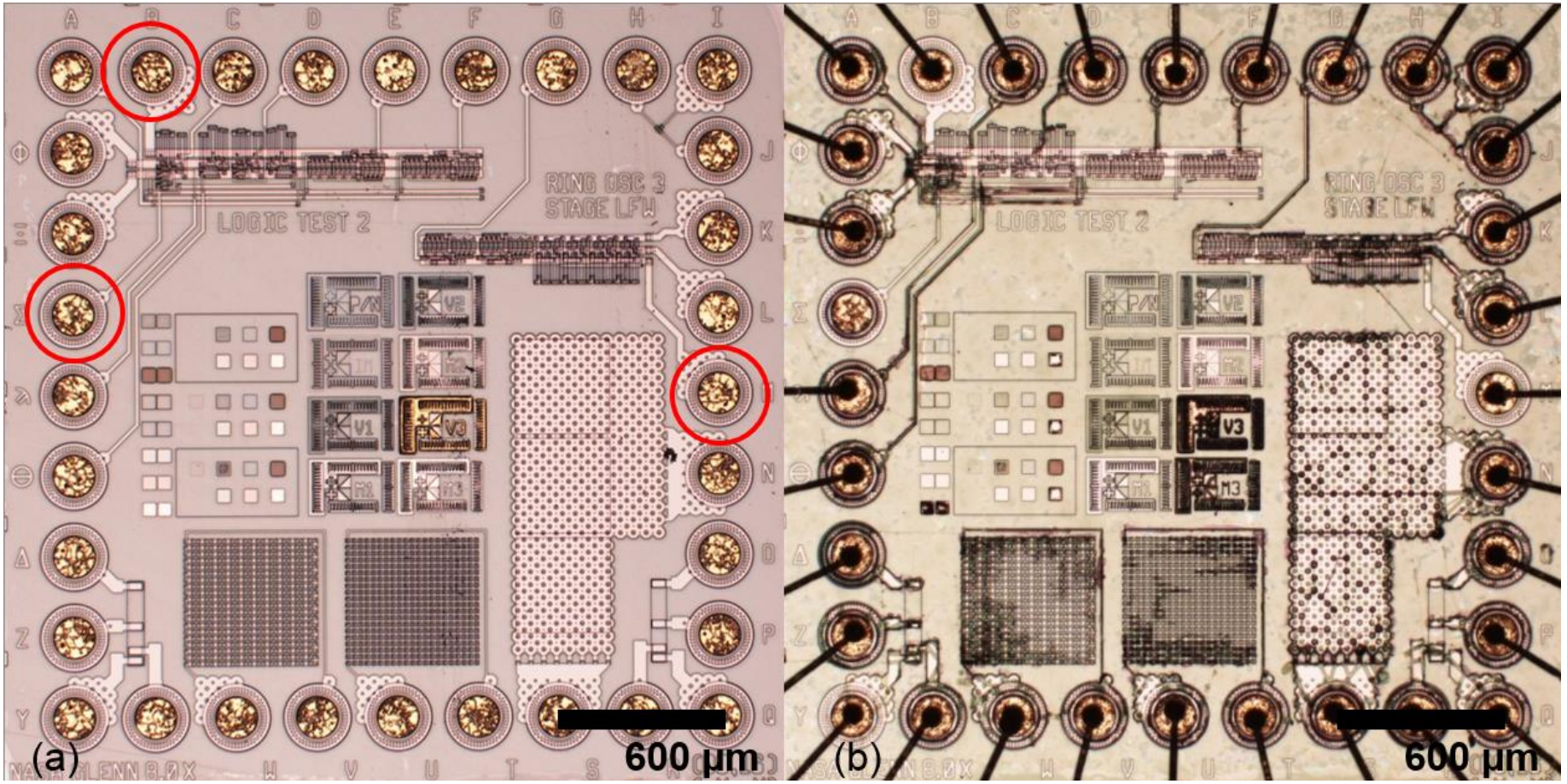
- Plot of frequency and amplitude output of 3 different ring oscillators
- HF lasted the longest possibly since it had the least lead oxide on it.
- LF had an intermittent failure at 10 hours.
- All three the output amplitude first started to drop at 8 hours.

VSS=-20V and VDD=25V



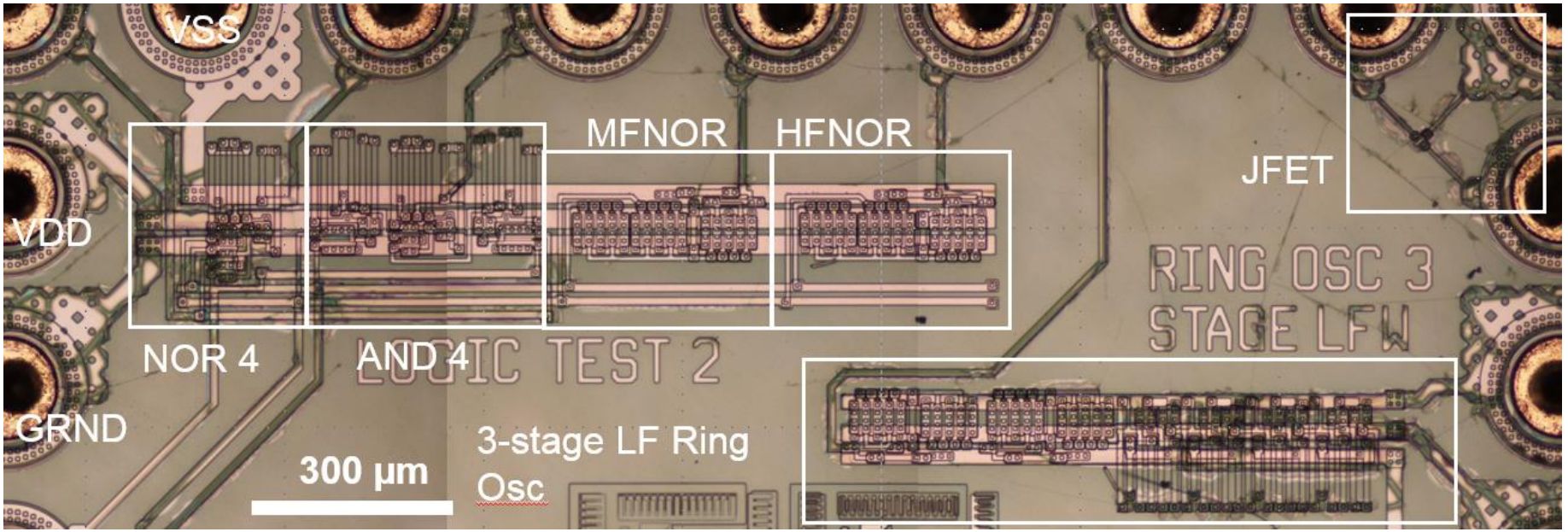
Test #	Design	Si_3N_4	Die Attach	Lid	Hrs @ 500 °C	# of Cycles	Test Temp °C	Hrs at Temp	Last Device Hrs
931	9.2	Yes	Au Paste	Yes	111	1	700	191.5	143.5

- No die attach migration or debris fallout - Au paste was used and lid covered the die.
- Circle in red on image (a) are three bond pads that did not show any aging and only near other traces or device was there any cracking. The areas circled in red were no biased or at VSS which was also the same potential as the backside of the die.



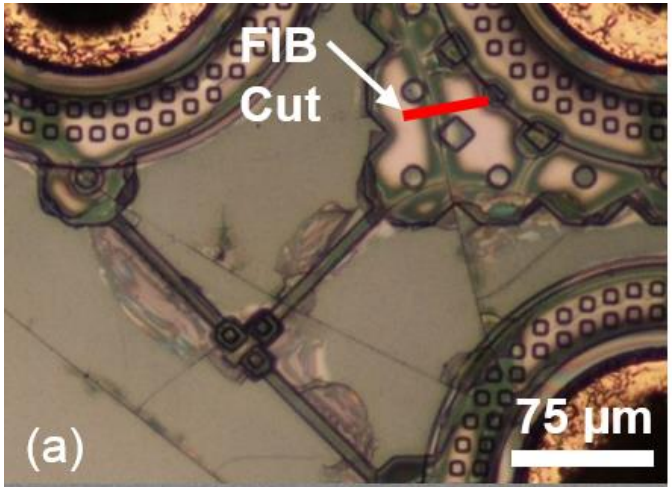
Test #	Design	Si_3N_4	Die Attach	Lid	Hrs @ 500 °C	# of Cycles	Test Temp °C	Hrs at Temp	Last Device Hrs
931	9.2	Yes	Au Paste	Yes	111	1	700	191.5	143.5

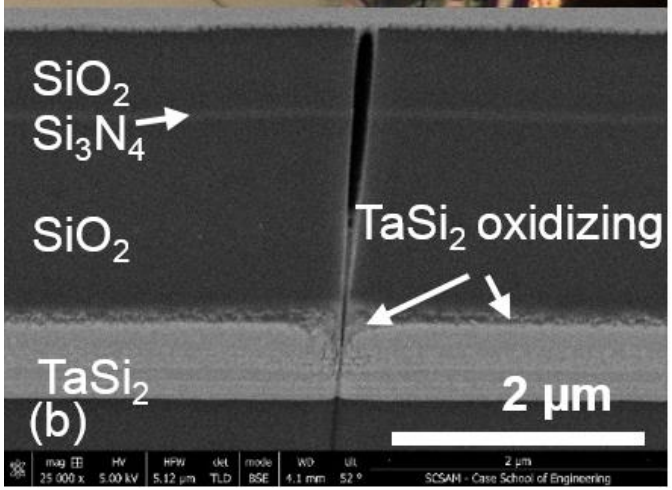
- A higher magnification optical micrograph of the top part of die (8,16) in test 931 after electrical testing for 191.5 hours at 700 °C.
- Note the absence of die attach migration or debris fallout since Au paste was used and lid covered the die.
- Only dielectric cracking and $TaSi_2$ oxidation are evident.
- An even larger view of the JFET area can be seen in the next slide.

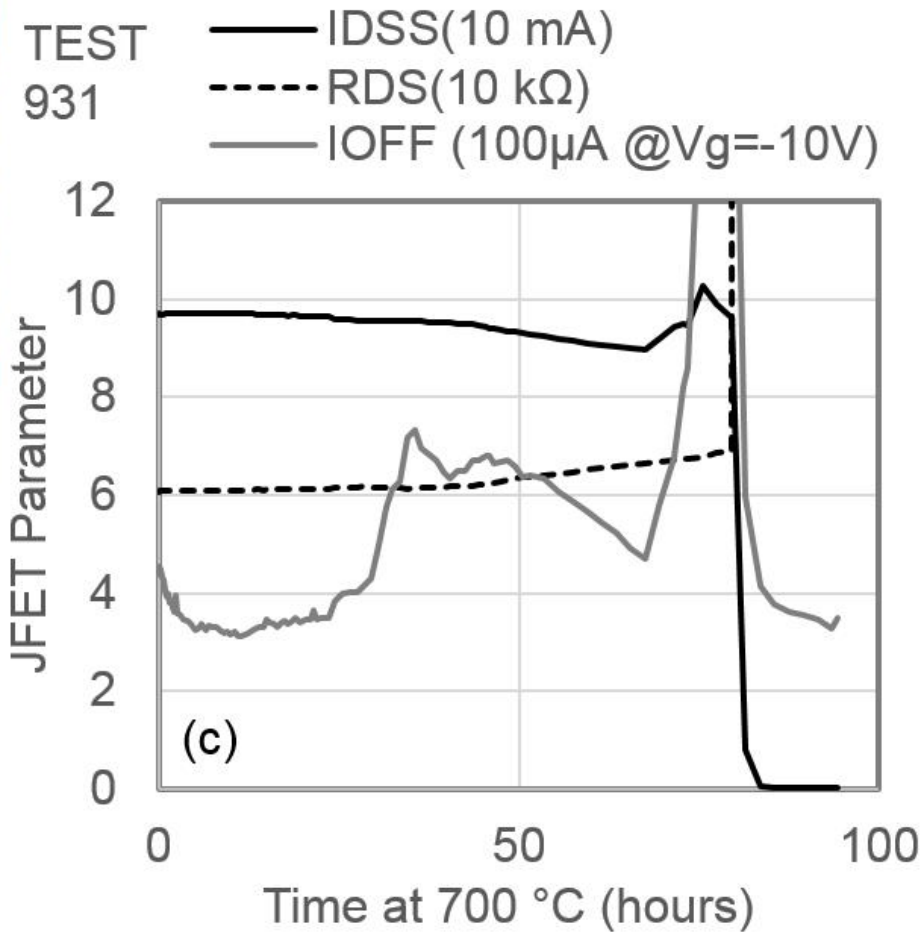


Test #	Design	Si_3N_4	Die Attach	Lid	Hrs @ 500 °C	# of Cycles	Test Temp °C	Hrs at Temp	Last Device Hrs
931	9.2	Yes	Au Paste	Yes	111	1	700	191.5	143.5

- (b) FESEM image of a FIB prepared cross-section of a crack. The crack allowed the $TaSi_2$ to oxidize.
- (c) JFET IOFF started shifting at 25 hour but with did not fail like 6A2.



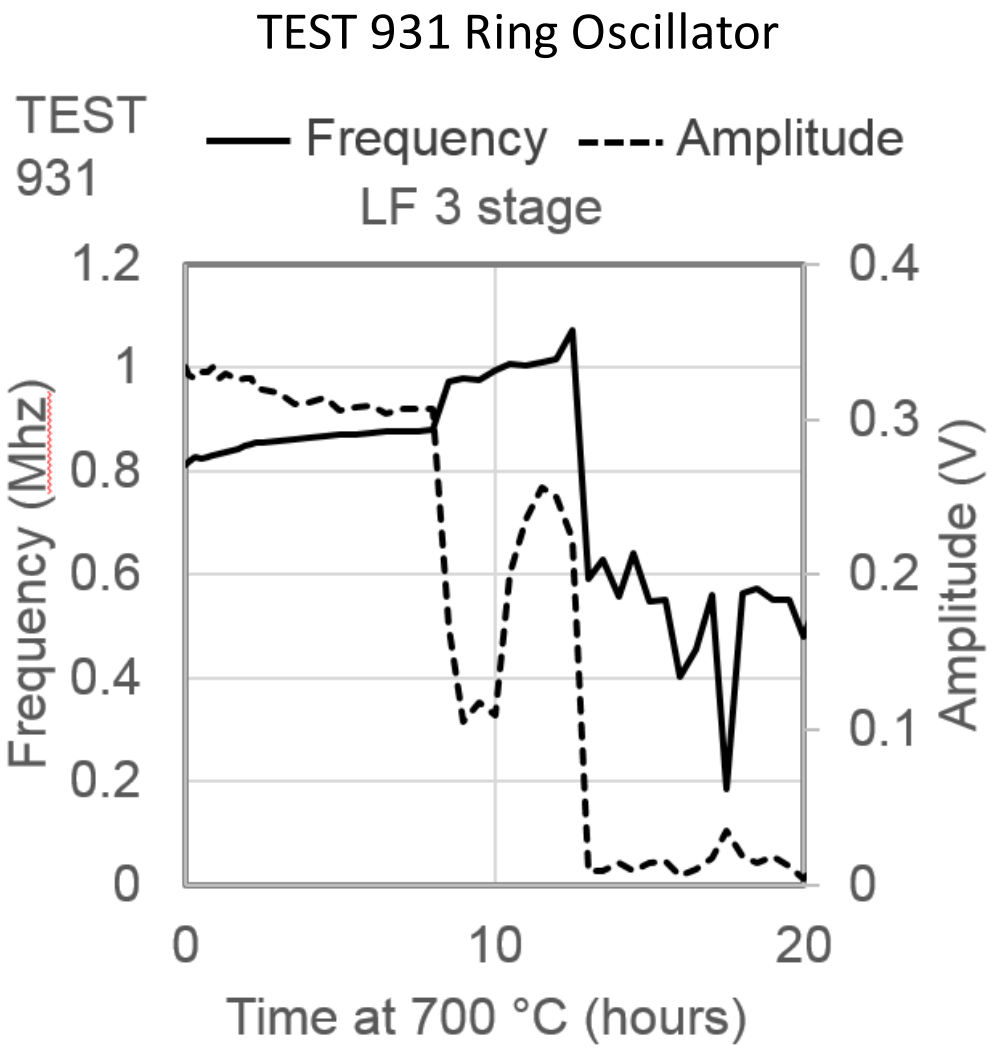




Test #	Design	Si_3N_4	Die Attach	Lid	Hrs @ 500 °C	# of Cycles	Test Temp °C	Hrs at Temp	Last Device Hrs
931	9.2	Yes	Au Paste	Yes	111	1	700	191.5	143.5

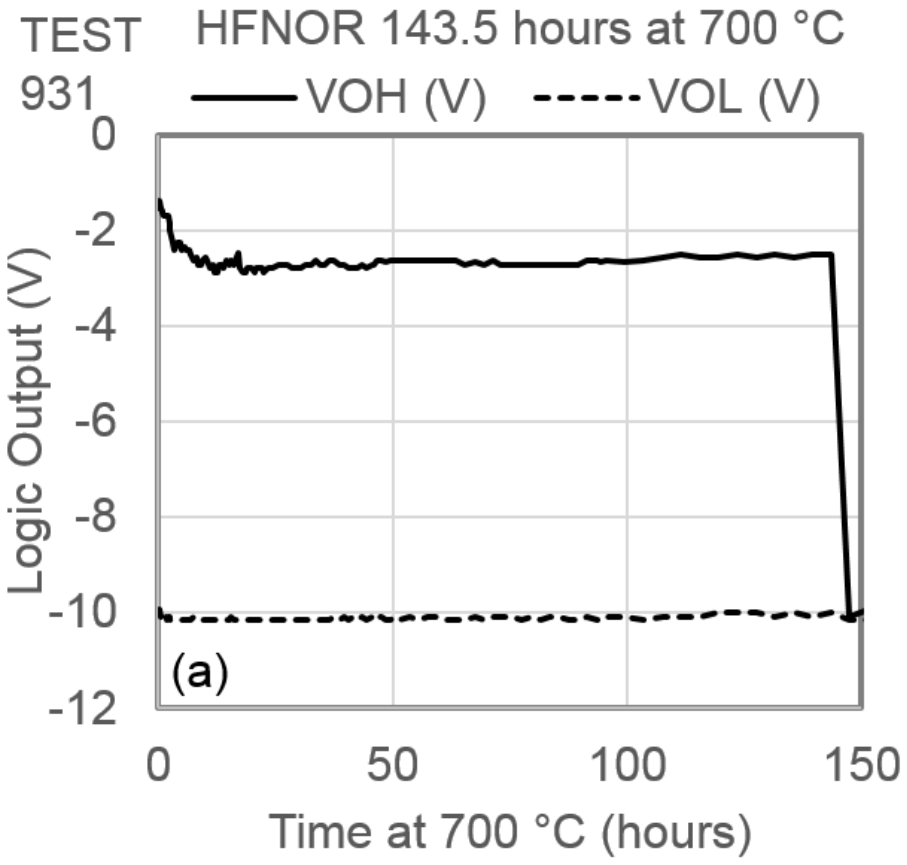
- The LF 3-stage ring oscillator of test 931 started to fail intermittently at 8 hours, similar to the LF 11 stage from 924.
- The three ring oscillators of test 924 and the ring oscillator of test 931 (shown right) all exhibited a shift in amplitude 8 hours into 700 °C testing suggests a possibly common mode/location of failure for these integrated circuits.

VSS=-25V and VDD=25V

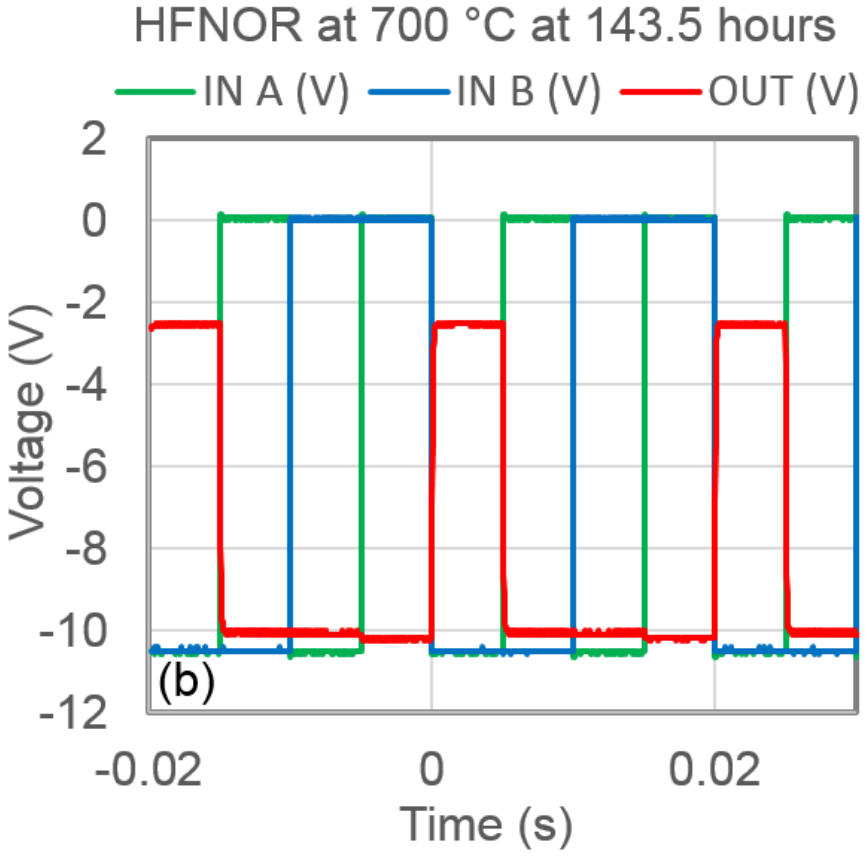


Test #	Design	Si_3N_4	Die Attach	Lid	Hrs @ 500 °C	# of Cycles	Test Temp °C	Hrs at Temp	Last Device Hrs
931	9.2	Yes	Au Paste	Yes	111	1	700	191.5	143.5

Output high and output low values as functions of time at 700 °C



The input and output wave forms for the HF NOR



MFNOR on 931 also lasted 143.5 hours at 700 °C VSS=-25V and VDD=25V

Conclusion

- Preliminary accelerated IC testing experiments at temperatures above 700 °C indicate that Au paste should be used for die attach at 700 °C instead of the lead oxide glass based Pt paste which had been designed for 500 °C operation.
- The formation of cracks in dielectric (SiO_2-Si_3N_4-SiO_2) overlying the IC interconnect, which induced oxidization and cracking of the $TaSi_2$ interconnect, was observed to be a limiting factor in our current 4H-SiC JFET IC process.
- Failure was not observed with T ≥ 700 °C for the 32 pin package, the SiC 4H-JFET structure, the Hf ohmic contacts, or $TaSi_2$ in regions free of dielectric cracks.
- If process revisions can eliminate overlying dielectric crack formation then highly durable 4H-SiC JFET integrated circuits for temperatures as high as 700 °C may become achievable.

Acknowledgements

Funded by **NASA Transformative Aeronautics Concepts Program**

HX5 Sierra

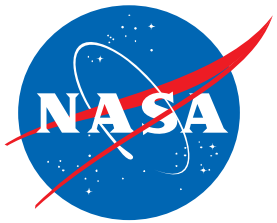
- Kelley Moses
- Jose Gonzalez
- Michelle Mrdenovich

NASA Glenn Research Center

- Gary Hunter
- Robert Buttler
- Roger Meredith

Case Western Reserve University

- Amir Avishai


NASA

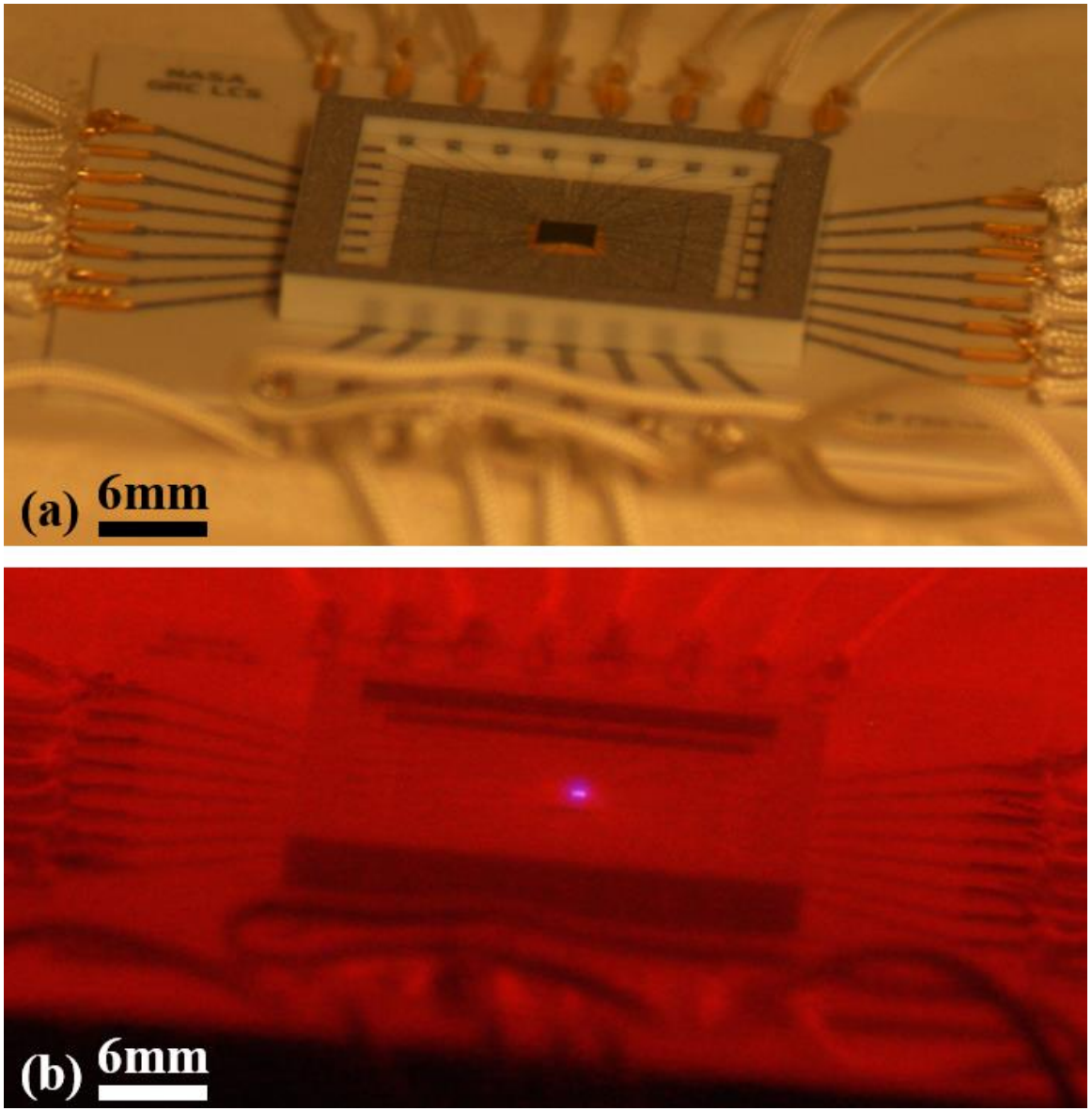


Fig. 10. (a) Optical image of packaged device with room light illumination. (b) Optical image at 650 °C of packaged device with a large JFET under forward bias of the gate-channel junction resulting in blue light emission. Three ring oscillators and a MF NOT are also operating while the image is taken.

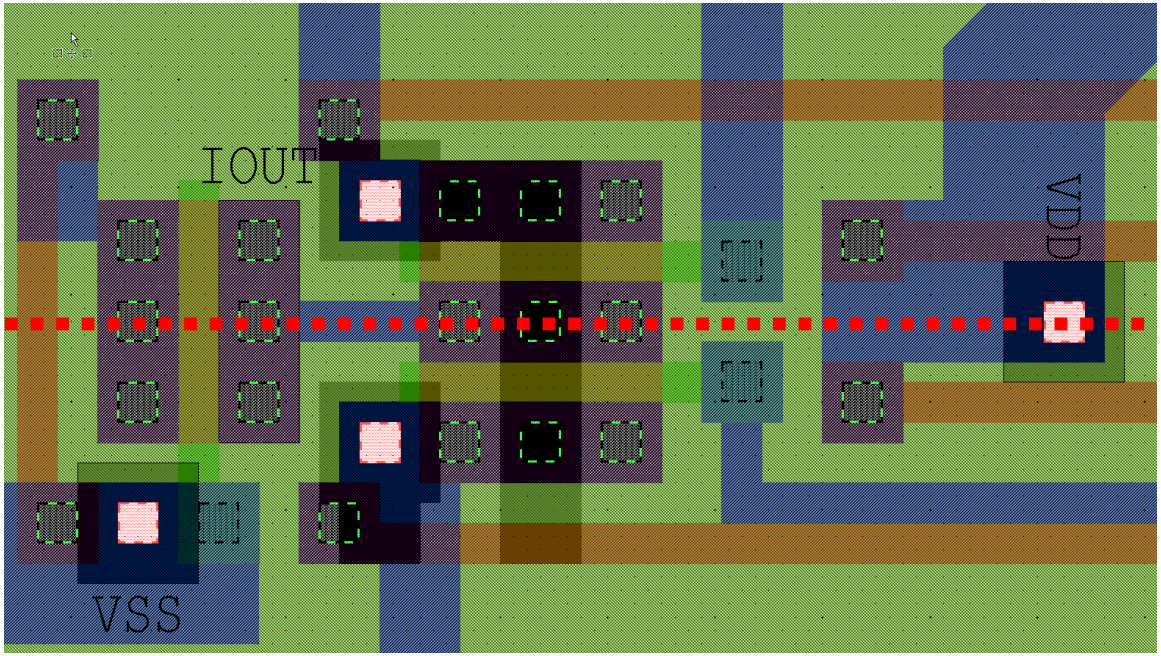
to appear in HiTEC 2016

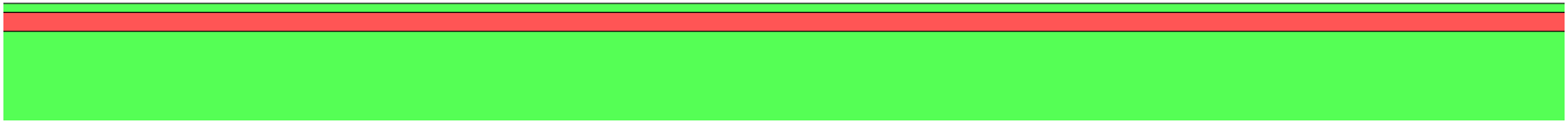
Integrated circuits in fabrication

Circuit	Inputs	Outputs	Transistors, I/O Pads	Comments
4-Bit A/D	Analog voltage signal, optional external clock, output type select	4 bit parallel digital latch, pulse width modulated (PWM)	203 JFETs, 23 I/Os	Internal ring-oscillator clock circuit
4X4 Bit Static RAM	Read, Write, Data Lines, Address Lines	4 bit parallel digital latch, pulse width modulated (PWM)	220 JFETs, 30 I/Os	Address decoder, sense amplifiers
Source Separation Sensor Signal Transmitter	Capacitive sensor	Frequency modulated with address code	301 JFETs, 20 I/Os	Each sensor signal is tagged with unique address code
Ring Oscillators	Capacitive sensors	Frequency modulated signals (up to 500 MHz)	10-12 JFETs, 6 I/Os	On-chip large transistors for power amplification
Binary Amplitude Modulation RF Transmitter	Low power binary signal	High-Power RF signal to antenna		Could connect with PWM from A/D
Op Amp, 2-Stage	Differential	Voltage gains to 50 w/ on-chip resistors	10 JFETs	For piezoelectric SiC pressure sensors
4-Bit D/A	4 digital	1 analog	20 JFETs	

Process with two levels of metal interconnect

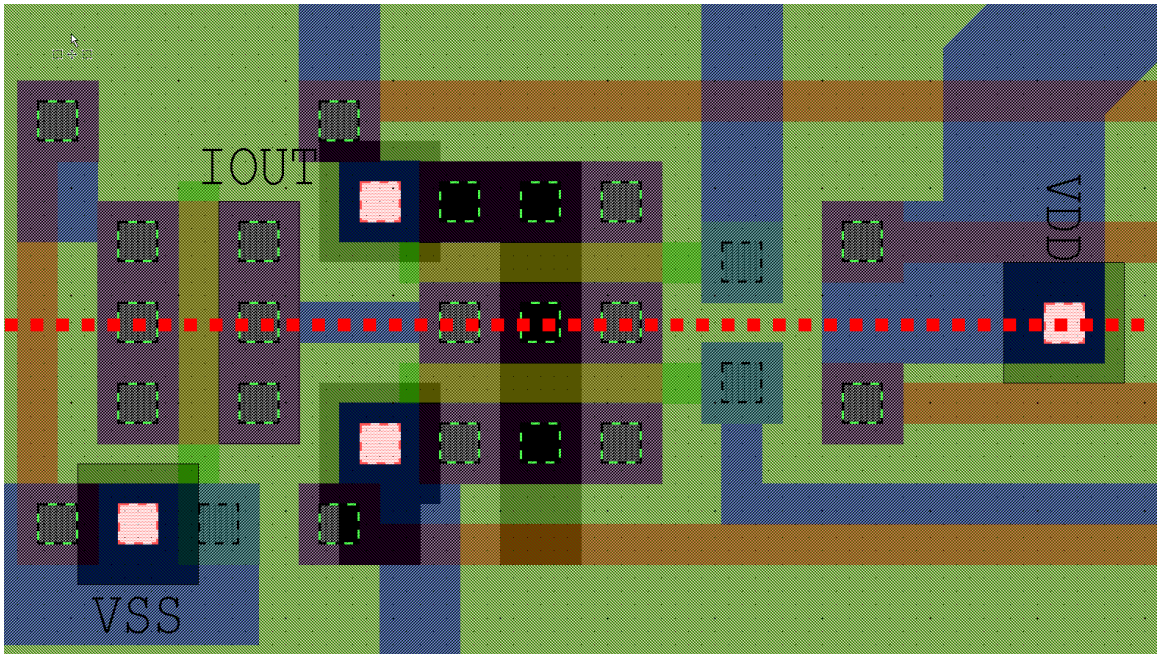
- Gate $N_A > 2 \times 10^{20}$ cm^{-3}
  at 0.17µm thick
- n-channel 1×10^{17} cm^{-3}
  at ~0.5 µm thick
- Lower p material
  $< 3 \times 10^{15}$ cm^{-3}
  at ~6-8 µm thick.

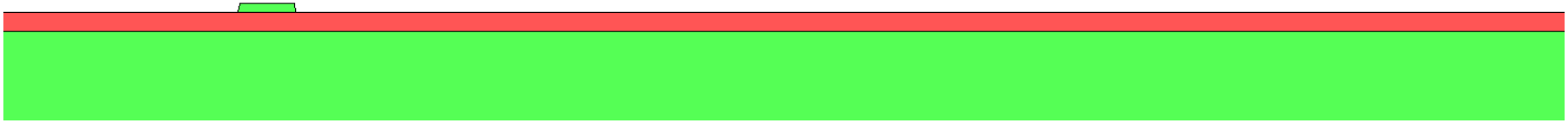




Process with two levels of metal interconnect

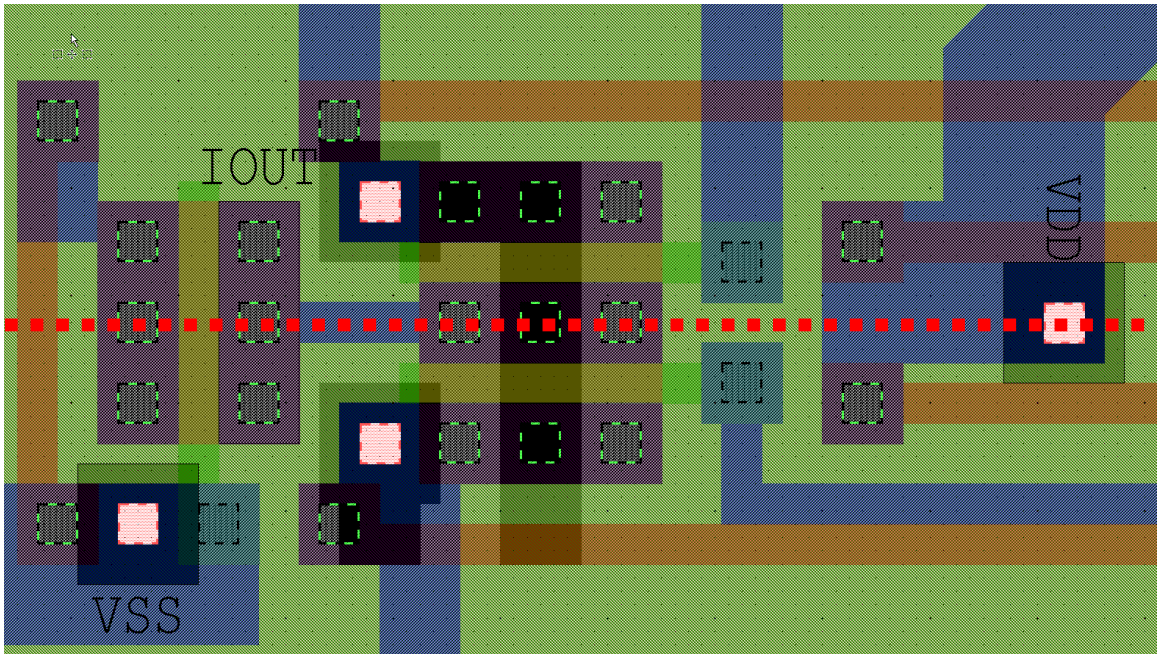
- Ti/Ni etch mask for gate.
- Self align nitrogen implant of dose 7.0 x $10^{12}cm^{-2}$ at 70 KeV.

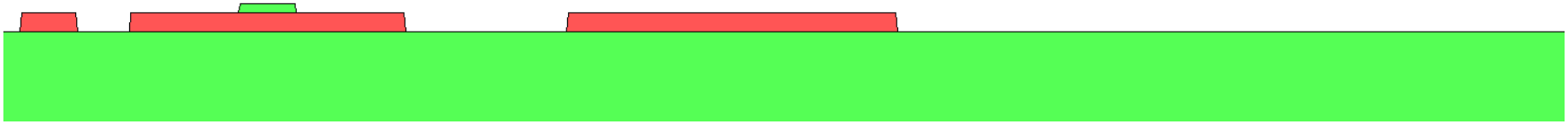




Process with two levels of metal interconnect

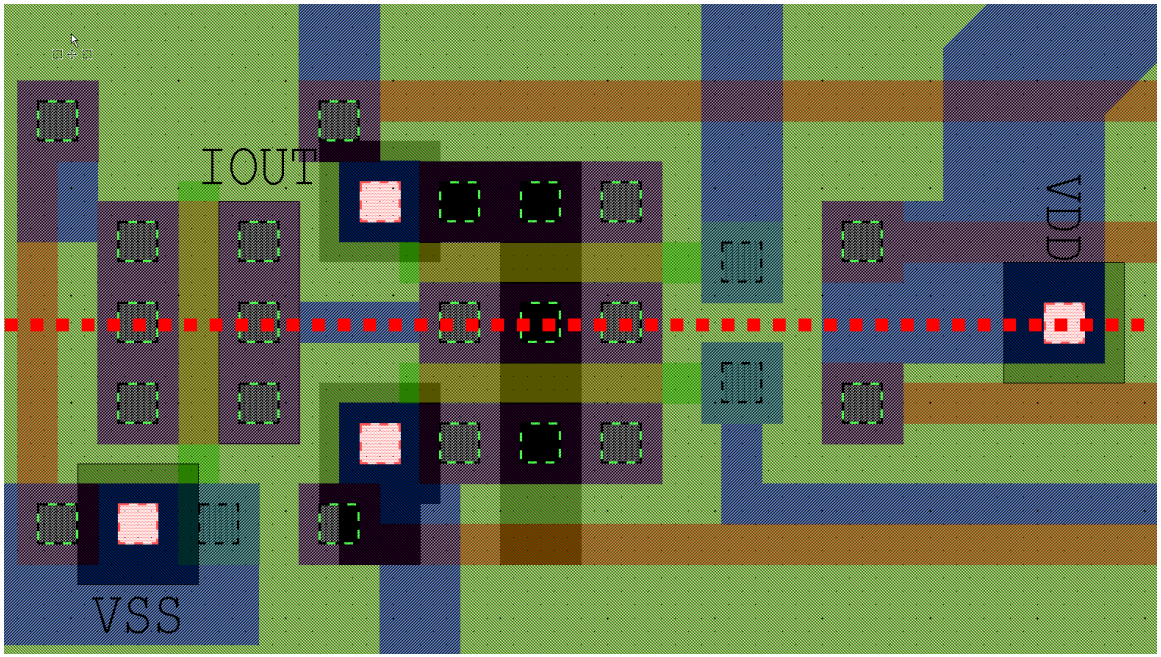
- Ti/Ni mask use to define resistors and channels.

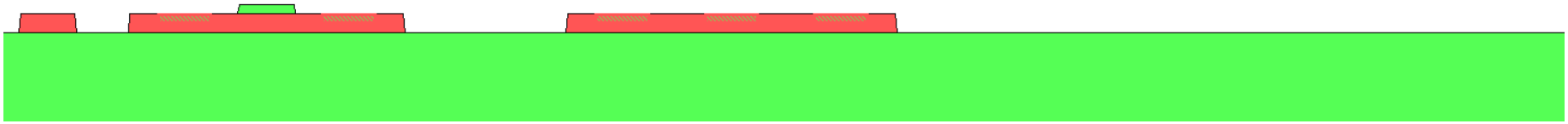




Process with two levels of metal interconnect

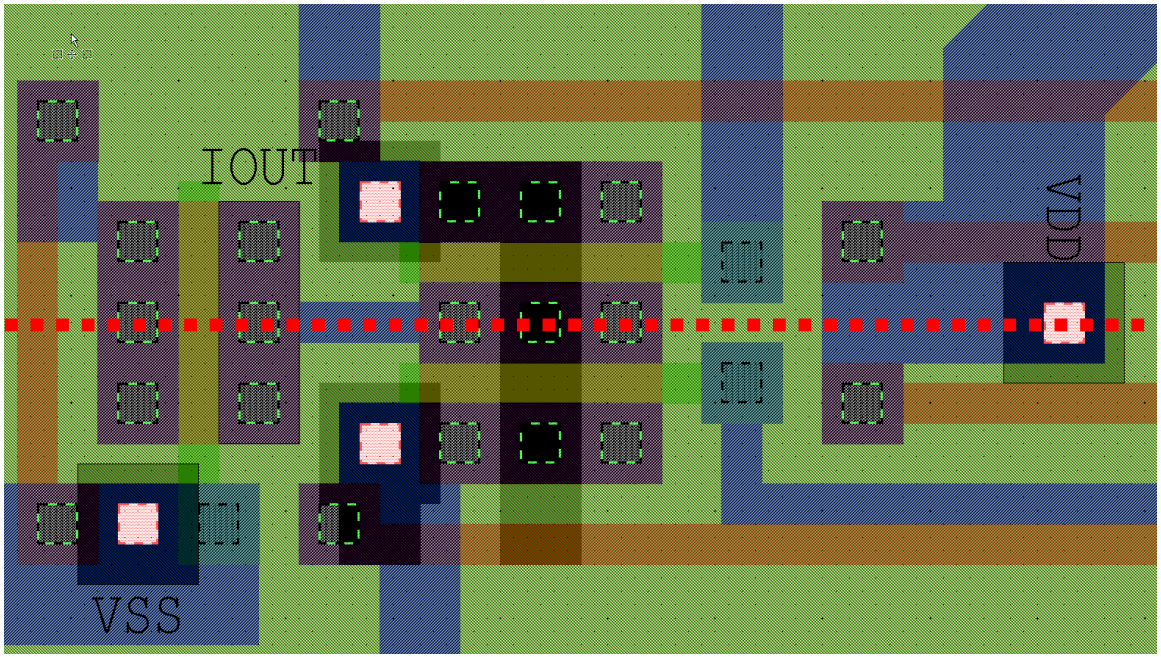
- Si mask was used for box implant of 1.6 x 10^{15} cm^{-2} while heated to 873 K.
- Capped and annealed at 1633 K for 4 hours in N_2.

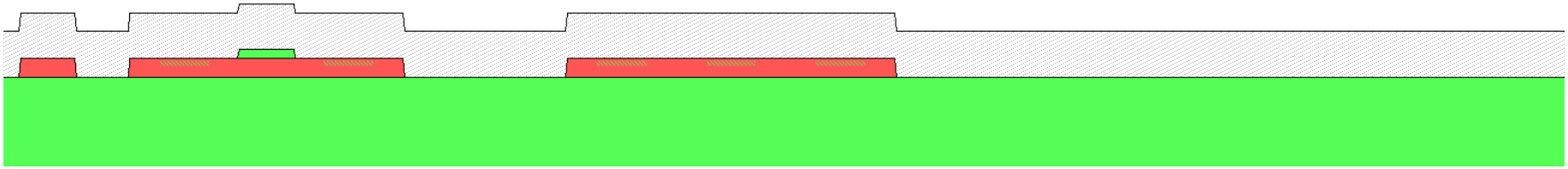




Process with two levels of metal interconnect

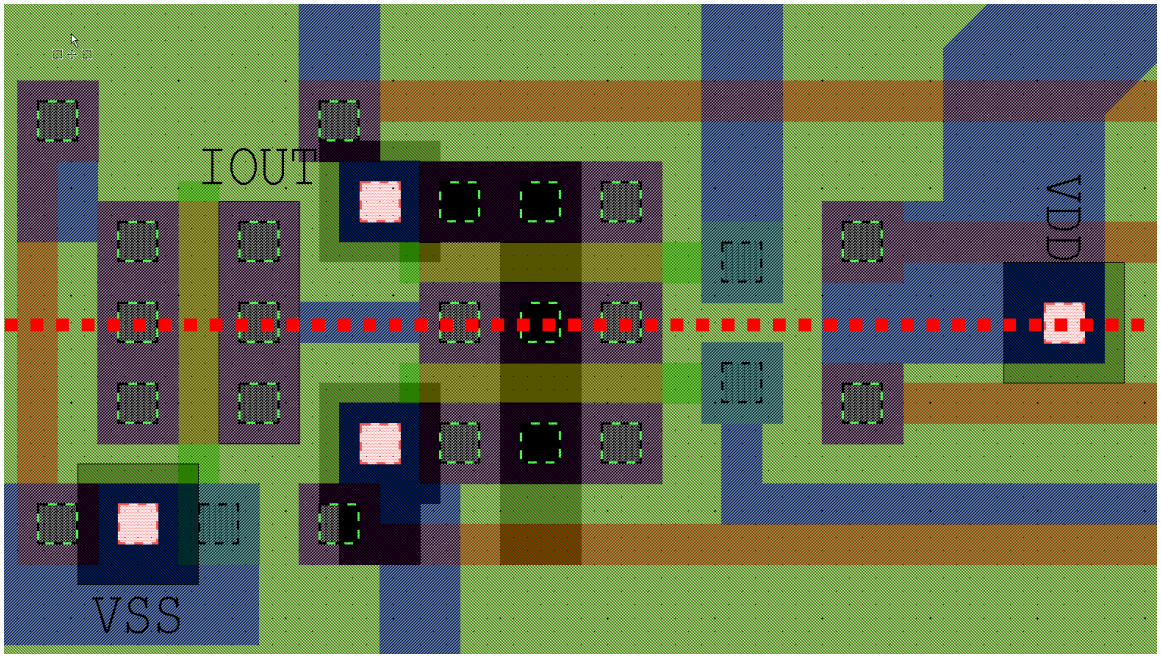
- Thermal and deposited oxide.

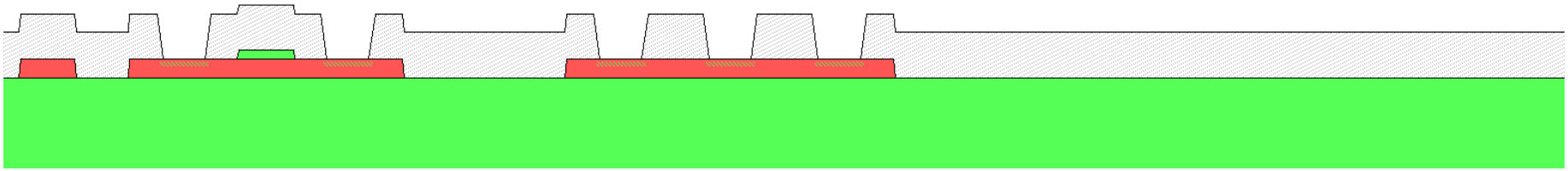




Process with two levels of metal interconnect

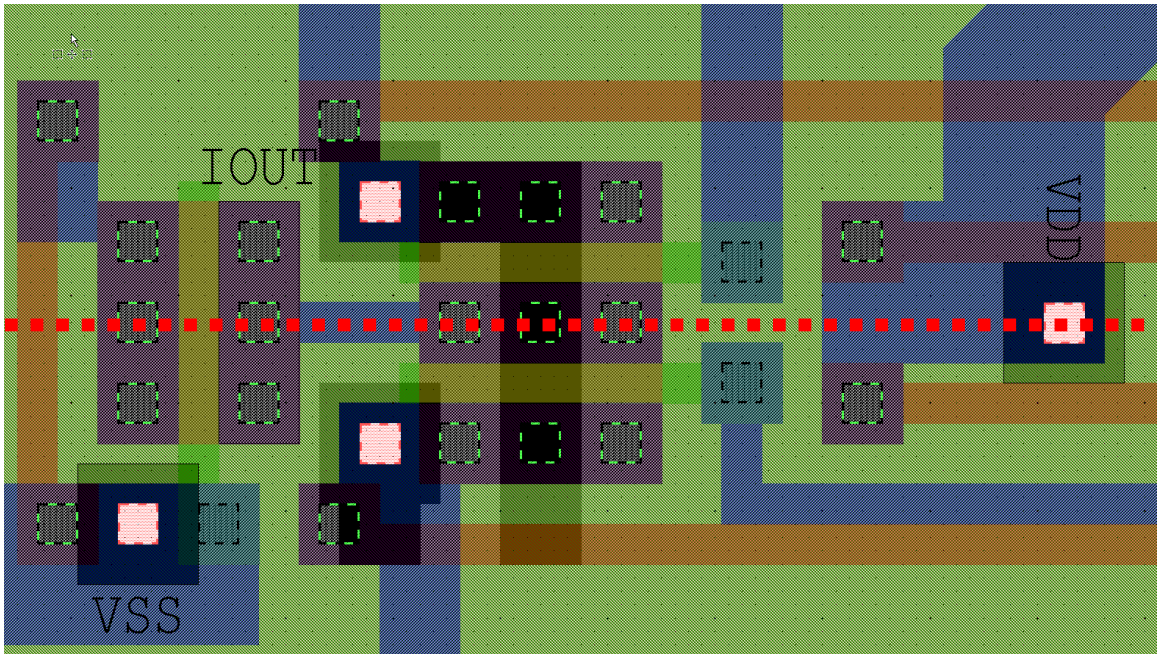
- Dry and wet etch of via 1.

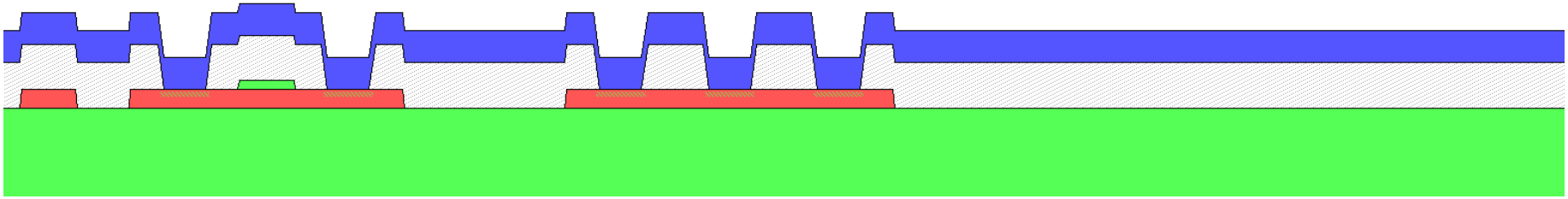




Process with two levels of metal interconnect

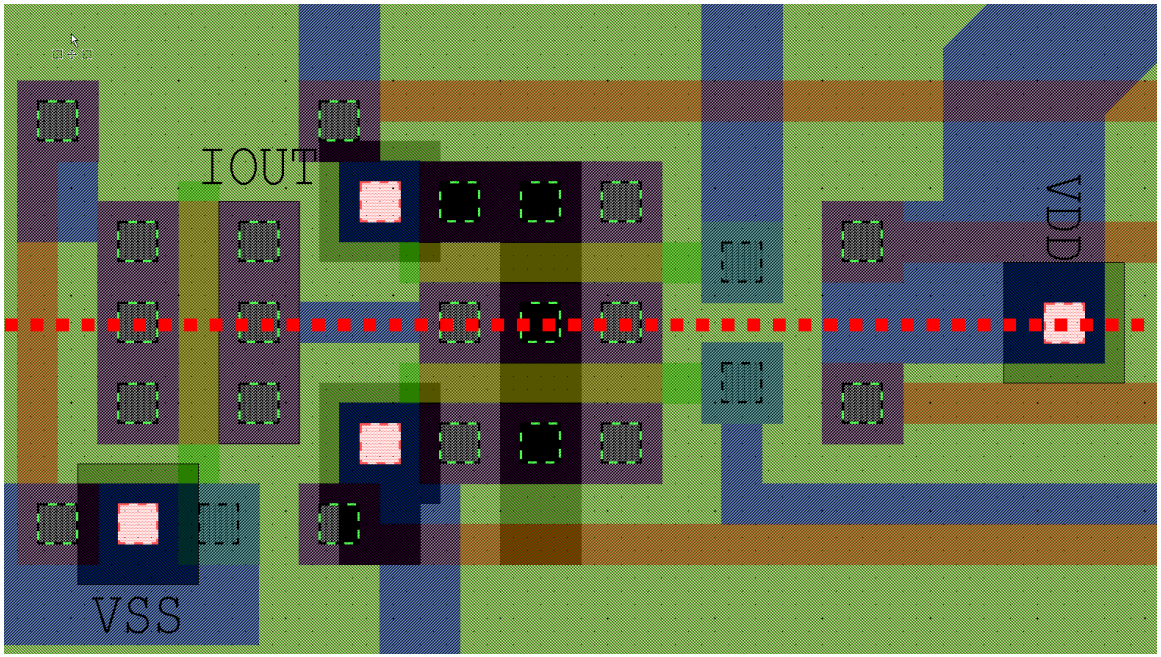
- Bake out and sputter deposition of metal 1.

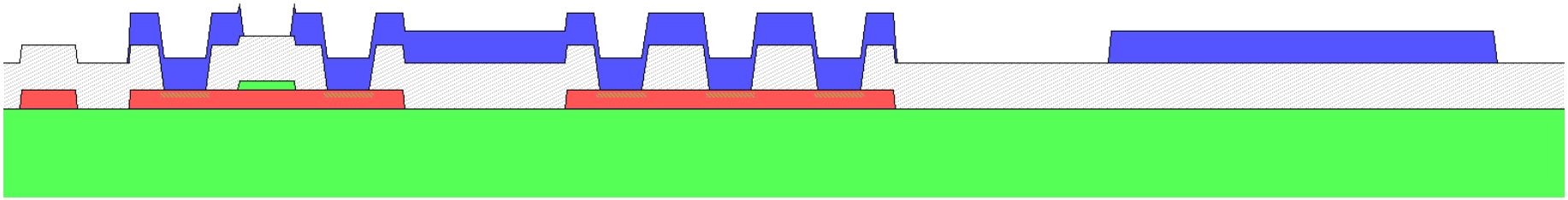




Process with two levels of metal interconnect

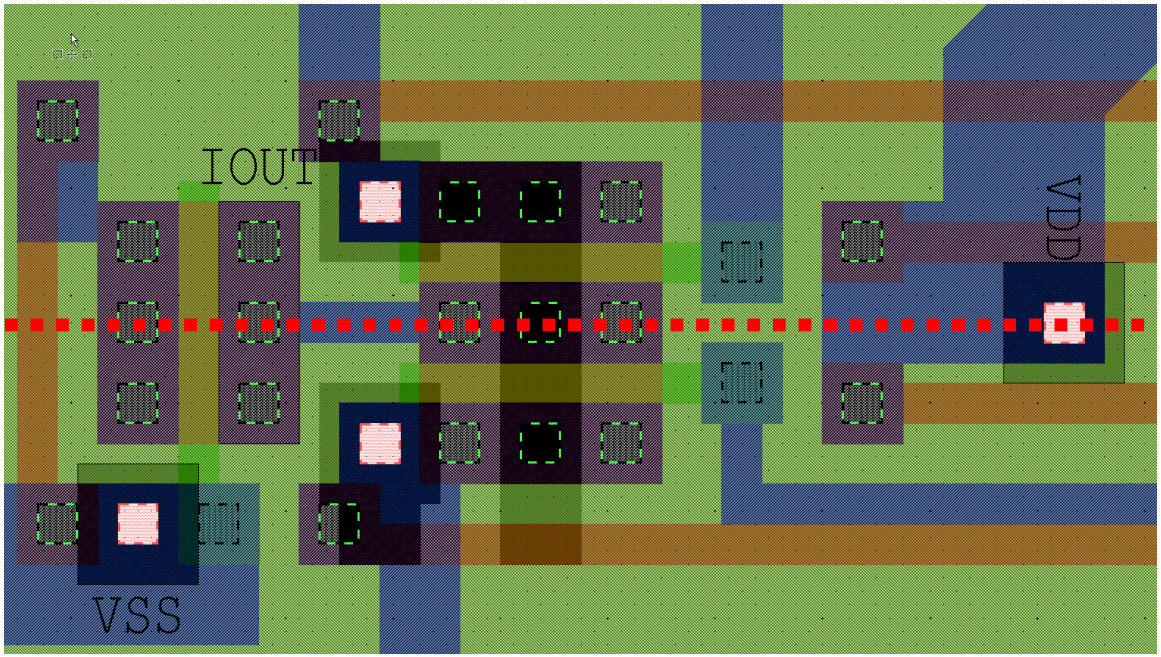
- Dry etch of metal 1.

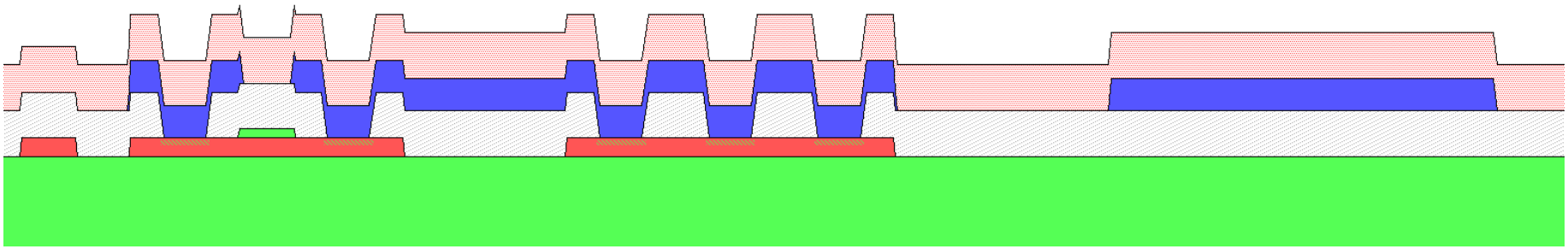




Process with two levels of metal interconnect

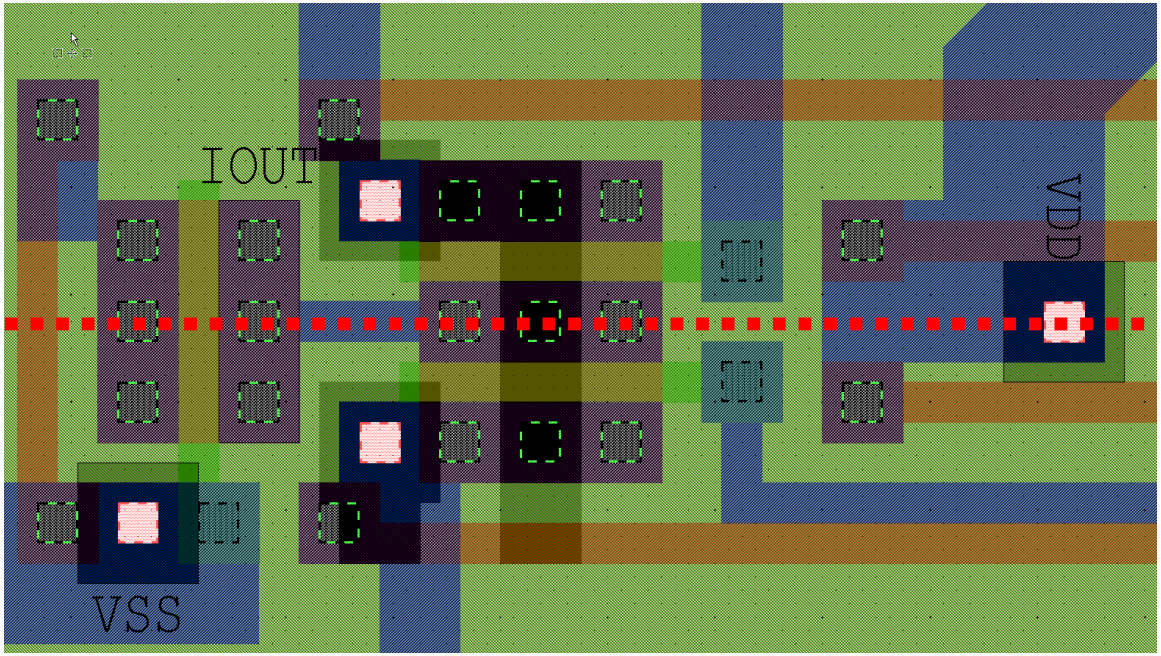
- Deposited oxide 2.

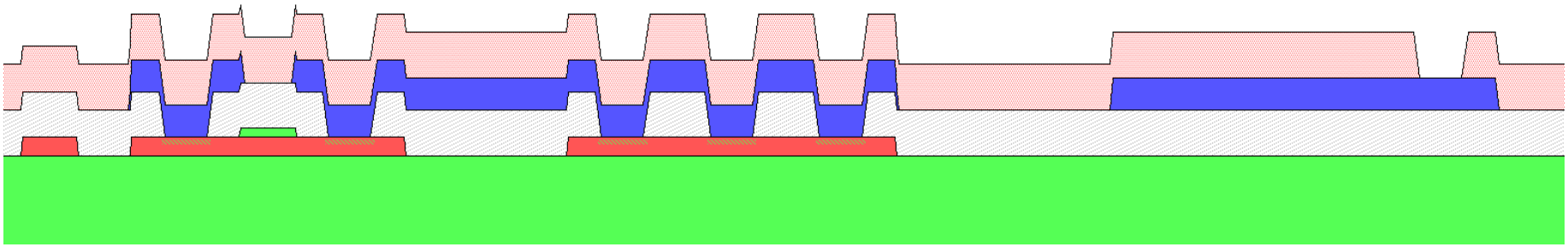




Process with two levels of metal interconnect

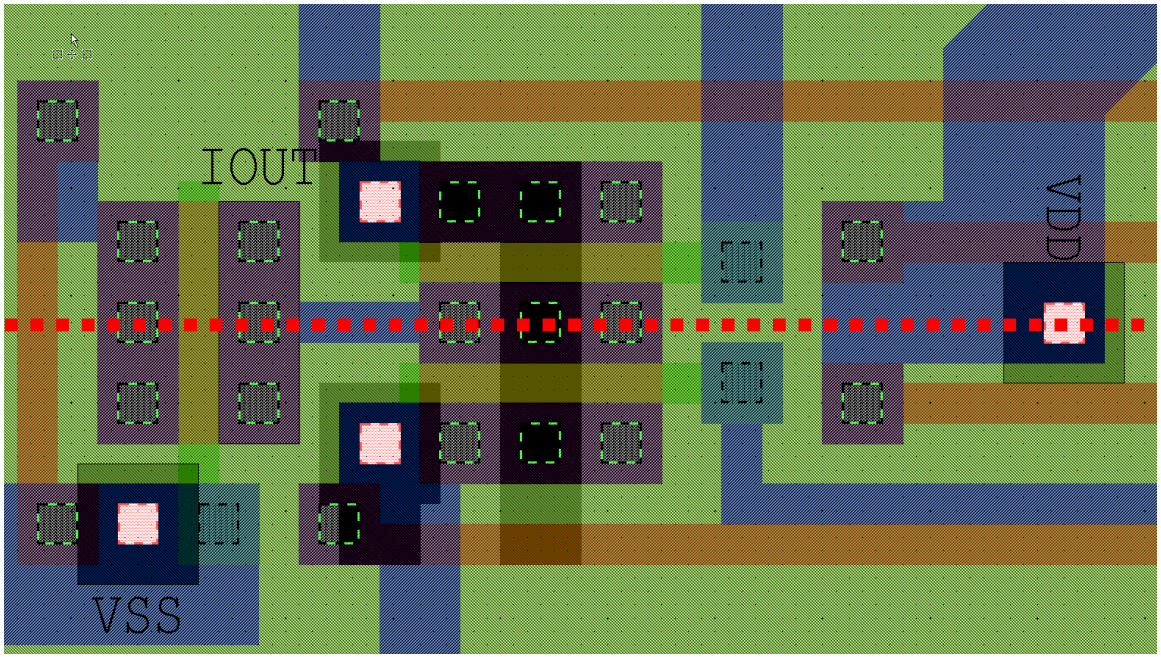
- Dry etch of via 2.

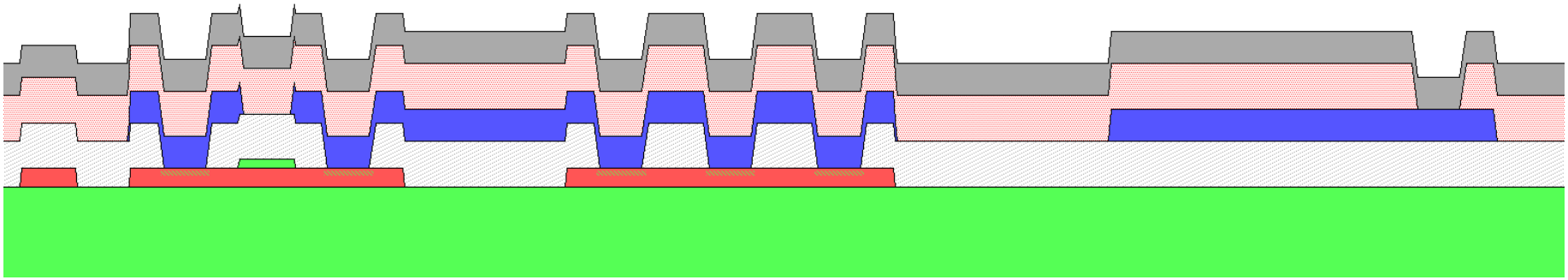




Process with two levels of metal interconnect

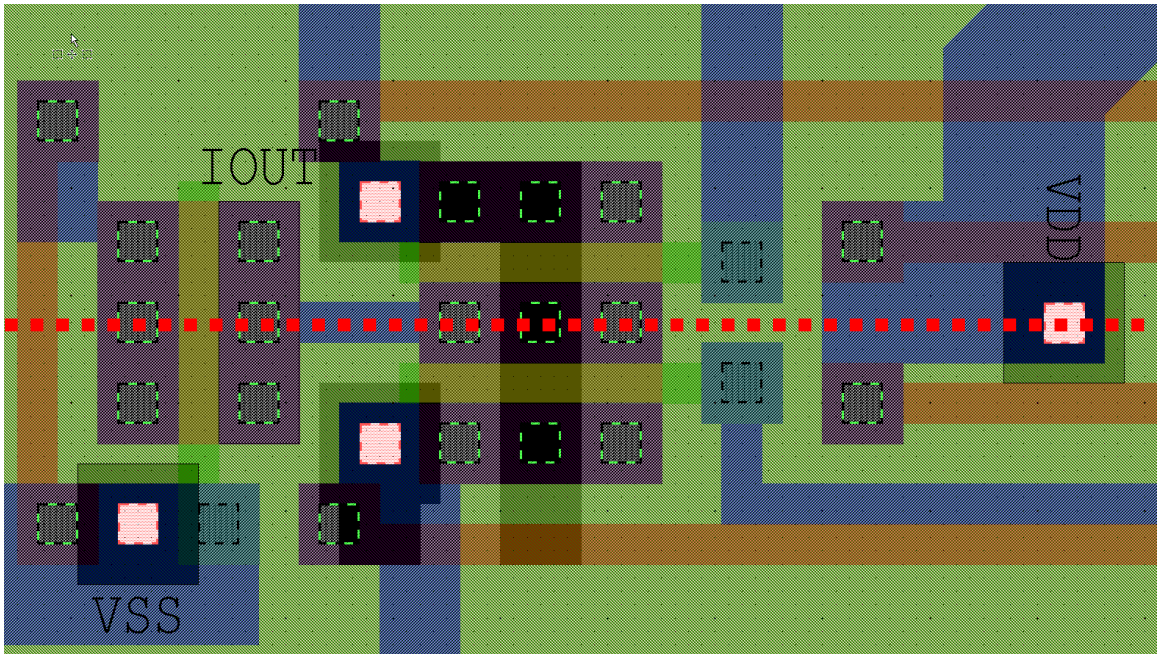
- Bake out and sputter deposit of metal 2.

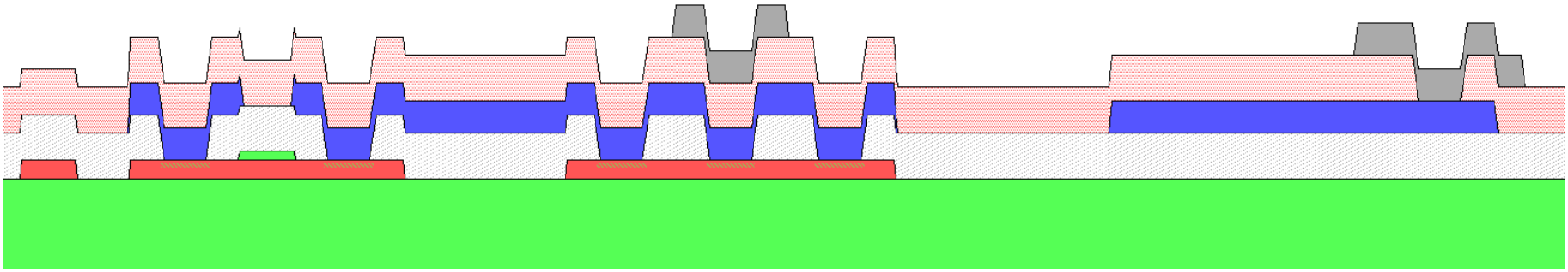




Process with two levels of metal interconnect

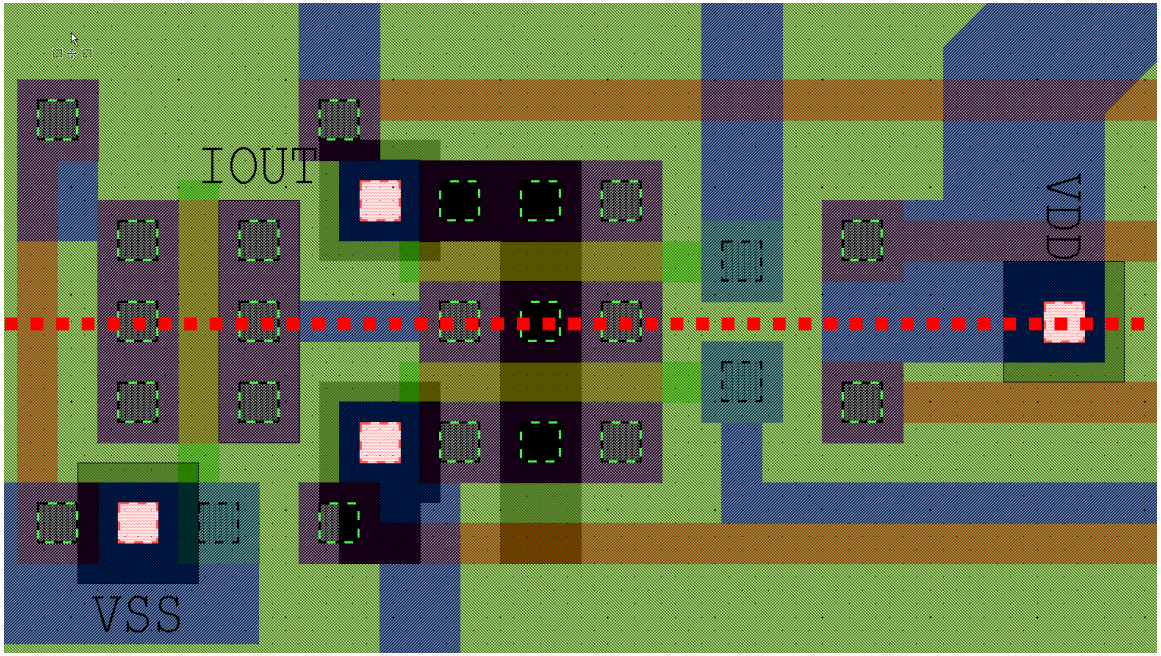
- Dry etch metal 2.

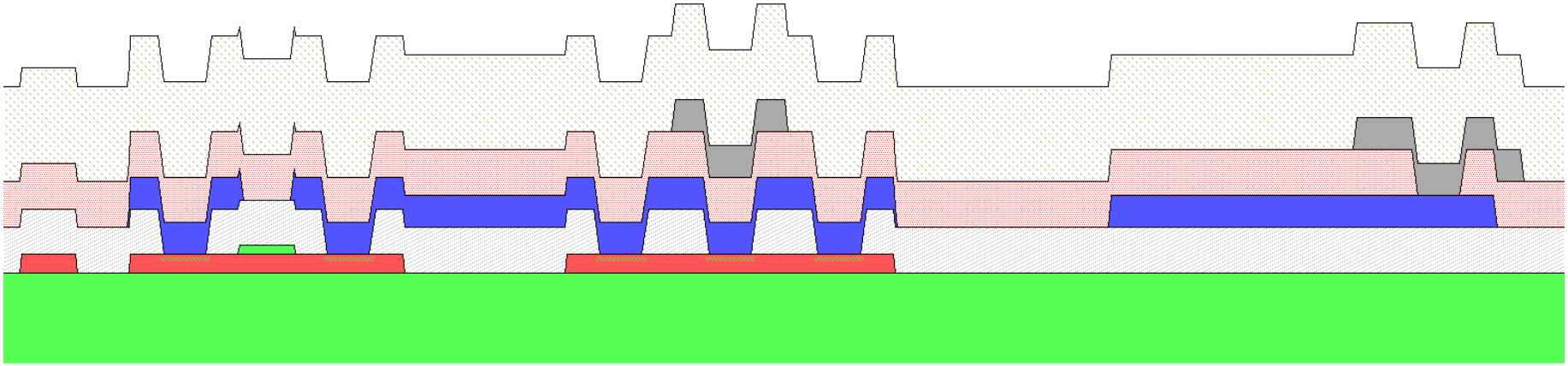




Process with two levels of metal interconnect

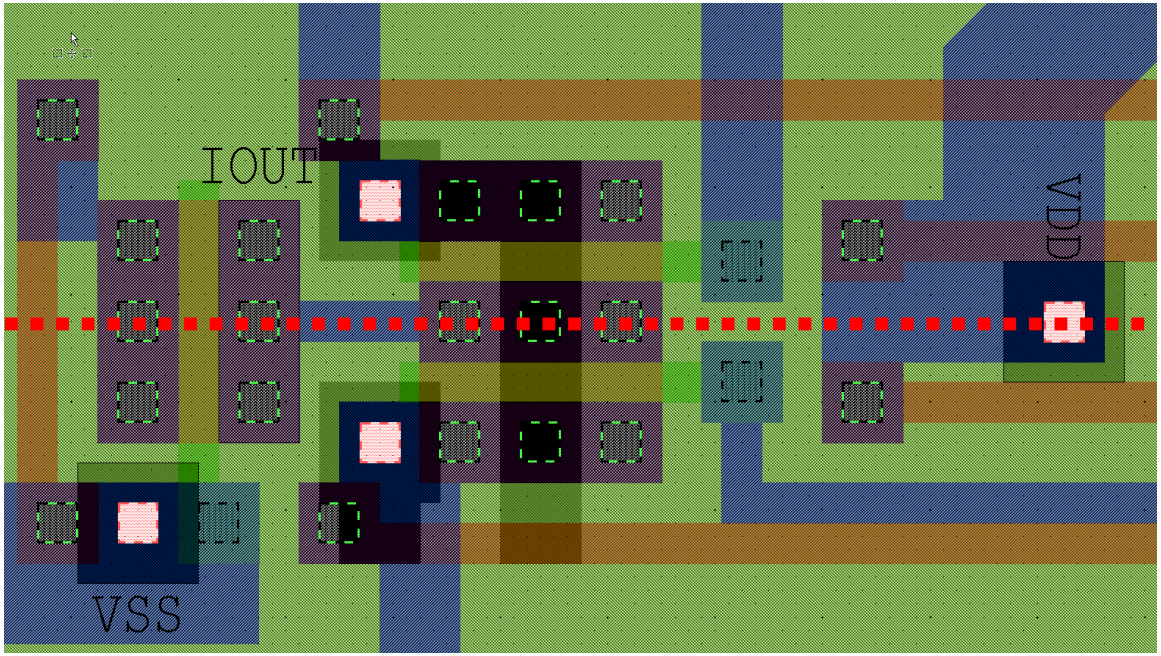
- Deposit oxide 3.
- Dry and wet etch of via 3 (not shown and only used for bond pads).

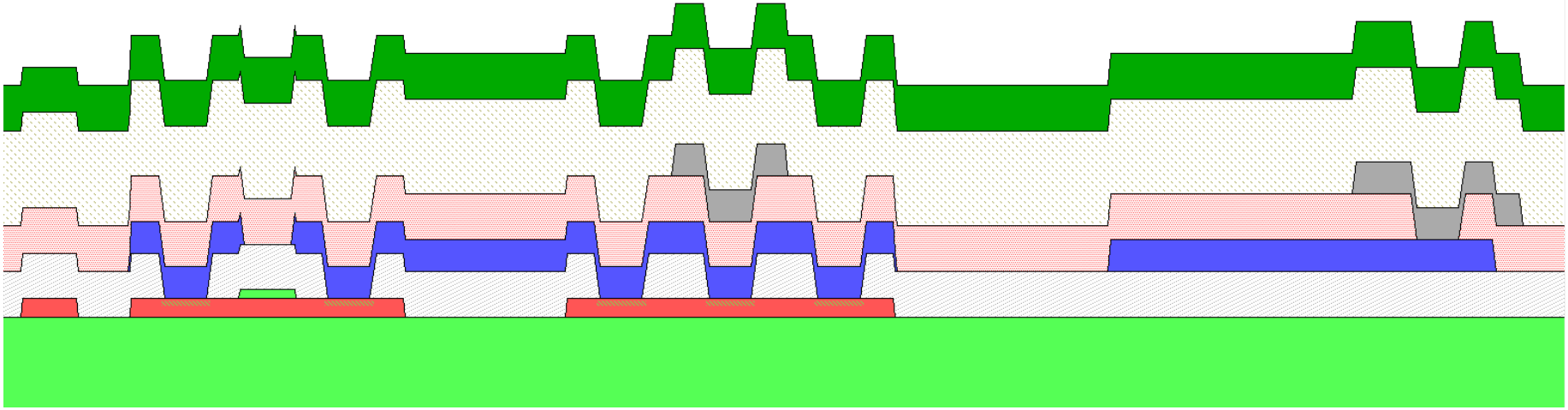




Process with two levels of metal interconnect

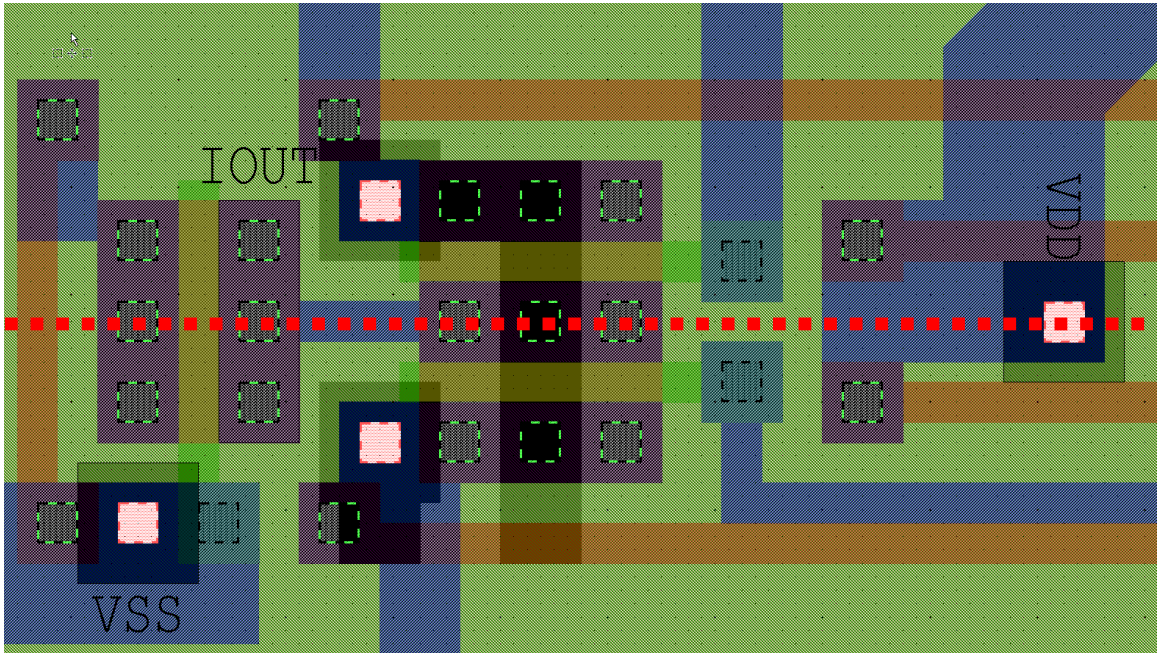
- Bake out and deposit of metal 3

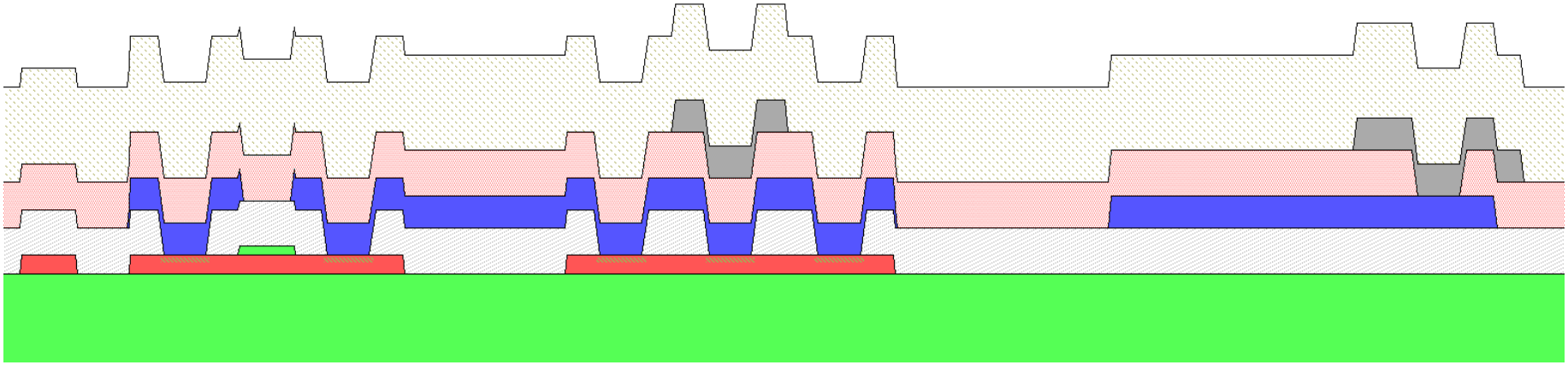


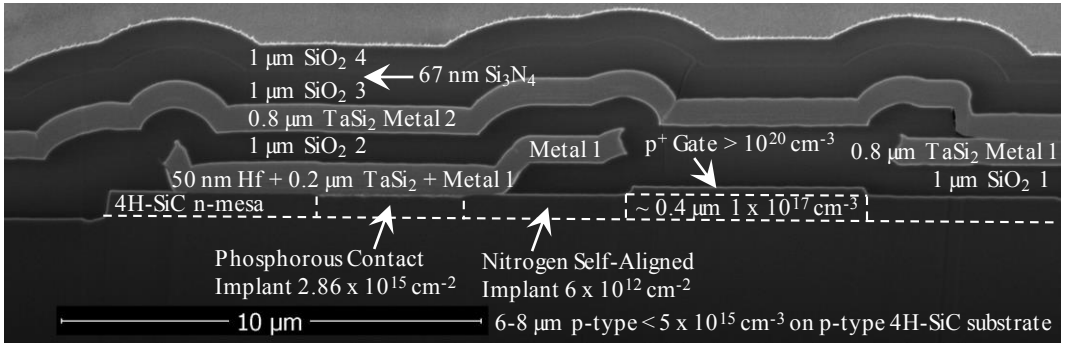


Process with two levels of metal interconnect

- Dry etch of metal 3.






1 µm SiO2 4
67 nm Si3N4
1 µm SiO2 3
0.8 µm TaSi2 Metal 2
1 µm SiO2 2
Metal 1
p+ Gate > 10^20 cm^-3
0.8 µm TaSi2 Metal 1
1 µm SiO2 1
50 nm Hf + 0.2 µm TaSi2 + Metal 1
4H-SiC n-mesa
~ 0.4 µm 1 x 10^17 cm^-3
Phosphorous Contact
Implant 2.86 x 10^15 cm^-2
Nitrogen Self-Aligned
Implant 6 x 10^12 cm^-2
10 µm
6-8 µm p-type < 5 x 10^15 cm^-3 on p-type 4H-SiC substrate