

Effects of Parasitic Reactance on Lattice Circuit Slotline Switch

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Abstract — A slotline lattice switch has recently been proposed and demonstrated. In that paper, ideal diode characteristics were assumed. In this paper, the effects of parasitic reactances, due to the diode and the wire bonds that connect it to the circuit, are investigated. The switch is compared to a traditional slotline switch with a single diode across the slot.

Index Terms — Lattice Circuit, pin diode, slotline, switch.

I. INTRODUCTION

A slotline switch based on a lattice circuit and a short circuit terminated stub has recently been published [1] and shown in Fig. 1. In that paper, ideal diode characteristics or a circuit with no parasitic reactances was assumed for the analysis. A question has been asked about effects of parasitic reactances on the switch.

This paper addresses that question by extracting the equivalent circuit model parameters of the pin diode when connected with a bond wire of approximate length equal to that used in the circuit. Then, the characteristics of the lattice switch circuit are derived with parasitic reactances included and the predicted characteristics are compared to the measured characteristics. Finally, an analysis is performed on the effects of the parasitic inductance, which is controllable by the circuit layout, on the switch characteristics, and the lattice switch is compared to the traditional switch [2], [3] with the same parasitic reactances.

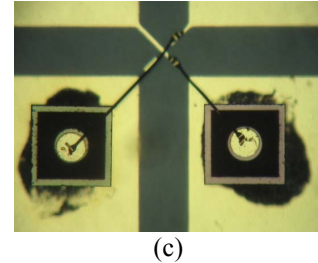
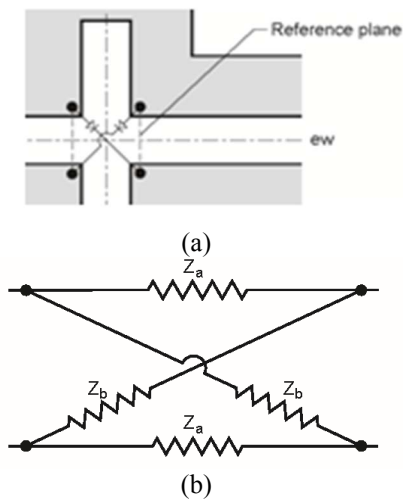


Figure 1: Schematic of (a) lattice circuit slotline switch, (b) equivalent circuit of slotline lattice circuit and (c) photograph of lattice circuit slotline switch.

II. DIODE MODEL

A simplified model of the *pin* diode is shown in Fig. 2 [4], with the additional assumption that the package capacitance is negligible. The reverse biased diode is modeled as a series connection of a resistance, R_r , inductance, L , and capacitance, C . R_r is the series combination of the wire bond resistance and the intrinsic layer resistance, and C is the junction capacitance. The forward biased diode is modeled as a series inductance, L , and resistance, R_f . The inductance is primarily due to the wire bond connecting the diode to the circuit and is therefore somewhat controllable by optimizing the circuit layout. It also means that the forward and reverse bias circuits have the same inductance. R_f includes the wire bond resistance and the intrinsic layer resistance.

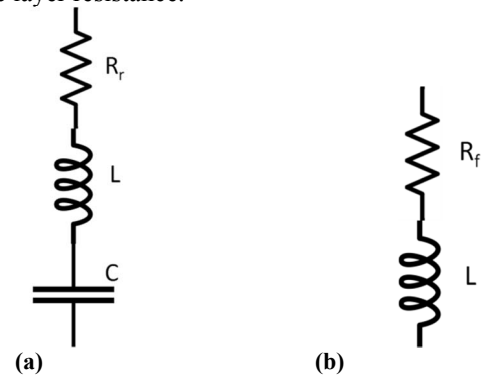


Figure 2: *pin* diode model (a) reverse bias (b) forward bias.

Using the model in Fig. 2, the impedance of the reverse and forward biased conditions of the diode can be written as:

$$Z_r = R_r + j\omega L + \frac{1}{j\omega C} = R_r + jX_r \quad (1)$$

where $X_r = -(1 - \omega^2 LC)/\omega C = -1/\omega C_{eff}$ and:

$$Z_f = R_f + j\omega L = R_f + jX_f \quad (2)$$

where $X_f = \omega L$.

III. DIODE MODEL EXTRACTION

The *pin* diode (MACOM MA4P404-132) was mounted on a 0.38 mm thick, alumina carrier for one port characterization and the length of the bond wire from the probe pad to the diode contact was made similar to that used on the slotline, lattice circuit switch (Fig. 1c). A 150 μm pitch ground-signal-ground (GSG) probe was used and an Agilent PNA was calibrated to the probe tip using a GGB Industries calibration standard. Measurements were made at the same bias conditions as used for the lattice circuit switches ($V_i=0$ V, $I_i=0$ mA, and $V_r=1.07$ V, $I_r=37$ mA) over the frequency range of 0.01 to 20 GHz. S-parameters were converted to Z-parameters and fit to (1) and (2). The extracted diode parameters are shown in Table 1.

Table 1: Extracted *pin* diode equivalent circuit parameters.

	R_r (Ω)	L (nH)	R_i (Ω)	C (pF)
Reverse Bias	-----	0.78	7.0	0.24
Forward Bias	1.3	0.78	-----	-----

IV. LATTICE CIRCUIT SWITCH

The lattice circuit switch is shown in Fig. 1. In [1] the S-parameters of the circuit are given as:

$$S_{11} = \frac{Z_a Z_b - Z_o^2}{Z_a Z_b + Z_o(Z_a + Z_b) + Z_o^2} \quad (3a)$$

$$S_{21} = \frac{(Z_b - Z_a)Z_o}{Z_a Z_b + Z_o(Z_a + Z_b) + Z_o^2} \quad (3b)$$

where Z_a is the impedance of the short circuit stub and Z_b is the impedance of the reverse or forward biased diode (Z_r and Z_i , respectively). Thus,

$$Z_a = jZ_o \tan(\theta) \quad (4a)$$

$$Z_b = R_i + jX_i \quad (i = f \text{ or } r) \quad (4b)$$

$\theta = \beta l$ for the slotline stub, β is the propagation constant and l is the length of the stub. Inserting (4) in (3) gives:

$$S_{11} = \frac{-(X_i \tan(\theta) + Z_o) + jR_i \tan(\theta)}{[(R_i + Z_o) - X_i \tan(\theta)] + j[(R_i + Z_o) \tan(\theta) + X_i]} \quad (5a)$$

$$S_{21} = \frac{R_i + j(X_i - Z_o \tan(\theta))}{[(R_i + Z_o) - X_i \tan(\theta)] + j[(R_i + Z_o) \tan(\theta) + X_i]} \quad (5b)$$

In most cases, R_r and R_i are small and have a small influence on S_{11} and S_{21} and they may be neglected to help derive a better understanding of the switch characteristics. Using $R_i=0$,

$$S_{11} = \frac{-(X_i \tan(\theta) + Z_o)}{[Z_o - X_i \tan(\theta)] + j[Z_o \tan(\theta) + X_i]} \quad (6a)$$

$$S_{21} = \frac{j(X_i - Z_o \tan(\theta))}{[Z_o - X_i \tan(\theta)] + j[Z_o \tan(\theta) + X_i]} \quad (6b)$$

From (6), it is observed that:

- (a) $S_{21}=0$ if $X_i=Z_o \tan(\theta)$, which is the condition of a matched Wheatstone bridge.
- (b) $|S_{21}|=1$ and $S_{11}=0$ if $X_i/Z_o = -\cot(\theta)$.

To visualize the effect of the parasitic reactances of the diode and wire bonds on the lattice switch described in [1] (slot width = 0.3 mm, strip width = 4.8 mm, stub length = 11.430 mm on an alumina substrate of 0.38 mm thickness), Fig. 3 shows the conditions for $S_{21}^{OFF} = 0$. From [1], $S_{21}^{OFF} = 0$ when the diodes are reverse biased, or $X_r/Z_o = \tan(\theta)$. If L and $C=0$, $S_{21}^{OFF} = 0$ when $\beta l = \pi/2$ or approximately at 3.786 GHz. If $L=0$ and $C=0.24$ pF, which is the capacitance of the *pin* diode, $S_{21}^{OFF} = 0$ at 4.6 GHz. If $L=0.78$ nH and $C=0.24$ pF, which are the measured reactances in Table 1, $S_{21}^{OFF} = 0$ at 4.79 GHz. Thus, the frequency at which $S_{21}^{OFF} = 0$ when the diodes are reverse biased, or the frequency of maximum isolation when the switch is OFF, increases due to the parasitic reactances. It is interesting to study the effect of the inductance on the frequency of maximum isolation since the capacitance is an inherent property of the diode whereas L is dependent on the length of the wire bond and thus controllable. This is also shown in Fig. 3, where it is seen that the frequency for $S_{21}^{OFF} = 0$ increases as L increases until $L \approx 2$ nH, at which $X_r/Z_o \neq \tan(\theta)$ if X_r is negative, or capacitive. Thus, for reasonable length bond wires, there is always a frequency at which isolation is infinite when the switch is off (remember that $R_r=0$ is assumed).

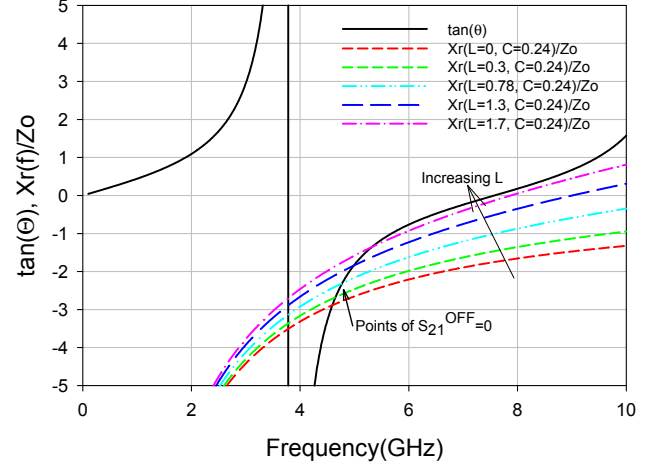


Figure 3: Condition at which isolation is maximum when the switch is OFF. Increasing L with $C=0.24$ pF.

When the switch is ON, the diodes are forward biased [1] and $|S_{21}^{ON}| = 1$ if $X_f/Z_o = \omega L/Z_o = -\cot(\theta)$. If $X_r=0$, or $L=0$, $|S_{21}^{ON}| = 1$ at $\beta l = \pi/2$. To visualize the effect of L on the frequency at which $|S_{21}^{ON}| = 1$, Fig. 4 shows the required condition. Note that there is always a condition at which $|S_{21}^{ON}| = 1$, although the frequency for zero ON state insertion loss increases as L increases.

Figure 5 shows the predicted characteristics for the ideal switch with $R_r + jX_r = 0$ when the diode is forward biased and

$R_f + jX_f = 0 + j\infty$ when the diode is reverse biased, or the ideal cases of $Z_b = 0$ and ∞ discussed in [1]. In addition, Fig. 5 shows the predicted slotline lattice switch characteristics with the extracted resistances and reactances shown in Table 1. Finally, the measured lattice slotline switch characteristics [1] are shown in Fig. 6. It is seen that the predicted and measured characteristics of the OFF state switch agree well except for measurement errors caused by the excitation of higher order modes by the T-junction and the GS probes. The ON state characteristics do not agree as well, which is probably caused by an over estimation of the wire bond inductance.

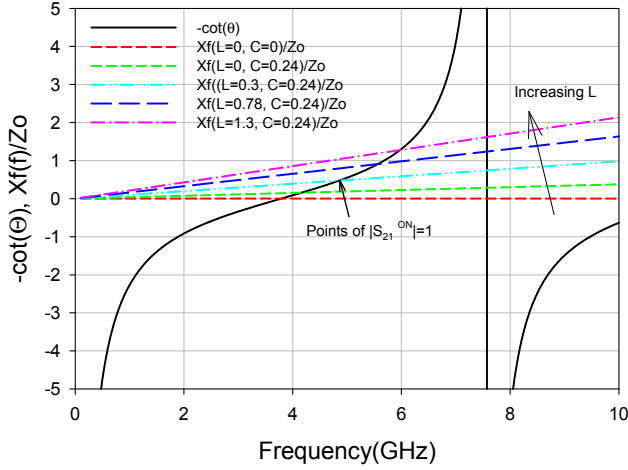


Figure 4: Condition at which zero insertion loss is achieved when the switch is ON.

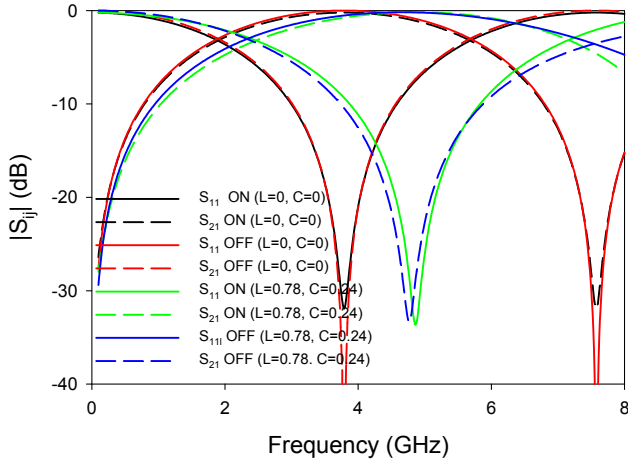


Figure 5: Predicted S-parameters of slotline lattice switch for the no parasitic reactances and extracted diode reactances.

It is interesting to examine if a switch with perfect ON and OFF state characteristics can be achieved at the design frequency even if the circuit contains parasitic reactances. The required conditions, which were stated in Section IV, are

$$\tan(\theta) = \frac{\omega^2 LC - 1}{\omega CZ_o} \quad (7a)$$

$$\cot(\theta) = \frac{-\omega L}{Z_o} \quad (7b)$$

From (7a) and (7b), we may derive:

$$L = \frac{1 \pm \sqrt{1 - 4\omega^2 C^2 Z_o^2}}{2\omega^2 C} \quad (8a)$$

and

$$\theta = \tan^{-1}(-Z_o/\omega L) \quad (8b)$$

This implies, after some algebra, that if $2\omega CZ_o < 1$ and $\pi/2 < \theta < 3\pi/4$ a value of L may be found to obtain ideal switch conditions. For diodes with small capacitance, these conditions can be met through the lower GHz range.

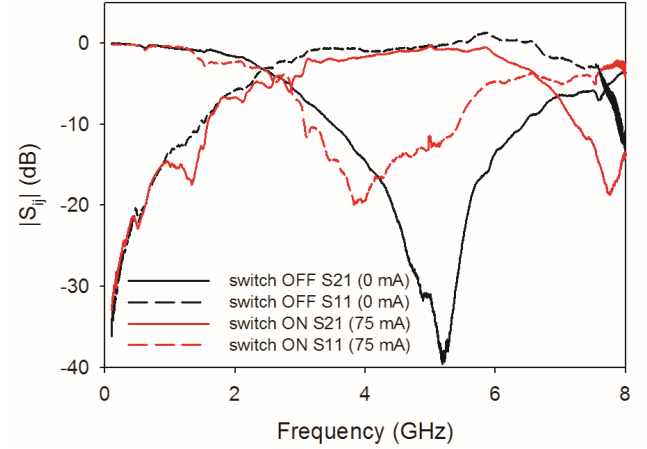


Figure 6: Measured S-parameters of slotline lattice switch.

V. COMPARISON WITH “TRADITIONAL” SLOTLINE SWITCH

The traditional slotline switch is comprised of a single diode across the slot [2], [3]. If the diode is forward biased, the low diode impedance appears as a short circuit across the slot and all of the power is reflected. If the diode is reverse biased, the high diode impedance does not interfere with the RF power propagation. The S-parameters may be derived as:

$$S_{11} = \frac{-Z_o}{(2R_i + Z_o) + j2X_i} \quad (9a)$$

$$S_{21} = \frac{2(R_i + jX_i)}{(2R_i + Z_o) + j2X_i} \quad (9b)$$

Note that $S_{21}^{OFF} = 0$ only if $R_i = X_i = 0$. Fig. 7 shows the predicted traditional switch characteristics using an ideal diode, a diode with the parasitic reactances in Table 1, and a diode with a parasitic inductance of 0.55 nH, which represents the inductance resulting from a wire bond length reduced by $1/\sqrt{2}$ since the bond wire should be shorter since it only needs to cross the slot and not the junction. It is seen that a zero insertion loss, infinite isolation switch is possible across the entire bandwidth if the diode is ideal, but the characteristics degrade if parasitic reactances are included.

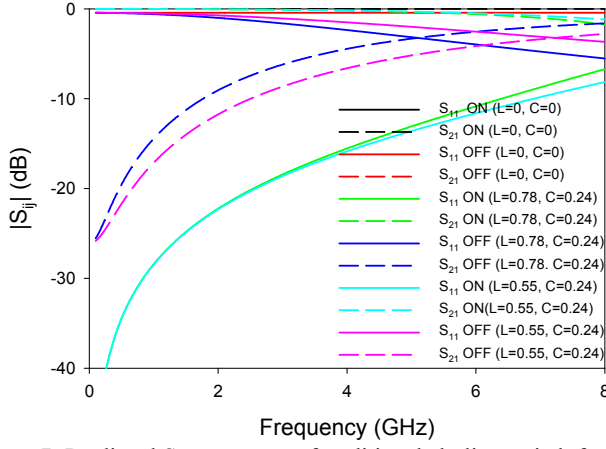


Figure 7: Predicted S-parameters of traditional slotline switch for the no parasitic reactances, extracted diode reactances, and reduced parasitic inductance ($S_{11}^{ON}=S_{21}^{OFF}=0$ for the ideal switch).

VI. CONCLUSIONS

It has been shown that the lattice switch, if assuming zero parasitic resistance, still has a frequency of infinite isolation and zero insertion loss if there are parasitic reactances. However,

the frequency at which they occur shifts to higher frequency and the ideal insertion loss and isolation frequencies may not occur at the same frequency. The lattice switch may achieve good characteristics at any frequency because it is a tuned circuit, by the quarter wavelength stub, whereas the reactances degrade the “traditional” slotline switch characteristics at higher frequency. Lastly, it is possible to choose l , L , and C so minimum insertion loss and maximum isolation occur at the same frequency.

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