"An Evaluation of Flash Cells Used in Critical Applications"

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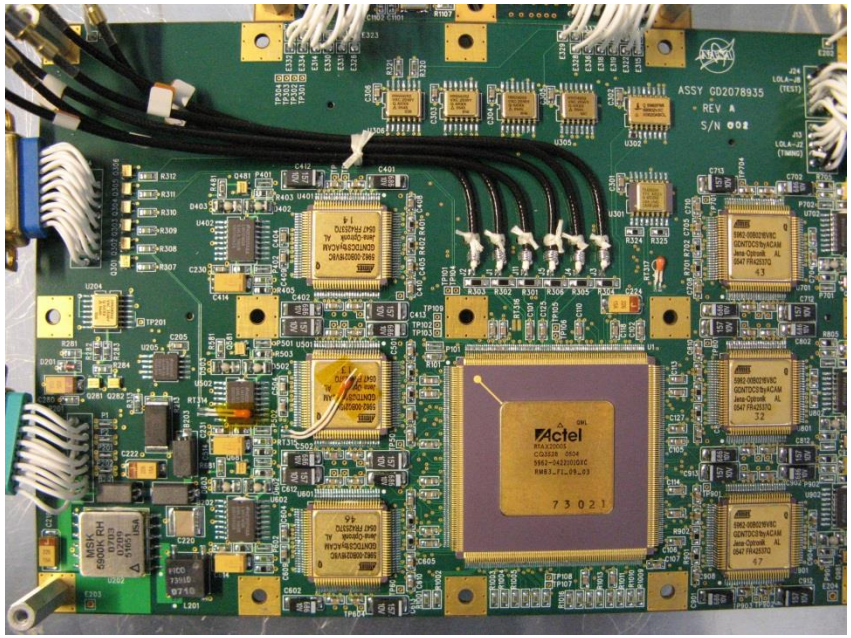

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Introduction and Agenda

- **Collaborative Effort Between NASA and DoD/DMEA**
- **Test Methods and Protocols**
- **Key Parameter: Threshold Voltage (V_T)**
- **DUT: Microsemi (Actel) A3P250L FPGA**
  - Common Technology Between spaceflight electronics and DoD fuze control circuitry.
- **Long-Term "Engineering Run" at +25 °C and +150 °C (6 DUTS)**
- **Threshold Voltage Distribution: Large Population (~1,000 DUTS)**
  - Part-to-Part Variability
  - Outliers
- **Results: Environmental Tests**
  - Temperature (+25 °C, +125 °C, and +150 °C)
  - Electromagnetic (EM) Susceptibility
  - Neutron Irradiation Susceptibility
  - Electrostatic Discharge (ESD) Susceptibility
- **Future Testing (in-process and planned; this is a work in progress)**
- **Additional Material and Data in the On-line Version of This Talk**

Threshold Voltage (V_T)

Microsemi A3PL FPGA Flash Cell

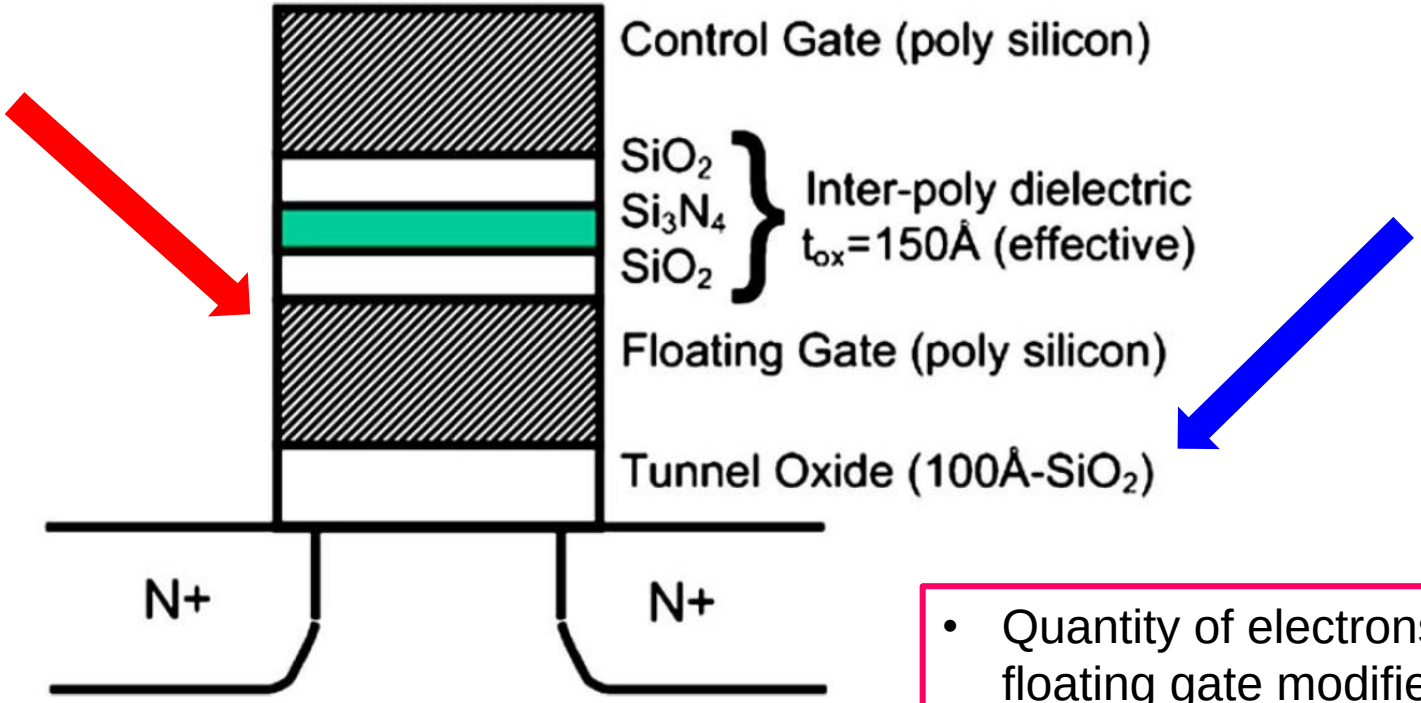


Figure courtesy of Microsemi Corp.

- Quantity of electrons stored on floating gate modifies the threshold voltage (V_T).
- Threshold voltage is the “turn on” voltage for the transistor.

Stress Induced Leakage Current (SILC)

Electrons can tunnel at low bias if Traps line up at a spacing of 3 nm or less

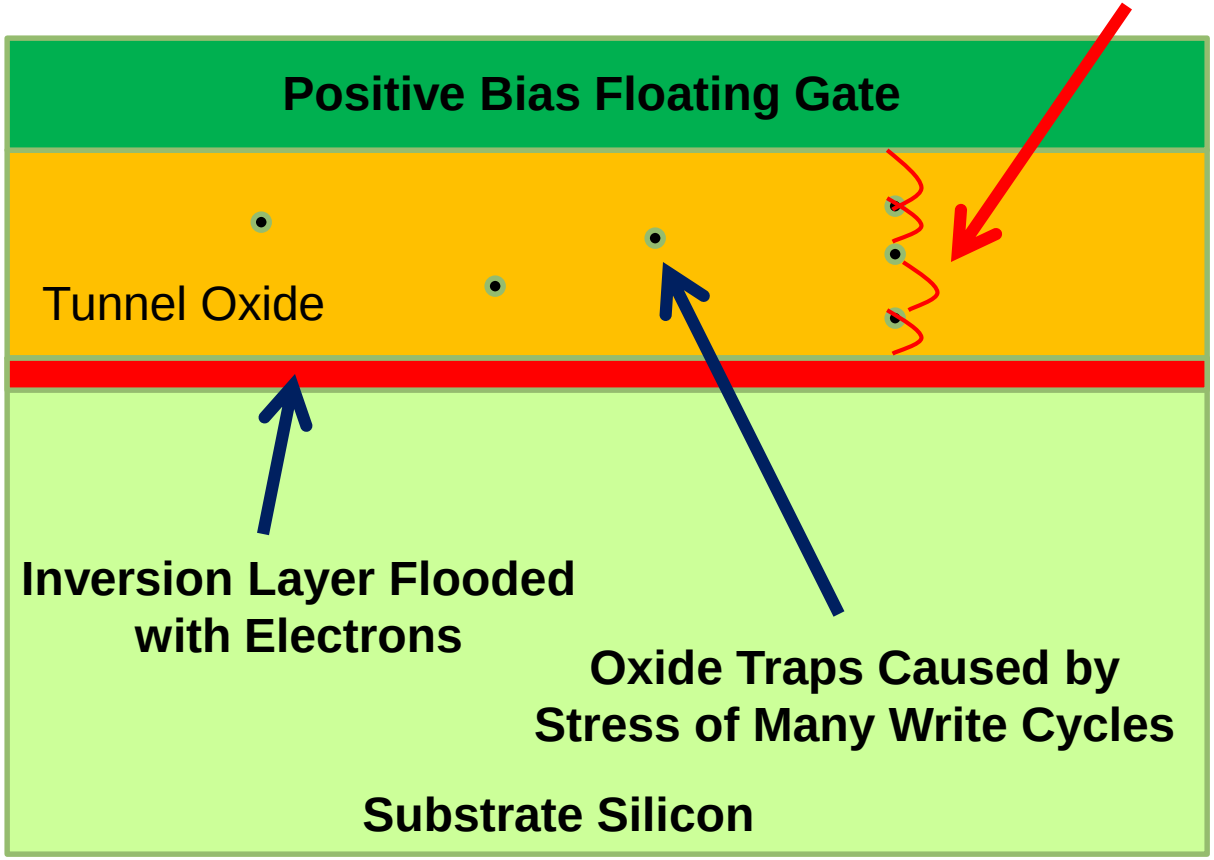
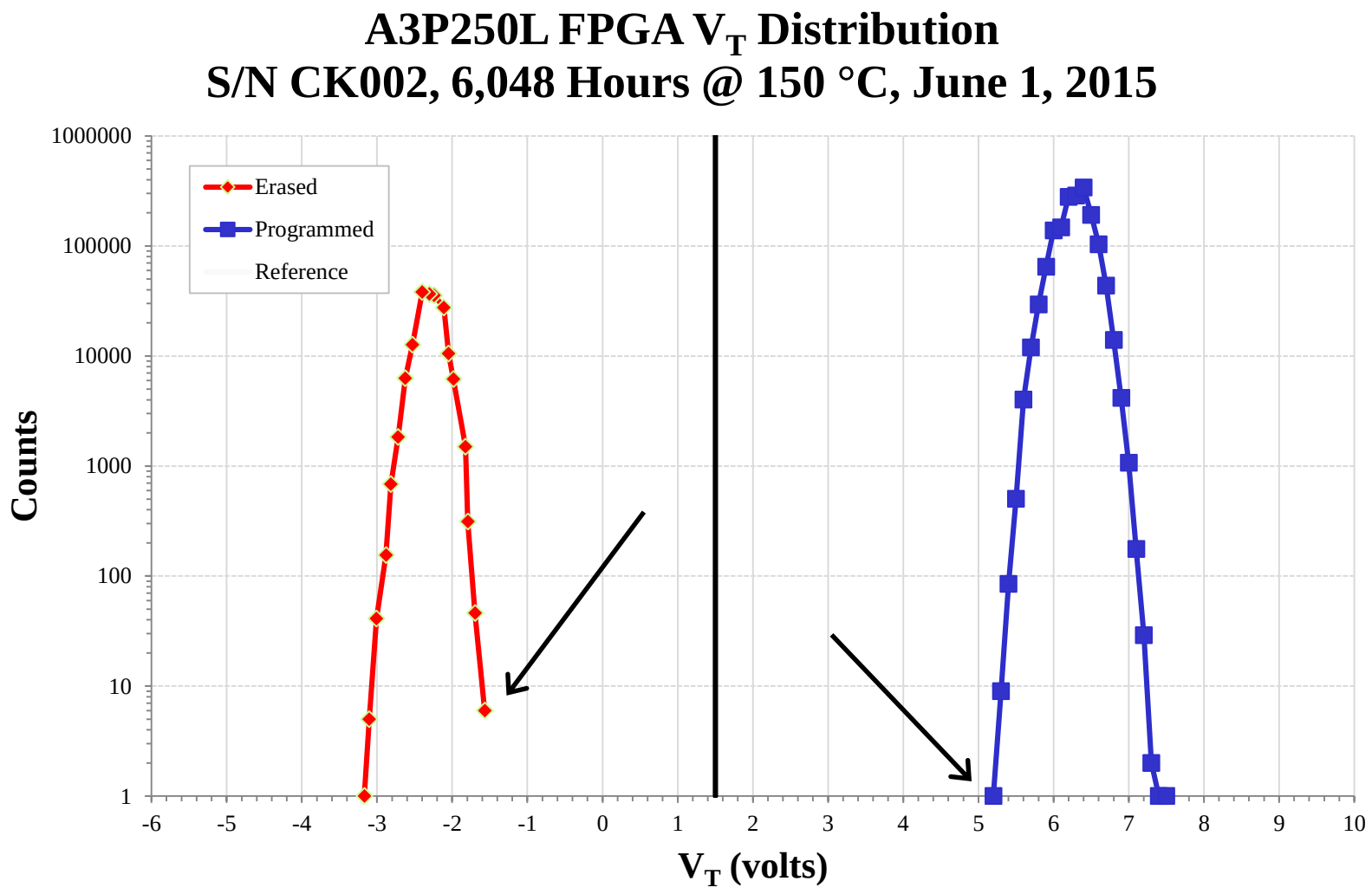


Chart courtesy of Microsemi Corp.

Sample V_T Distribution in an FPGA



Experiment Goals

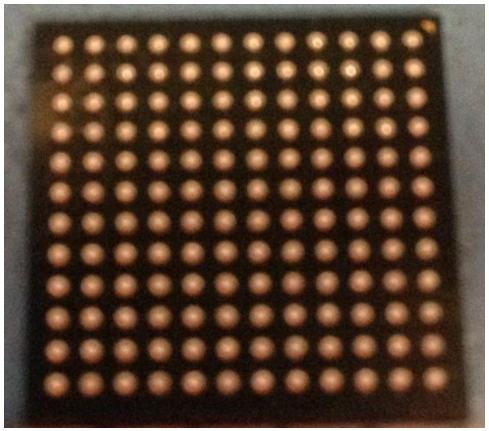
- **The primary objective is to determine the probability of extrinsic flash cells in the population and to determine how that will limit the device's lifetime.**

- **A secondary objective is to track the intrinsic populations lifetime which is a function of storage temperature.**

- **A third objective is to measure the flash cells' susceptibility to other environmental stresses.**
  - Electromagnetic (EM) radiation
  - Neutron irradiation
  - Electrostatic Discharge (ESD)
  - Heavy Ion Irradiation (total dose tests have been conducted)
  - Other (please suggest)

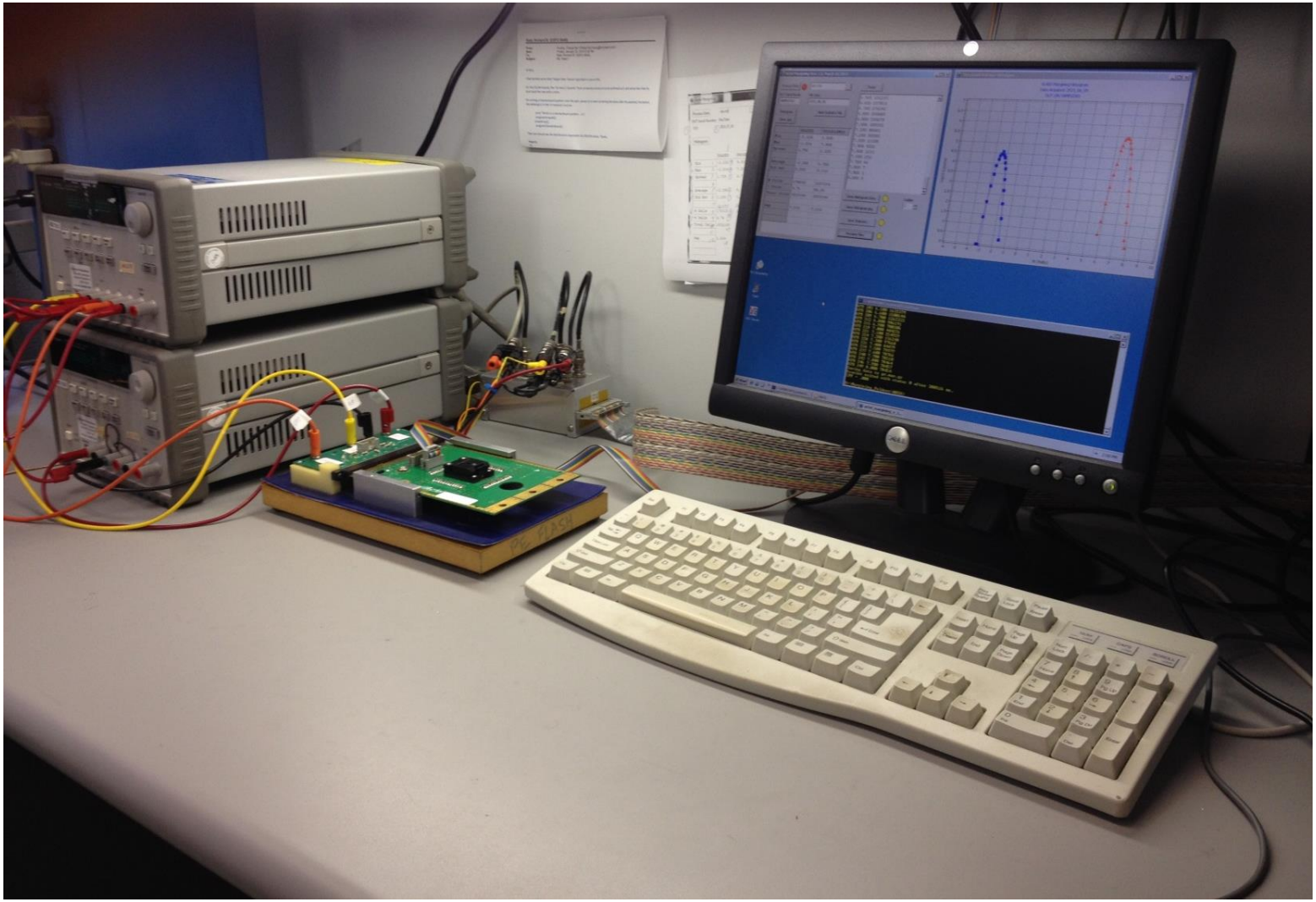
Description of DUTs

- **Microsemi (Actel) A3P250L FPGA**
  - Relatively small FPGA
  - PBGA (Plastic Ball Grid Array) Package (FG144)
  - Single Foundry for all DUTs
  - Most parts from one wafer lot (QLWY8)
    - Small number of DUTs from a second wafer lot (QLG10)



- **9 Logic Designs Used**
  - No artificial test structures
  - Logic blocks designed by different authors and styles (including macro generators)
- **10 Erase-Program-Verify Cycles for Each Device**
  - Realistic stress for our applications.
  - Manufacturer’s rating: 500 cycles
- **Complements and Extends work by Sandia National Labs**
  - Sandia is a Department of Energy organization that has previously investigated flash cell reliability. See references at the end of this presentation.

Test Station for A3P250L FPGA

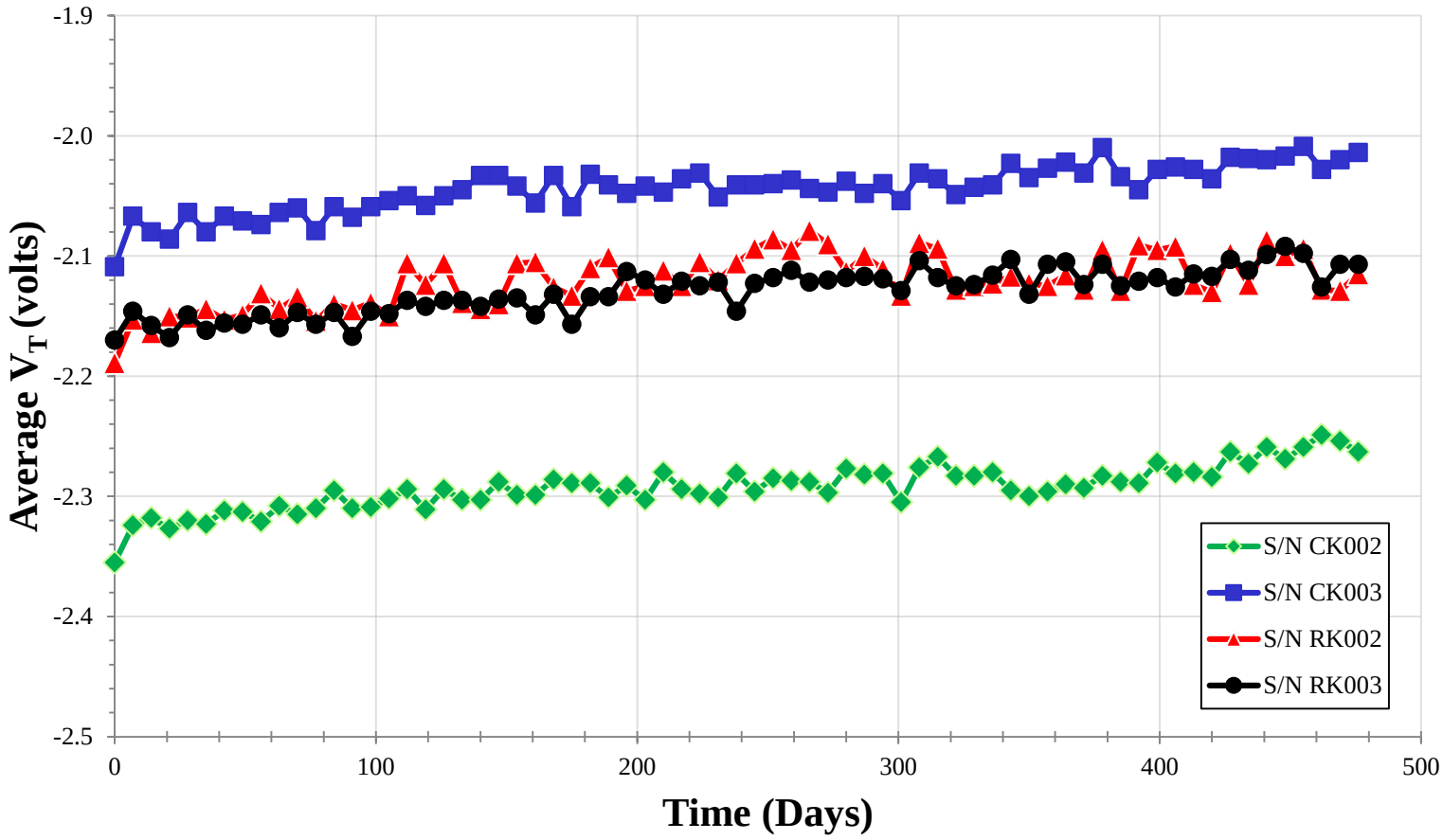


Long-Term “Engineering Run”

- **Goals**
  - Develop and refine test methods, procedures, and analysis tools and techniques
  - “Look ahead” at device response and behavior of intrinsic population
- **DUTS: 6 A3P250L FPGAs (3 each from two lots)**
  - 4 DUTs baked at 150 °C
  - 2 DUTs kept at room temperature (control samples)
- **11,592 hours (~1.3 years) at 150 °C**

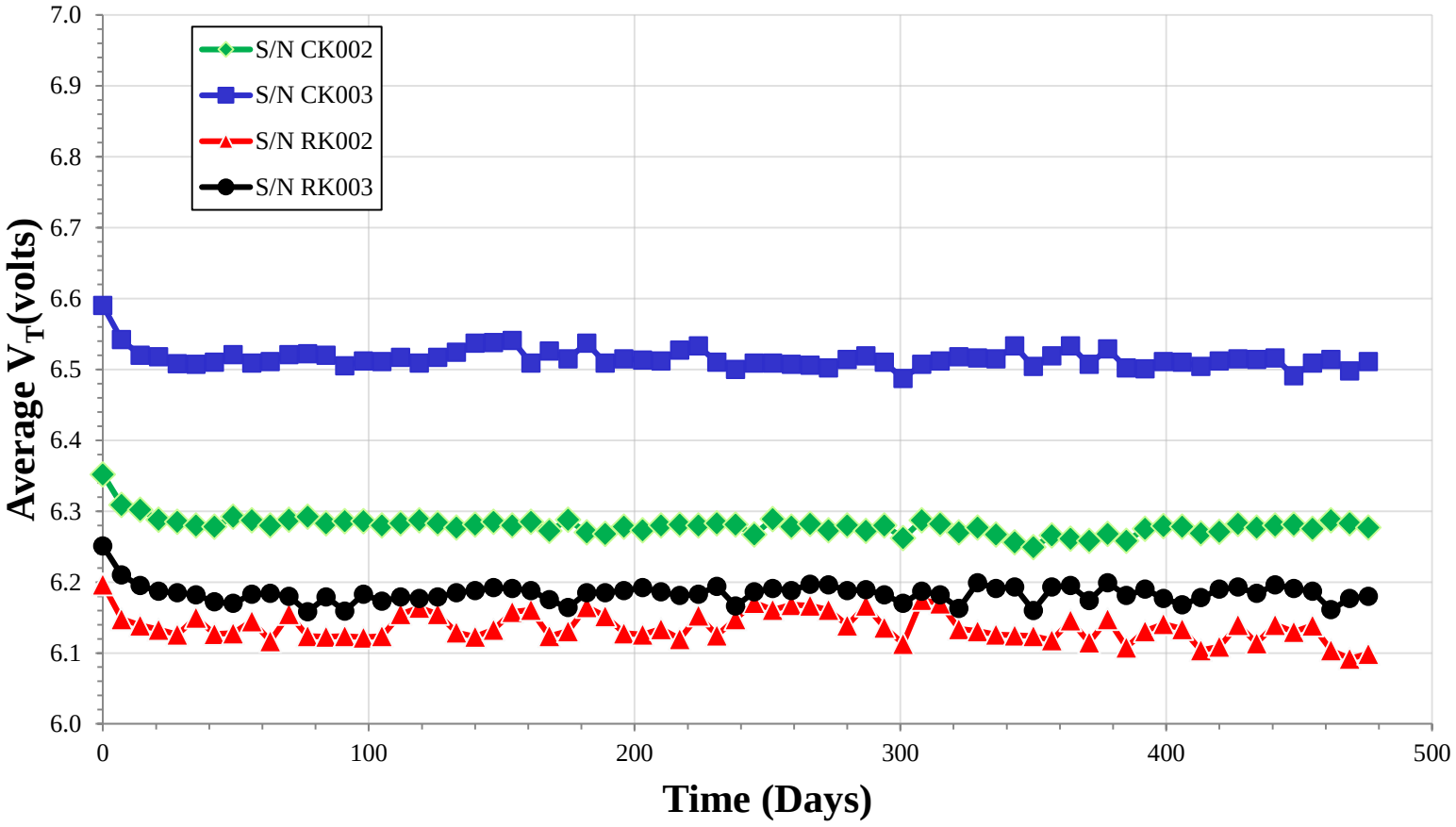
Erased: Engineering Run

A3P250L FPGA Average Erased V_T
11,424 Hours @ 150 °C, March 26, 2016



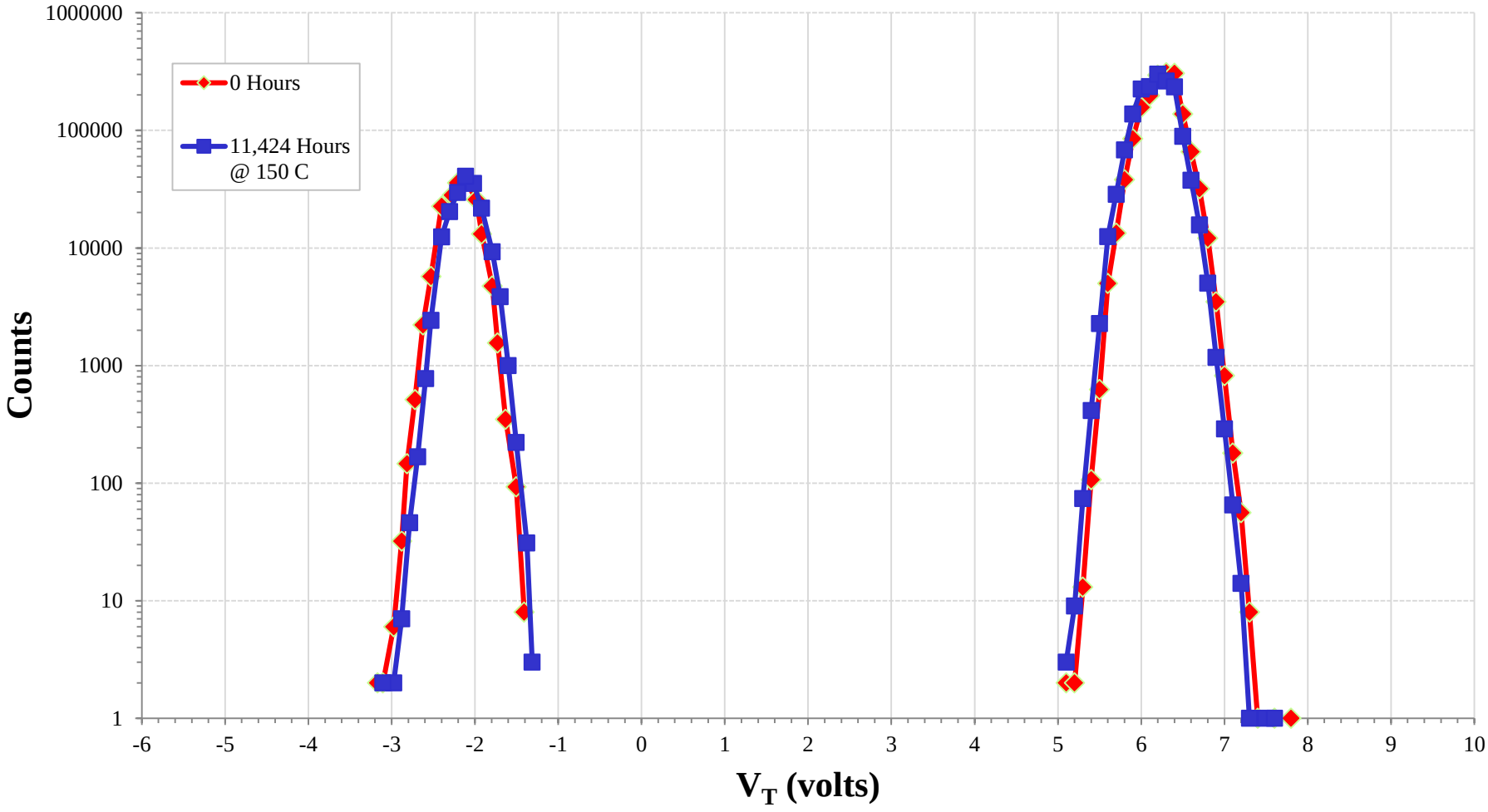
Programmed: Engineering Run

A3P250L FPGA Average Programmed V_T
11,424 Hours @ 150 °C, March 26, 2016



Effects of 150 °C Bake on Flash-based FPGA

V_T Delta After 11,424 Hours @ 150 °C: S/N RK003



Erased Cell Data Retention at 150 °C Performance vs. Specification

Tj (°C)	Spec Life (years)	6,000 Hour Data Life (years)
70	102.7	306.8
85	43.8	131.1
100	20.0	60.0
105	15.6	46.9
110	12.3	36.9
115	9.7	29.2
120	7.7	23.2
125	6.2	18.6
130	5.0	15.0
135	4.0	12.1
140	3.3	9.8
145	2.7	8.0
150	2.2	6.6

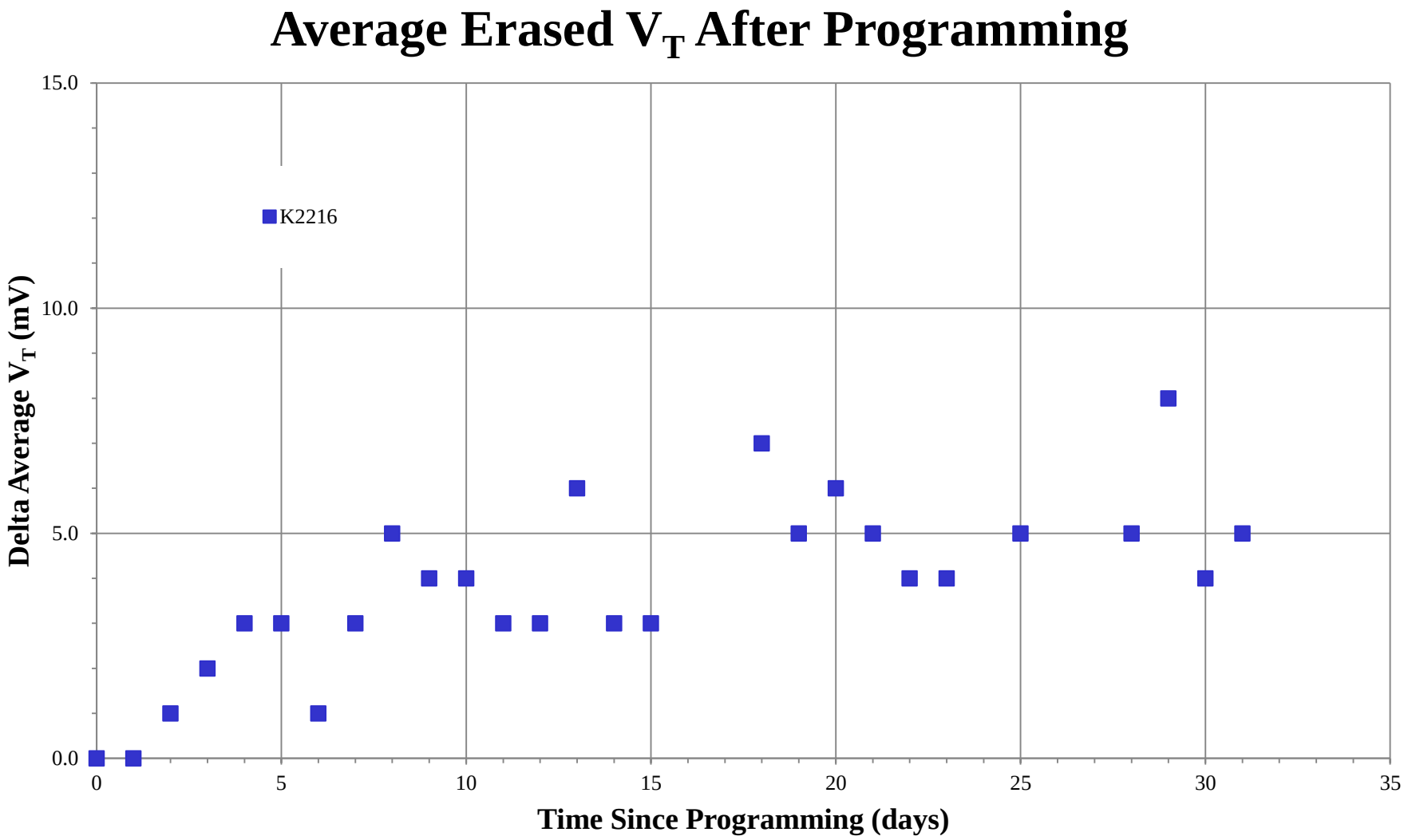
Specification Data From RT and Military ProASIC3 Data Sheets.

6,000 Hour Data derived predictions courtesy of Microsemi Corporation.

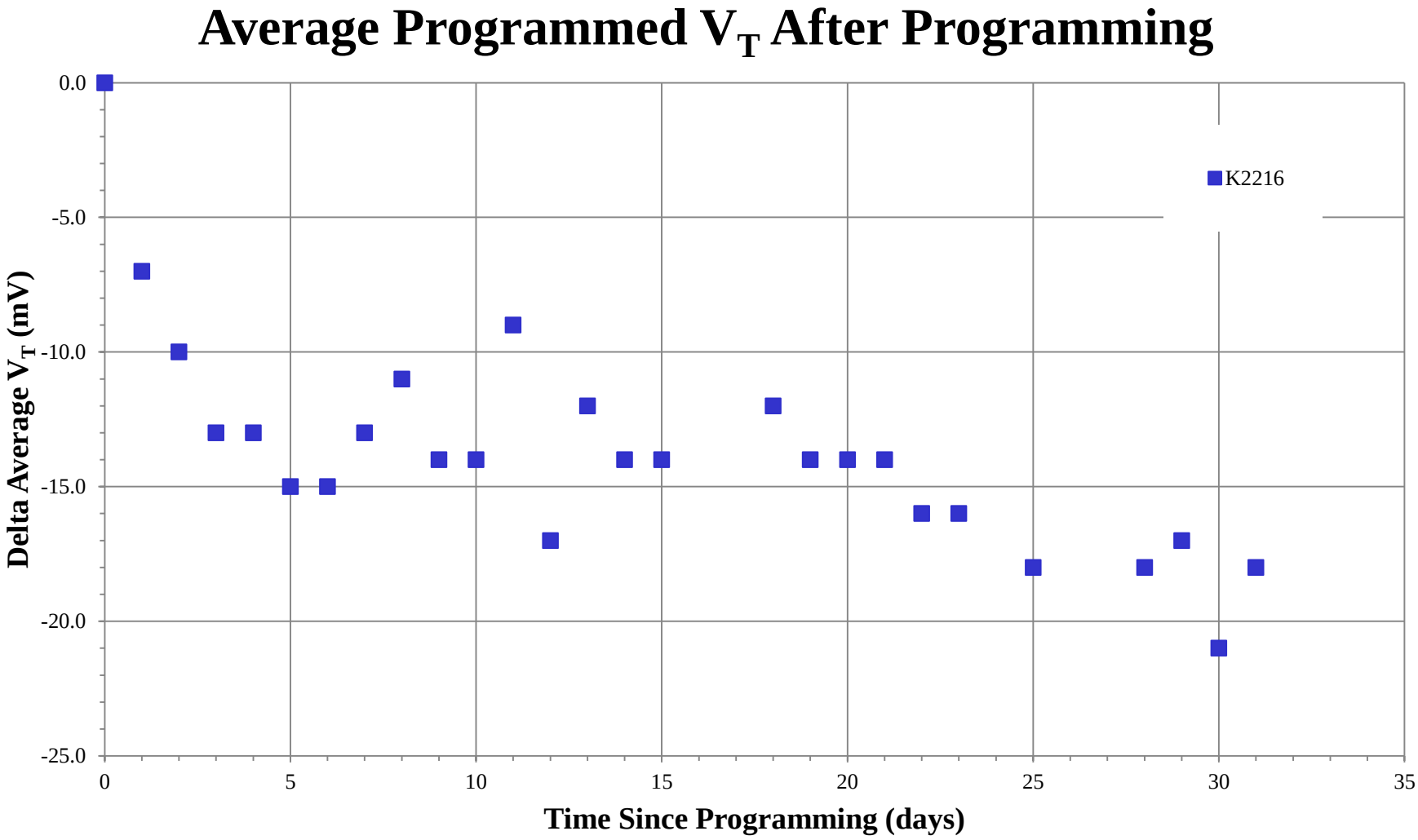
Initial Effects

- Engineering tests and data in literature showed an initial rapid movement in threshold voltage after configuring a device
- Three devices configured and then margin tested once per day
- Protocol updated: Baseline margin tests after several weeks of “settling time”

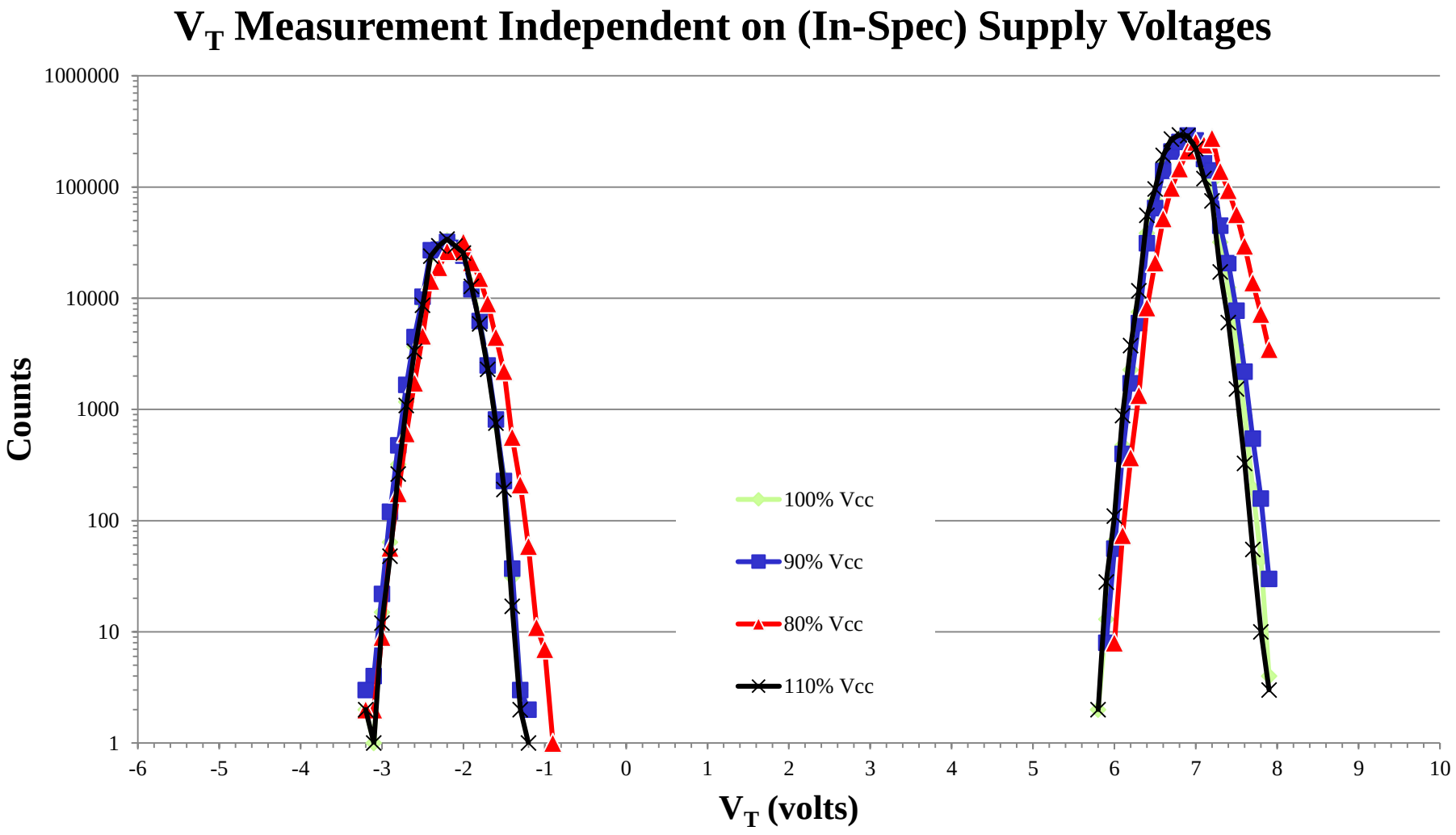
Initial Effects: Erased



Initial Effects: Programmed



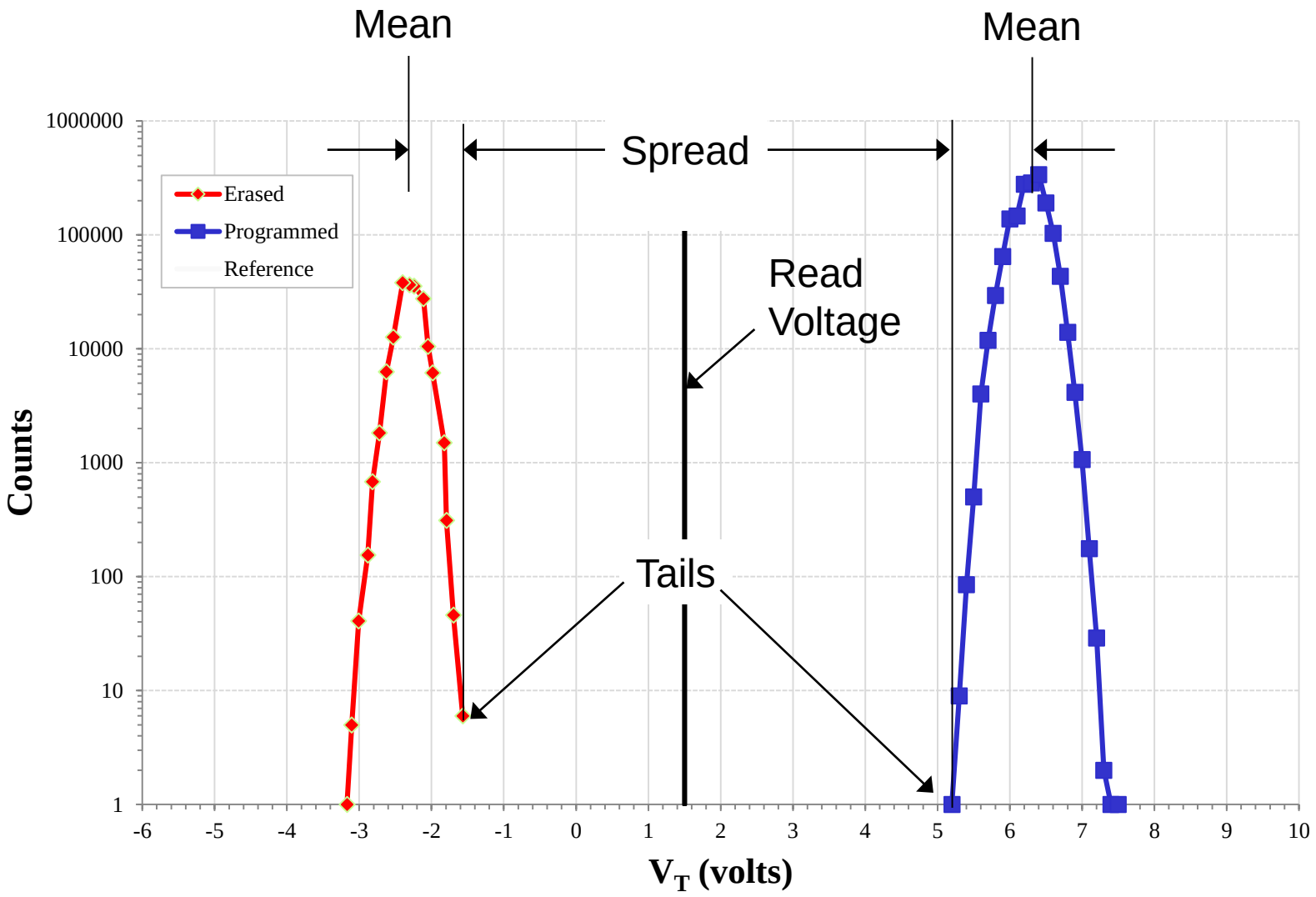
Instrumentation Sensitivity



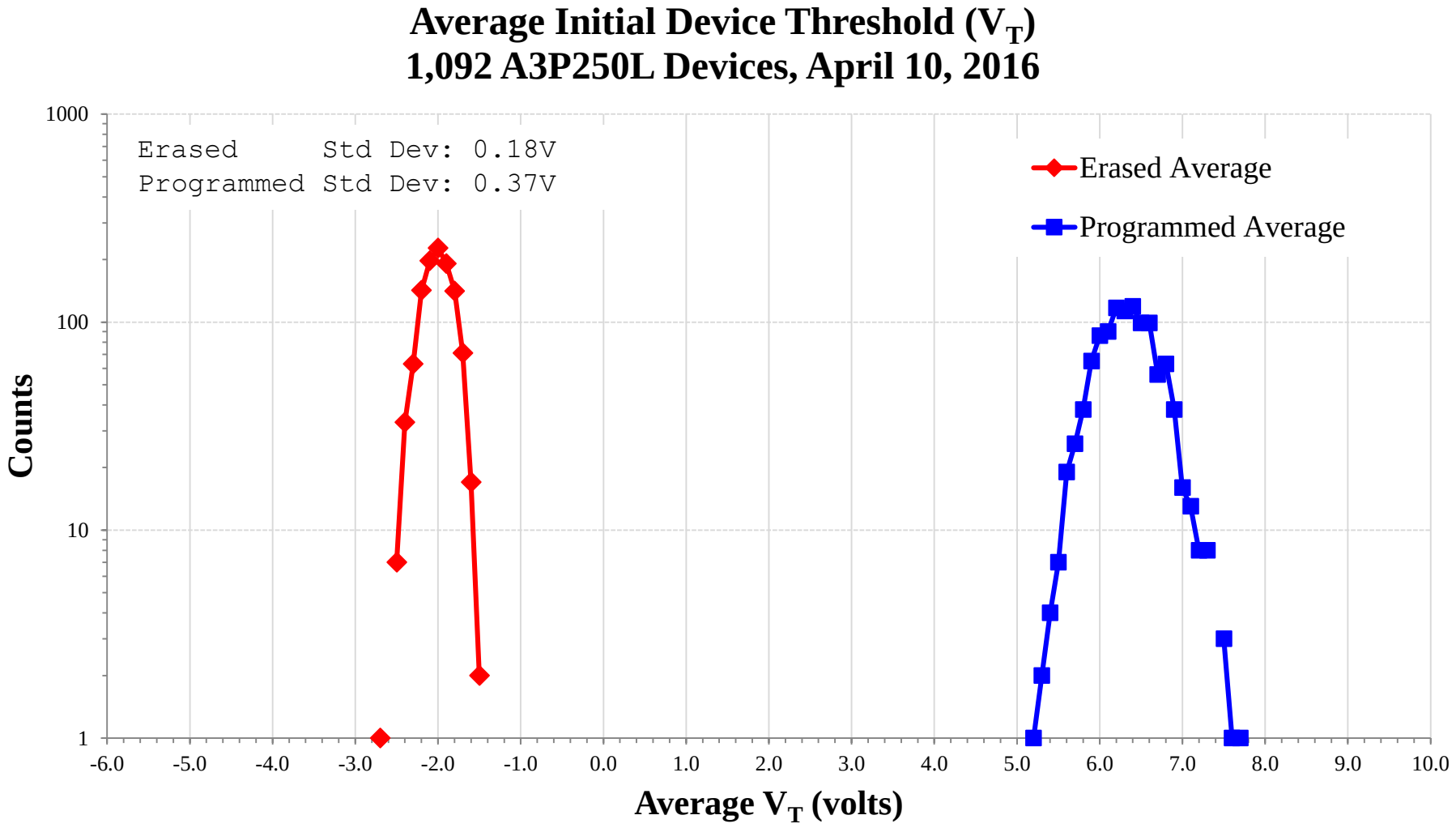
Population Analysis

- **Determined V_T Characteristics of a Large Population of Parts**
  - ~1,100 DUTs
- **Analysis Criteria on Threshold Voltage (V_T) Histograms**
  - Mean
  - Spread
  - Tails
  - Outliers

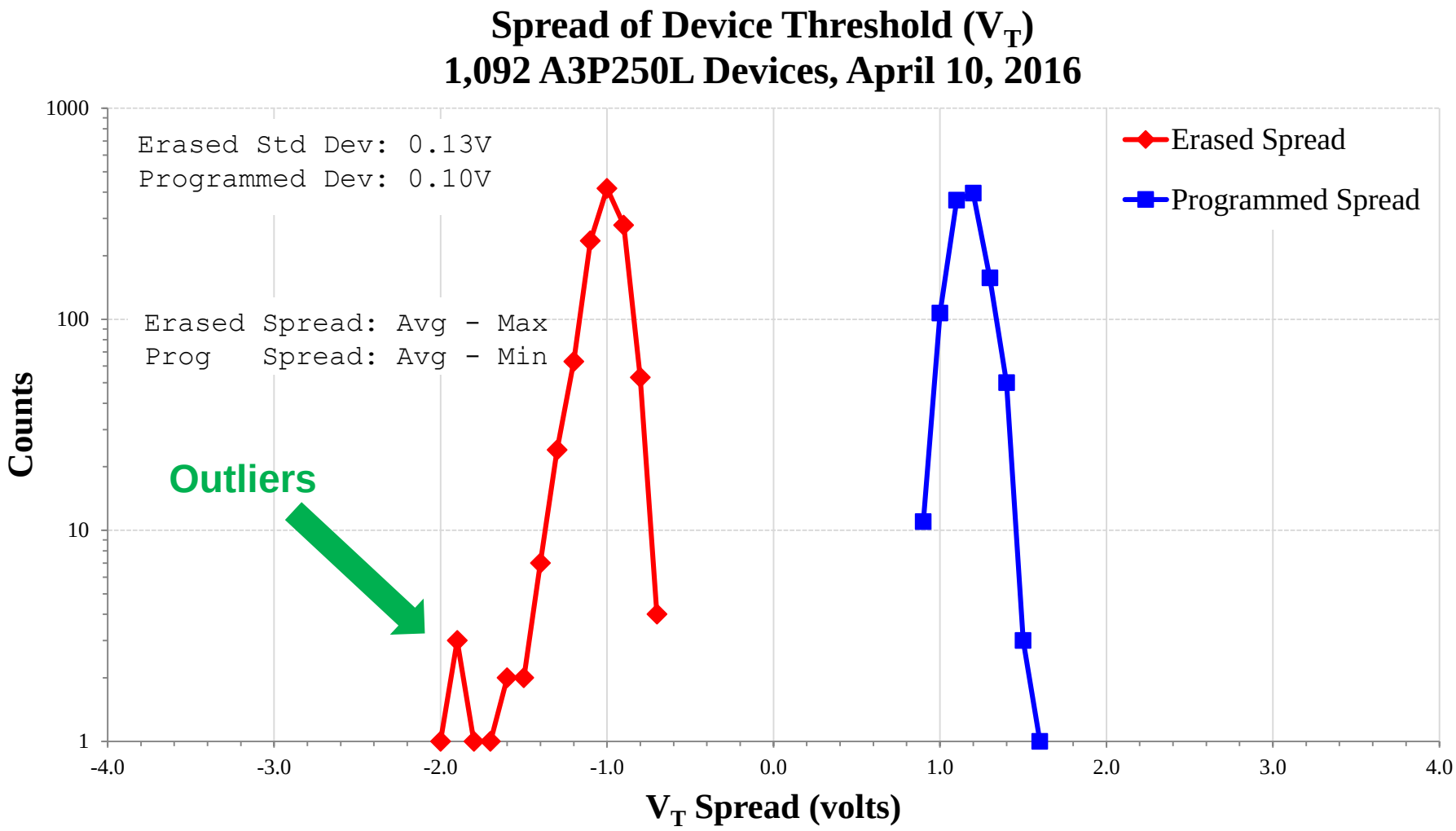
Population Analysis: Metrics



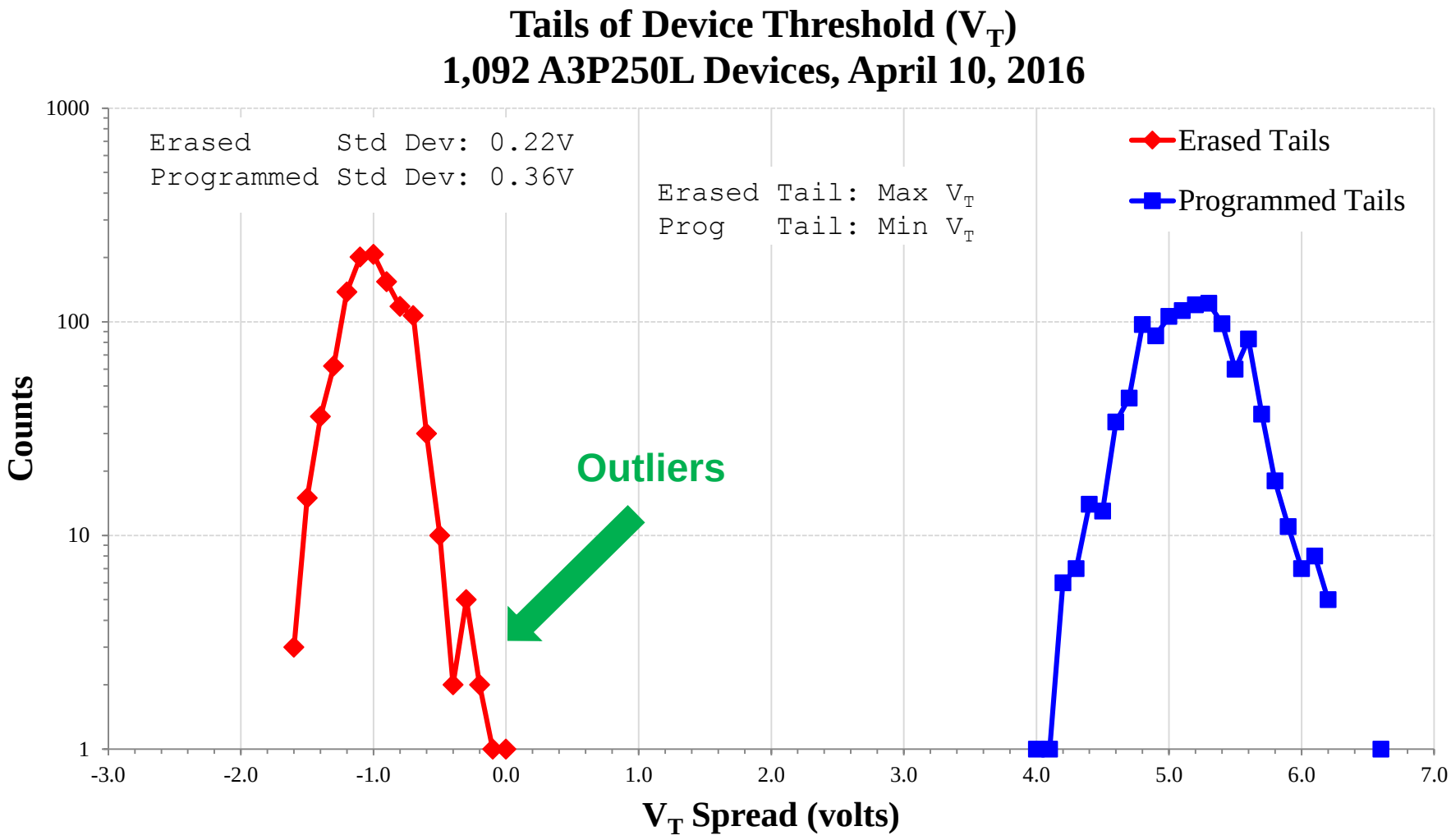
Population Analysis: Mean



Population Analysis: Spread

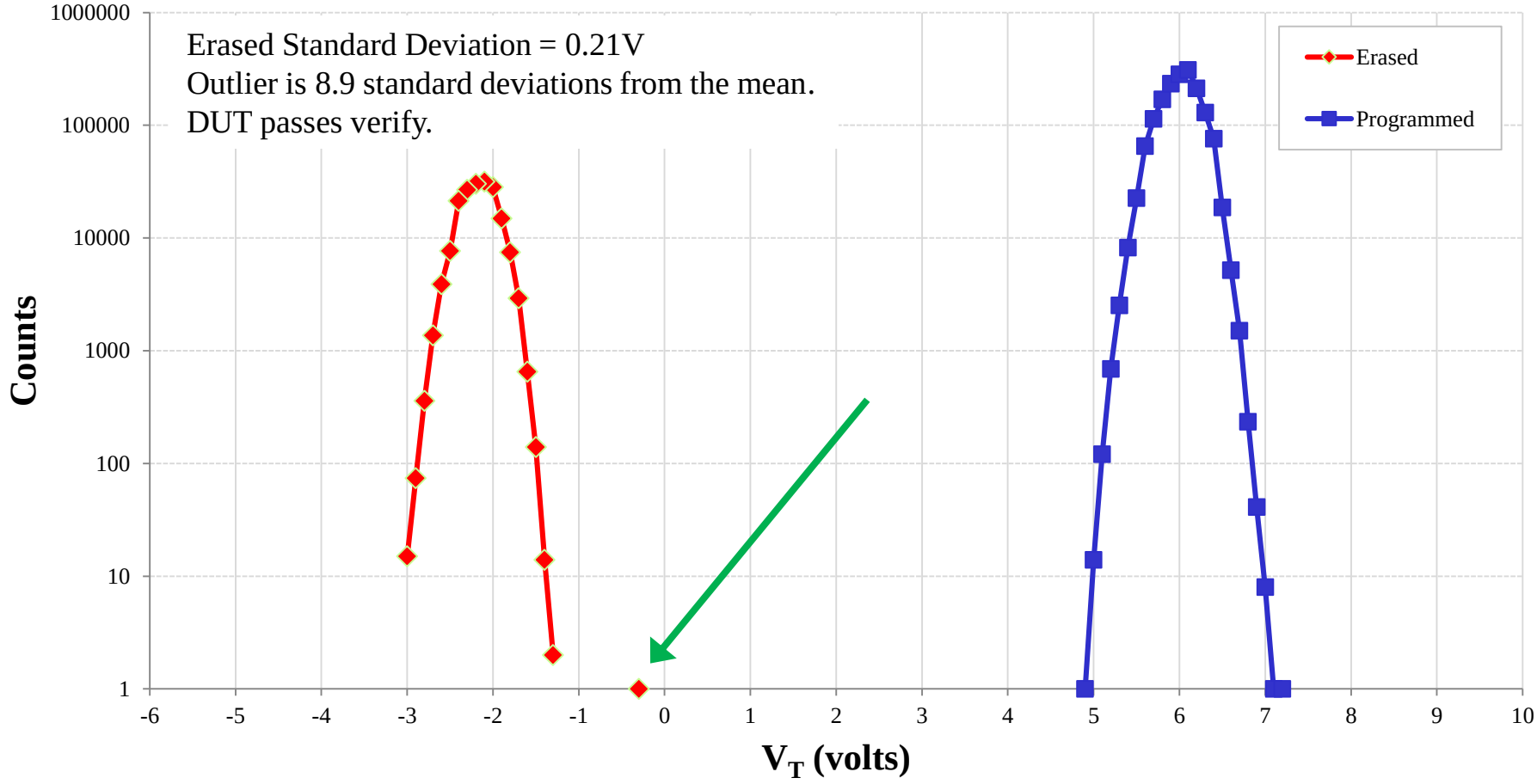


Population Analysis: Tails



Population Analysis: Outlier

S/N F0205, Initial Margin Test, March 10, 2016



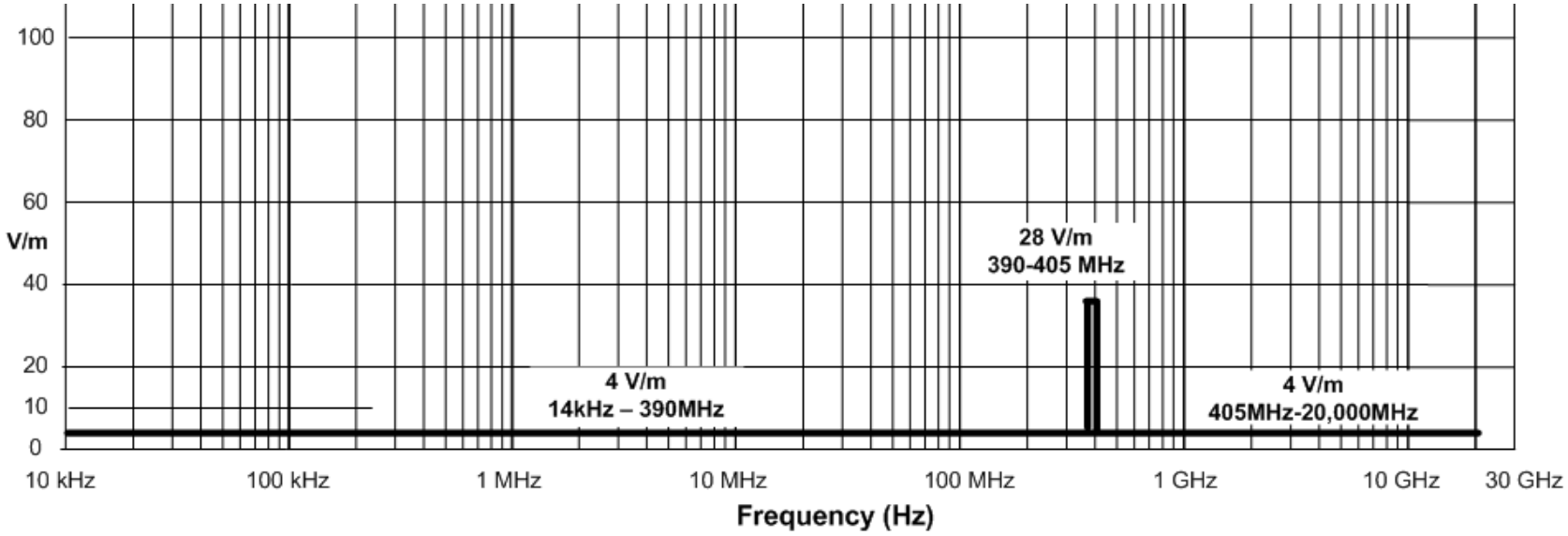
EM Susceptibility: Introduction

- **Goal: Determine Susceptibility of Flash Cell to EM Radiation**
- **DUT Configuration:**
  - 3 DUTs
  - Unpowered
  - No enclosure or other shielding
  - Simple Board: Traces for power, ground, and programming (not I/O)
- **A first test: Tested with a NASA Mars science instrument**
  - Multiple Runs with horizontal and vertical polarizations
  - Test levels based on science instrument (not fuze) requirements

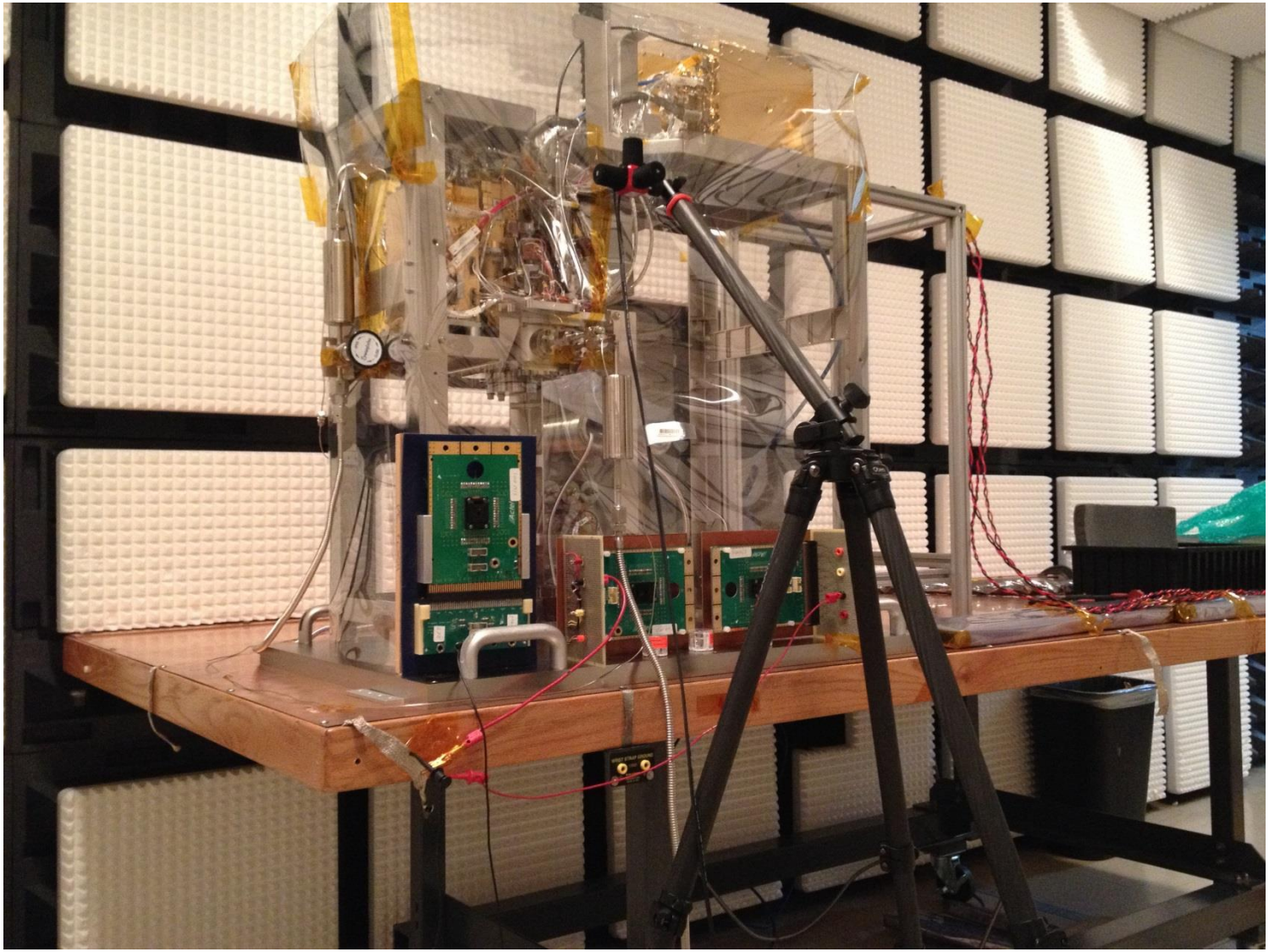
EM Susceptibility: Testing Levels

Table 3-8: RS103 Test Levels

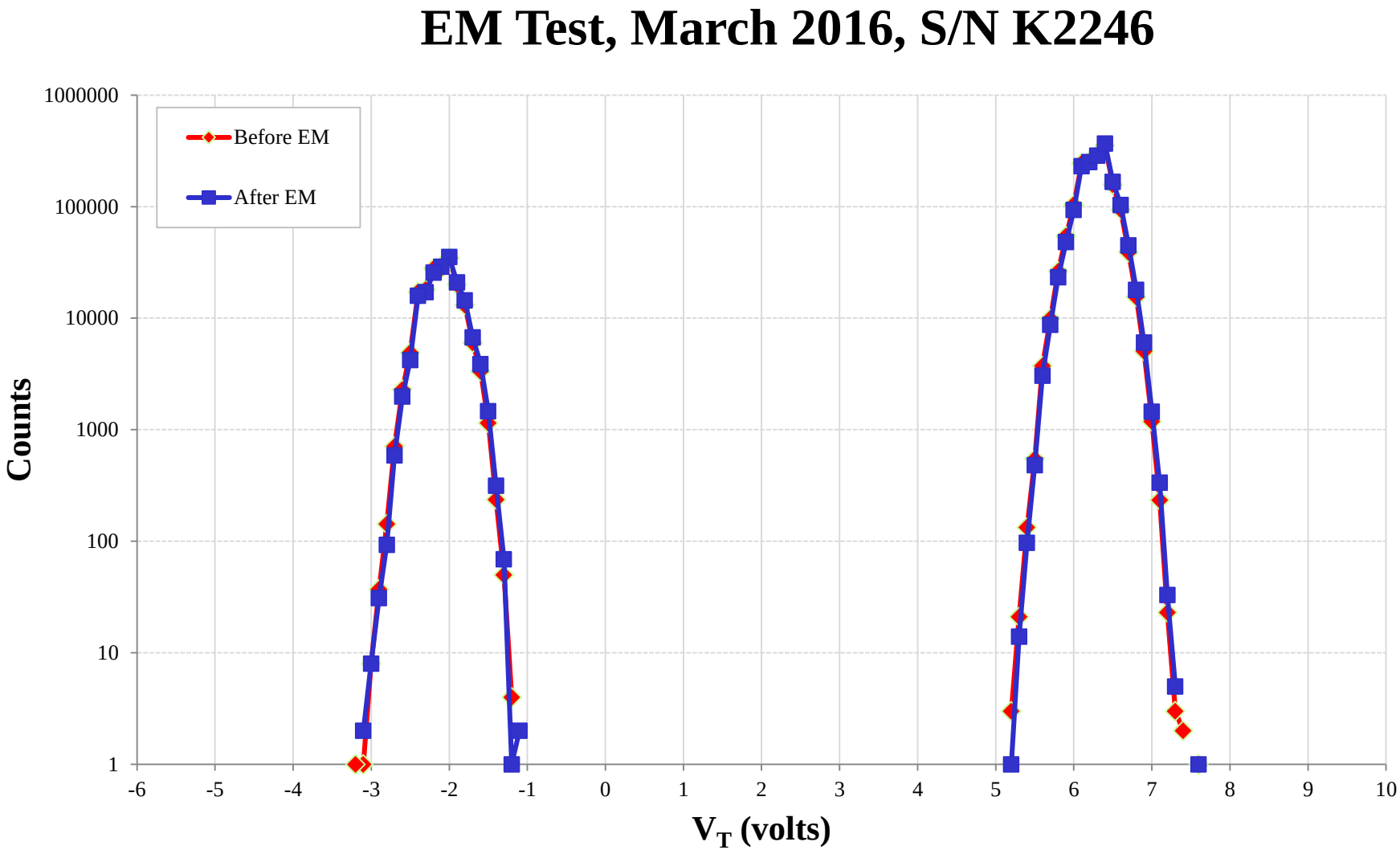
Frequency Band /Range	Test Level V/m (dBuV/m)	Notes
14 kHz to 390 MHz	4 V/m (132dBuV/m)	
309 MHz to 405 MHz	28 V/m (148dBuV/m)	UHF Band, Direct Downlink
405 MHz to 500 MHz	4 V/m (132dBuV/m)	
500 MHz to 3000 MHz	4 V/m (132dBuV/m)	WISDOM Payload
3000 MHz to 20,000 MHz	4 V/m (132dBuV/m)	



EM Susceptibility Testing Facility

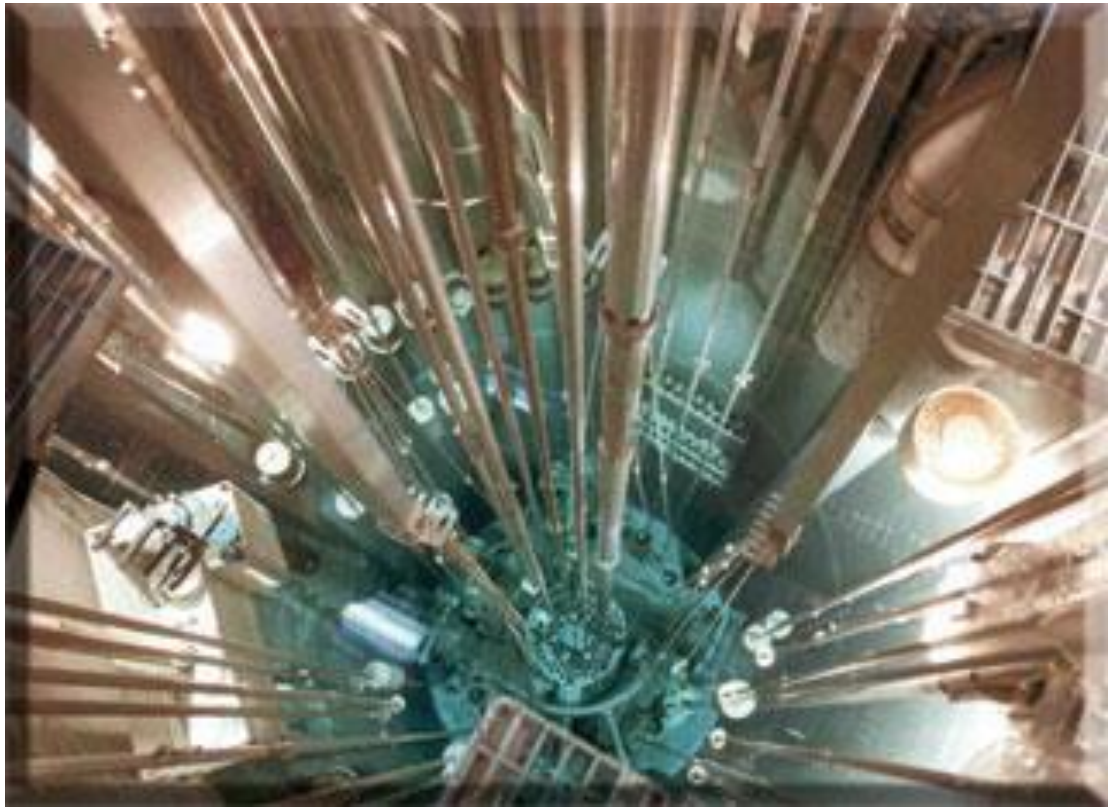


EM Susceptibility Results (typical)



Neutron Susceptibility Testing

- **Sample Size:** 20 DUTs
- **Test Levels:**
  - 2 x 10^{12} n/cm^2 (7 DUTs)
  - 2 x 10^{13} n/cm^2 (7 DUTs)
  - 2 x 10^{14} n/cm^2 (6 DUTs)
- **Test Conditions**
  - 1 MeV equivalent spectrum
  - DUTs unbiased
  - DUTs' balls shorted
- **Test Facility:** McClellan Nuclear Research Center (near DMEA)



MNRC Reactor in Operation

ESD Susceptibility Testing

- **Sample Size:** 20 DUTs
- **Test Levels:**
  - Phase Lock Loop (PLL): 500V
  - Other Power and I/O: 2 kV
- **Test Equipment:** Thermo Scientific MK.1 ESD and Static Latch-up Test System

Temperature Experiment Summary

Engineering Run

* 4 devices at 150 °C for 11,592 hours + 2 control samples
* One failure at 11,592 hours; probably mechanical, part undergoing analysis
* V_T shift very small

Large Population

* # of Parts Programmed: 1,091
* # of Parts Margined: 1,091
* # of Outliers[1]: 7 (~0.6%)
* # of Part Failures[2]: 1

322 Parts Soaking at 150 °C
327 Parts Soaking at 125 °C
333 Parts Soaking at 25 °C (add'l 57 being prepared)

[1]All outliers were erased cells and passed Verify test.
[2]K1631 would not margin or verify; likely non-flash failure, under failure analysis.

Summary, Conclusion, and Path Forward

- **Test Method and Data Analysis Tool Development**
  - Utilize Device's Design for Test Capability
  - Write Semi-custom Data Analysis Tools
  - Produce Credible, Useful Results
- **Testing Large Populations Necessary**
  - Significant Variability Between DUTs
  - Detect Outliers (~ 0.6 % for the subject device)
  - Significant Difference in Device Retention Time
- **Investigate Tighter Threshold Voltage (V_T) Limits on Verify Operation**
- **Assistance Needed on EM Test Limits, Protocols, and Facilities**
- **Possible Future Large Population Test: TI Microcontroller**
- **Track Large Populations: Temperature Testing Ongoing**
  - +25 °C, +125 °C, and +150 °C

References

- "**Anatomy of an in-flight anomaly: investigation of proton-induced SEE test results for stacked IBM DRAMs**," K. A. LaBel; P. W. Marshall; J. L. Barth; R. B. Katz; R. A. Reed; H. W. Leidecker; H. S. Kim; C. J. Marshall, IEEE Transactions on Nuclear Science, 1998, Vol.: 45, Issue: 6, pp. 2898 - 2903

- "**Long Term Data Retention of Flash Cells Used in Critical Applications**," K. Bergevin, R. Katz, and D. Flowers," 58th Annual Fuze Conference, July 7-9, 2015, Baltimore, MD.

- "**Viability of New COTS Technologies in Future Weapon Systems**," J.Marchiondo, et. al, Sandia National Labs, September 2010.

- "**Threshold voltage distribution in MLC NAND flash memory: characterization, analysis, and modeling**," Cai, Yu; Haratsch, Erich; Mutlu, Onur; and Mai, Ken, Proceedings of the Conference on design, automation and test in europe, ISSN 1530-1591, 03/2013, DATE '13, pp. 1285 – 1290.