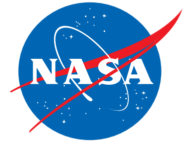
National Aeronautics and Space Administration



Processing and Characterization of Thousand-Hour 500 °C Durable 4H-SiC JFET Integrated Circuits

David J. Spry[1], Philip G. Neudeck[1], Liangyu Chen[2], Dorothy Lukco[3], Carl W. Chang[3], Glenn M. Beheim[1], Michael J. Krasowski[1], Norman F. Prokop[1],

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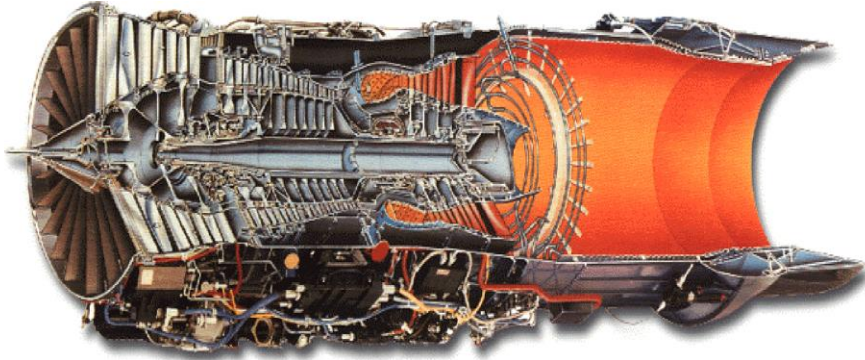
[2]Ohio Aerospace Institute

[3]Vantage Partners LLC

SiC Electronics Benefits to NASA Missions

Intelligent Propulsion Systems



Venus Exploration

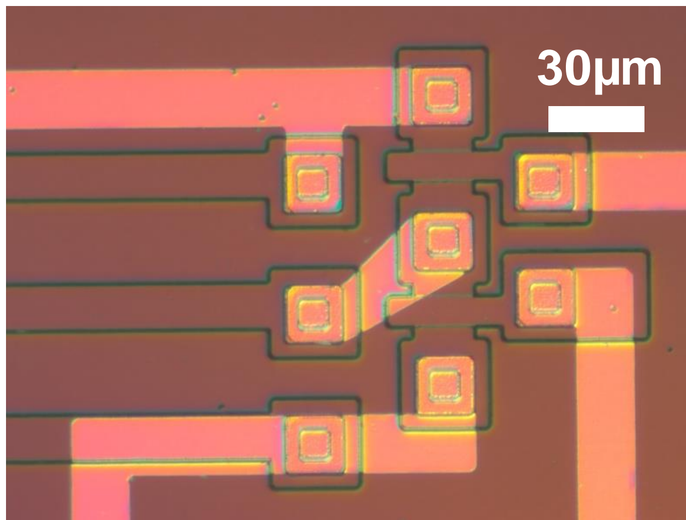
Hybrid Electric & Turbo Electric Aircraft

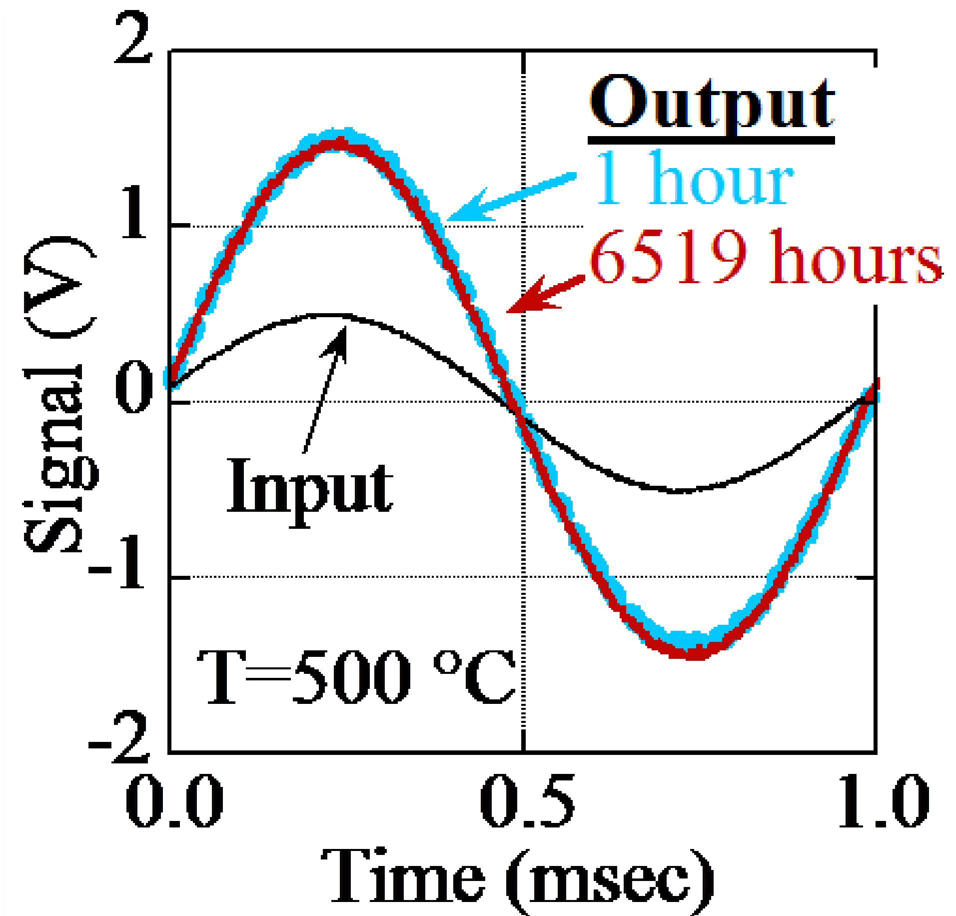
"GEER" Venus Test Chamber

NASA GRC's internal research effort has been to focus on durable integrated circuits at 500 °C for > 1000 hrs.

Past work with single layer of interconnect

- Differential amplifier made in 6H-SiC operated 6519 hours at 500 °C in air ambient.
- Complexity limited. Only 2 transistors and 3 resistors.
- JFET approach good for minimizing gate leakage and durability at 500 °C.





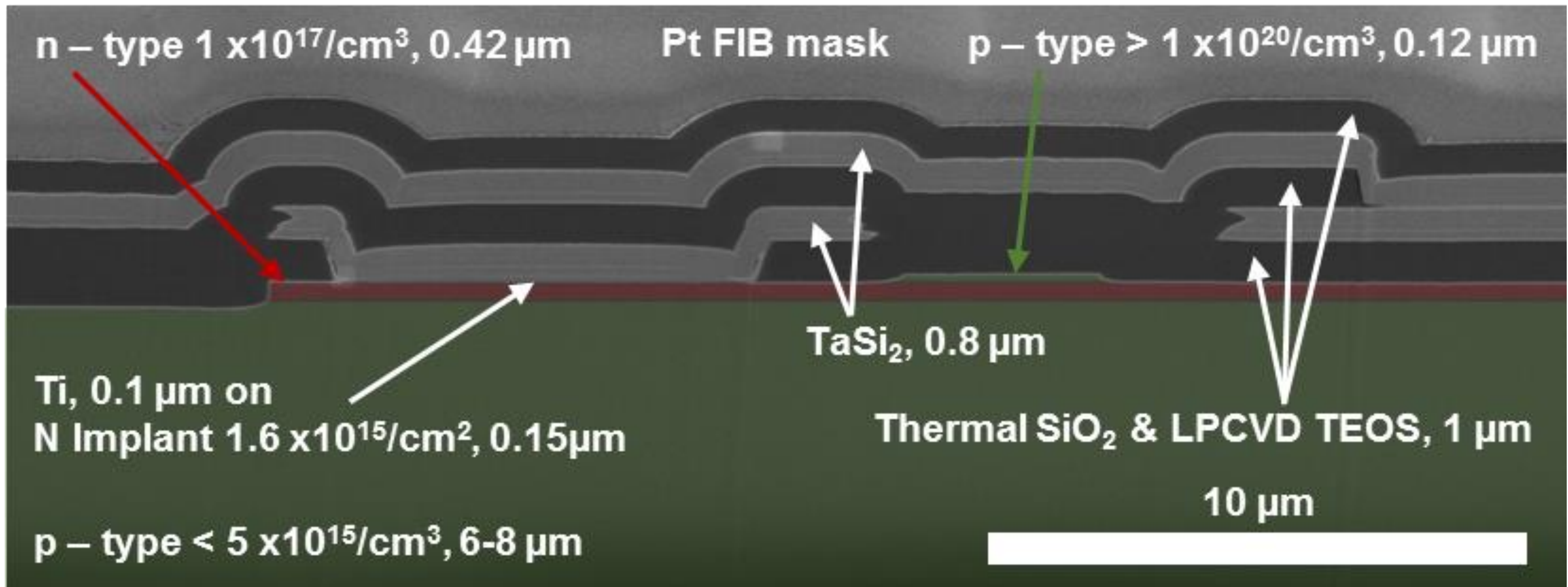
Phys. Status Solidi A **206**, No. 10, 2329–2345 (2009)

8.1 vs past work - Two level interconnect

Processing enhancements for conformal processing on topology.

- Proximity sputtering of $TaSi_2$ (21mm target to substrate spacing).
- LPCVD tetraethyl orthosilicate (TEOS) deposited 720 °C.
- Design rules for thick dielectrics and metal traces.

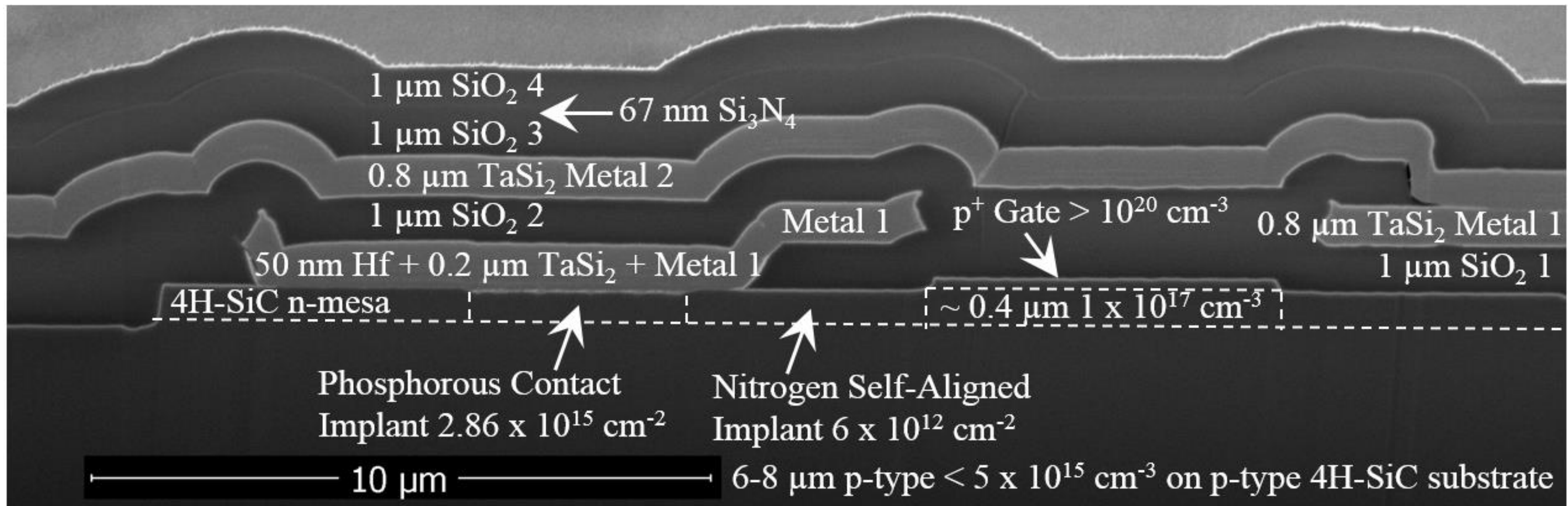
Enables crisscrossing traces and on chip capacitors. Now 4H not 6H



Materials Science Forum. 858, pp. 908-912 (2016)

8.1 vs 9.2

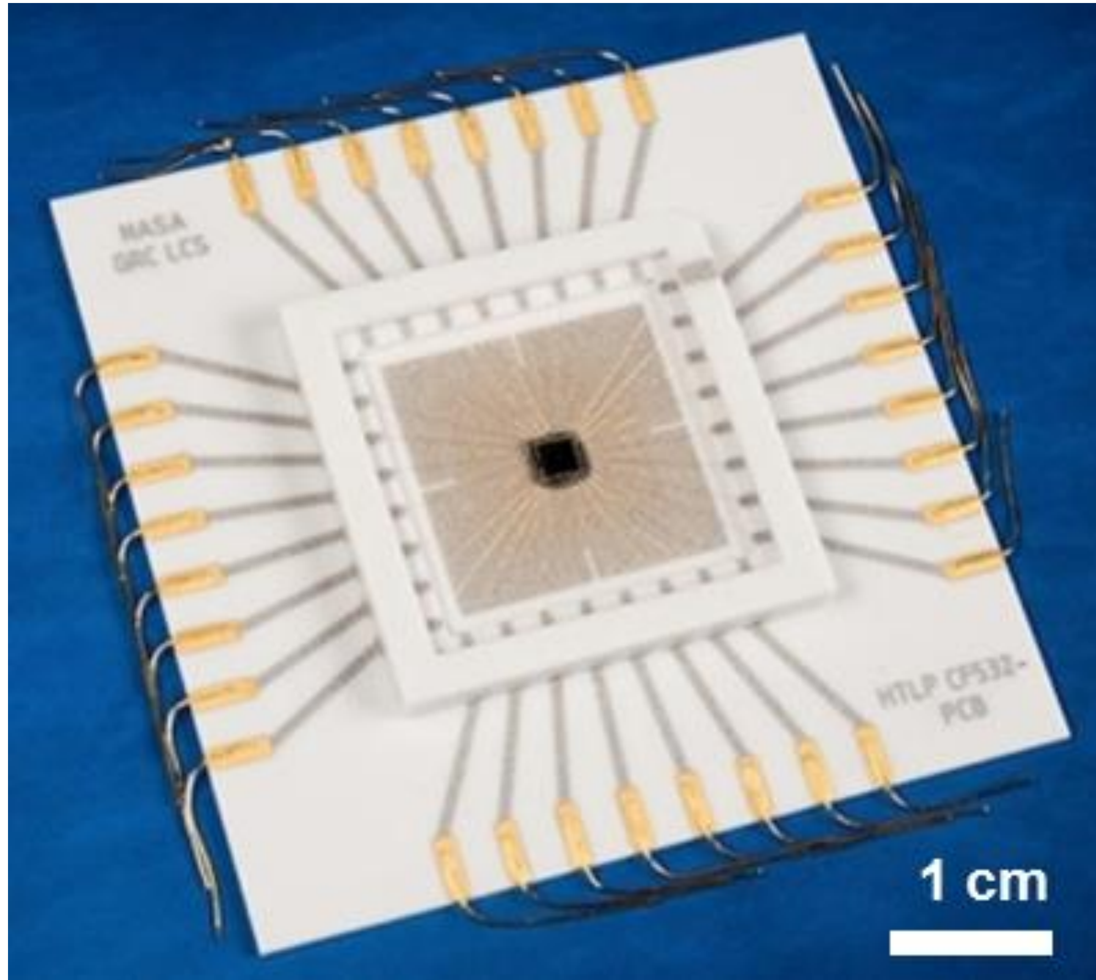
- "Gate notching" present in 8.1 JFETs were eliminated for 9.2 JFETs.
- Heavily-implanted SiC contact regions were formed using **P** implantation for 9.2 chips instead of **N** implantation used for 8.1 chips.
- SiC contact for 9.2 chips was implemented using a 50 nm sputtered **Hf** layer instead of the 50 nm sputtered **Ti** layer used for 8.1 chips.
- The 9.2 added a **67 nm Si_3N_4** layer in top dielectric.
- Extensive laboratory improvements to mitigate **Na** contamination were implemented for 9.2 wafer processing.



IEEE Electron Device Letters. (2016)

New high-T packaging (32 pins)

See Dr. Liangyu Chen's talk at HiTEC for more.

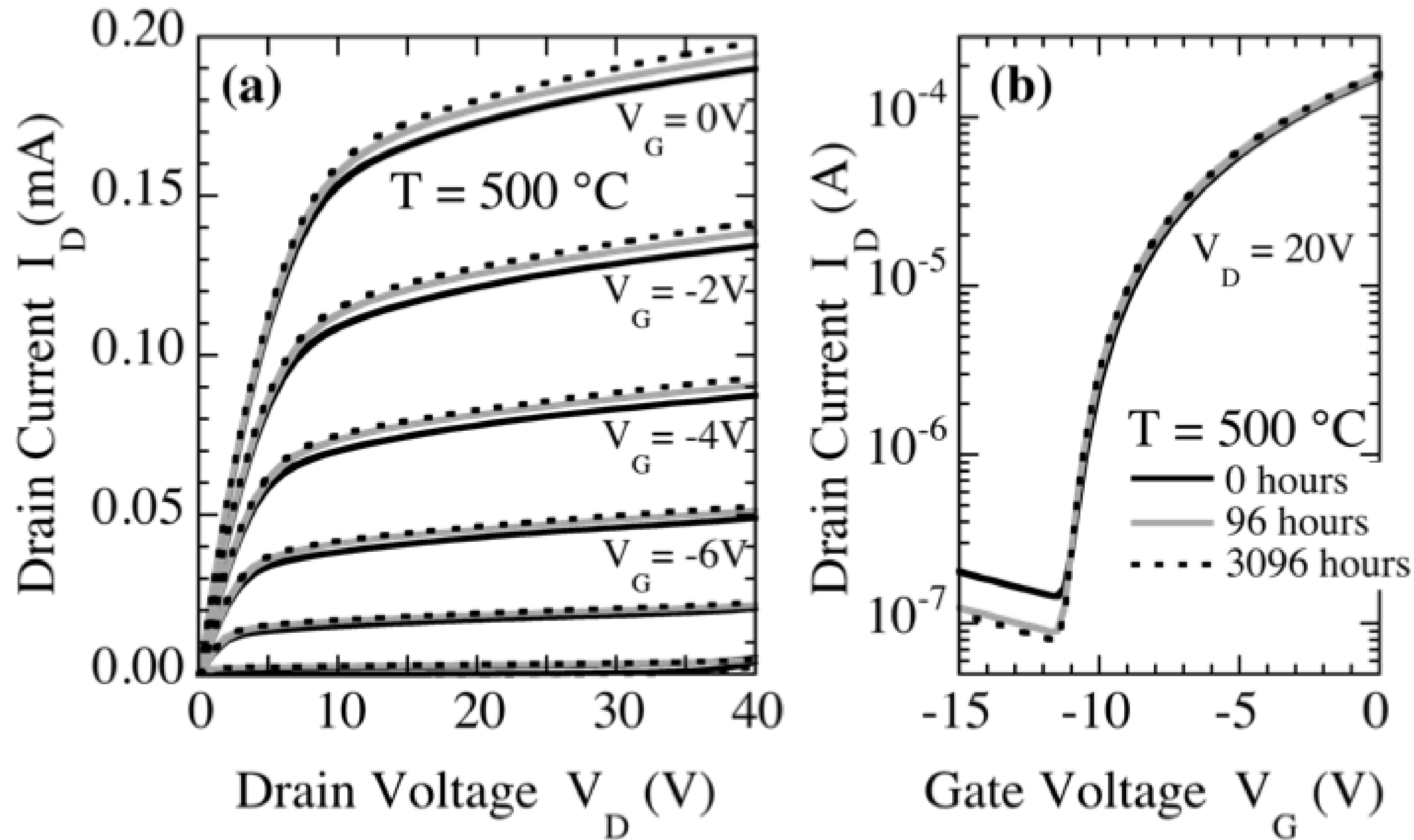


Wafer 9.2 IC Functional Yield at 25 °C

Integrated Circuit Designation	# FETs	# Good	# Tested	% Yield
MF Gate 3-Stage Ring Oscillator	10	36	39	92%
HF Gate 3-Stage Ring Oscillator	10	66	78	85%
Op Amp Design A	10	19	20	95%
Op Amp Design B	10	18	20	90%
LF Gate 3-Stage Ring Oscillator	12	35	41	85%
LF Gate 11-Stage Ring Oscillator	24	37	41	92%

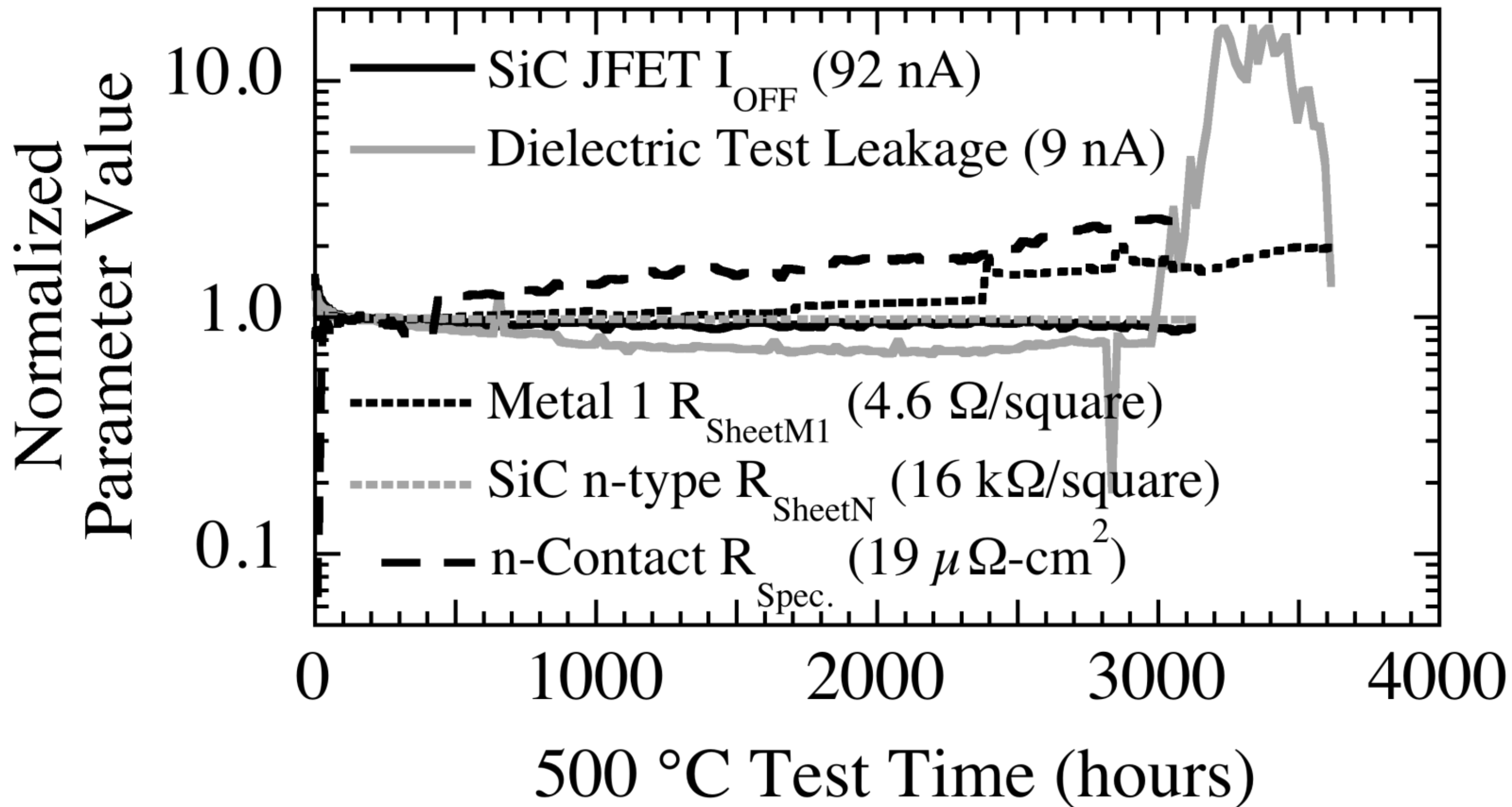
LF, MF and HF = low, medium, and high frequency

9.2 JFET Characteristics at 500 °C vs. Time



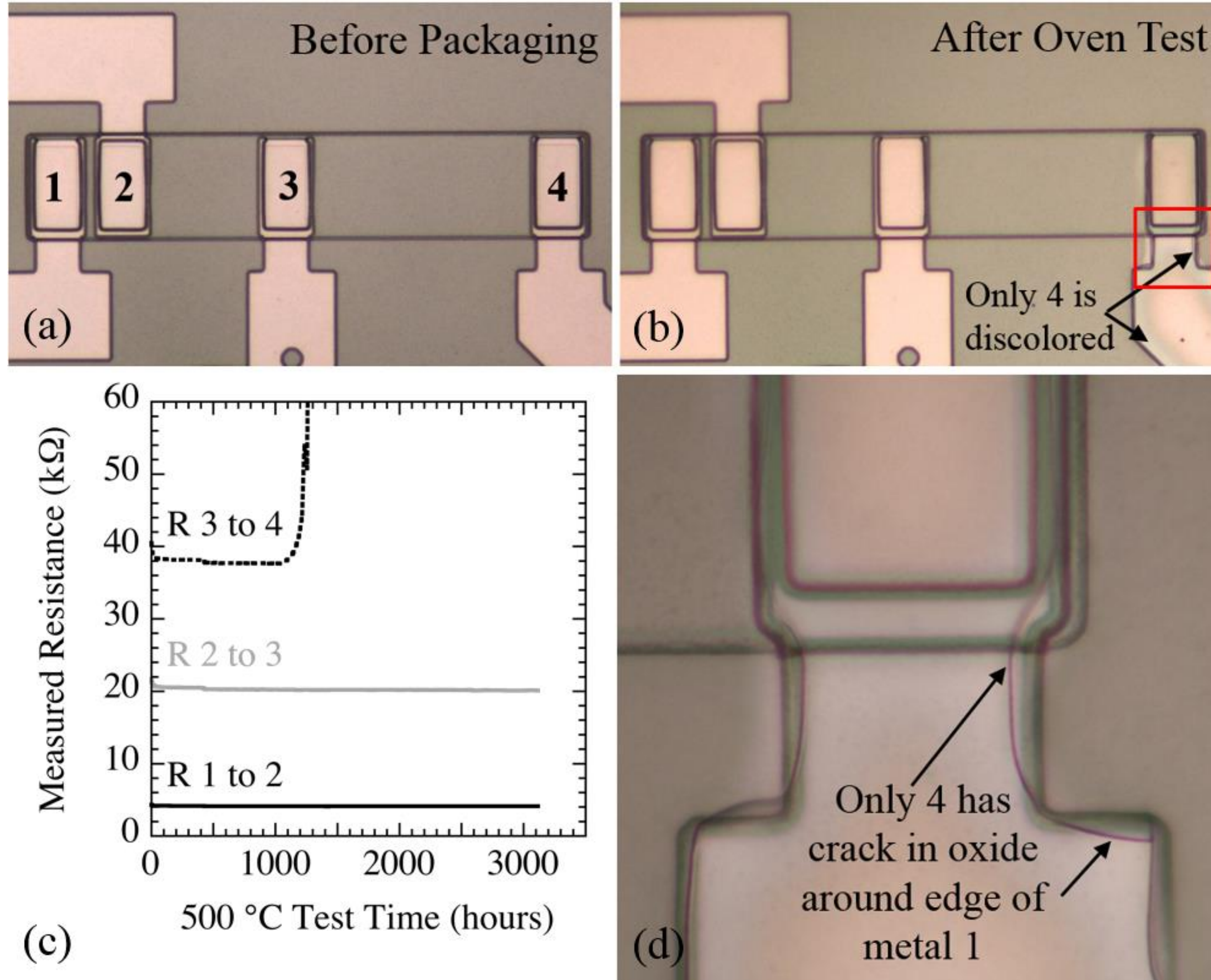
Measured 12µm/6µm JFET (a) I_D vs. V_D and (b) I_D vs. V_G at 0, 96, and 3096 hours of packaged 500 °C testing with V_S = -15V. This JFET was from a chip ***r*** = 23 mm from the wafer center.

9.2 Device Parameters at 500 °C vs. Time



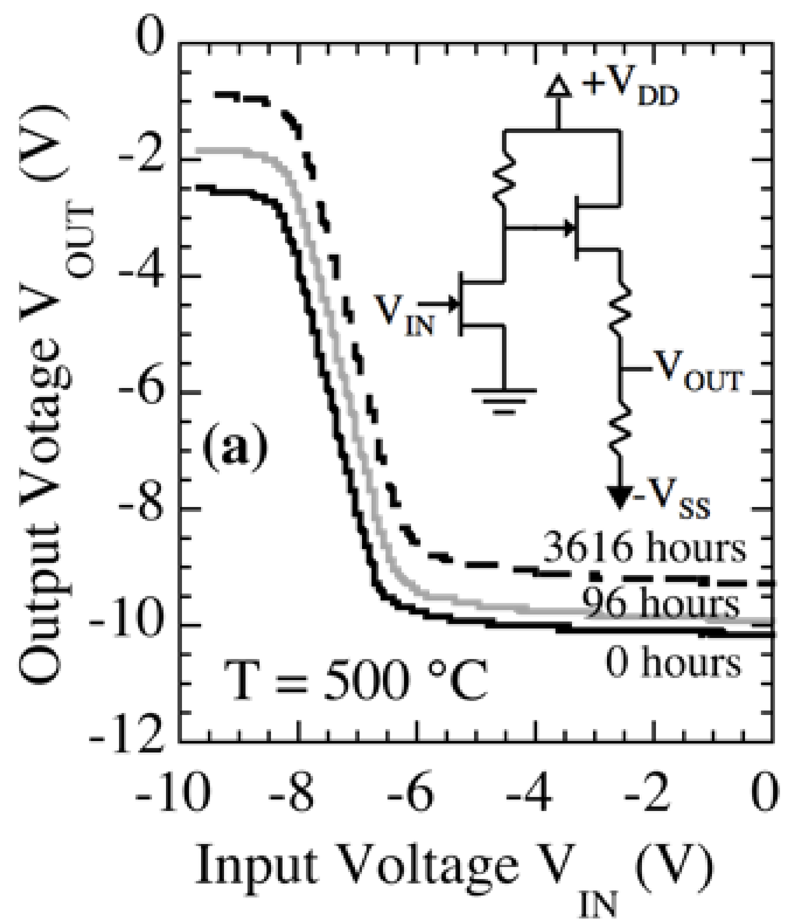
Selected process test device parameters for the 3615 hours at 500 °C, plotted normalized to each parameter's value 96 hours into the test (96 hour values shown in parenthesis).

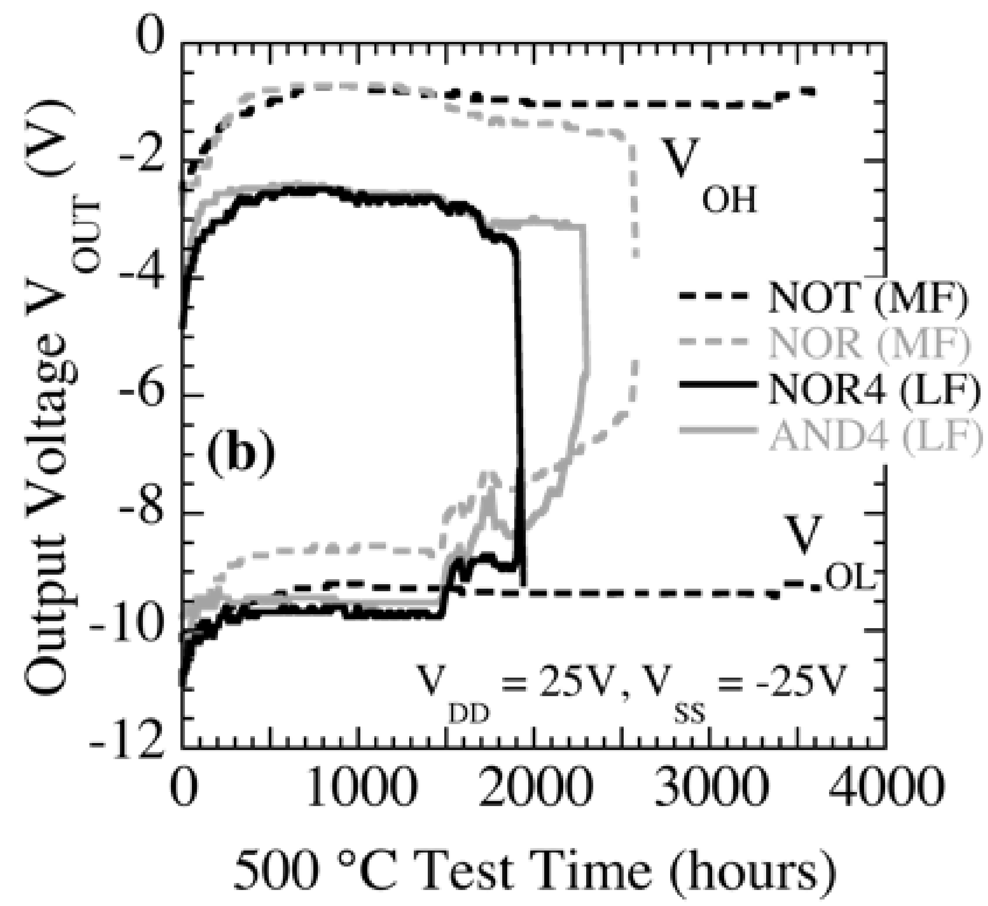
TLM



(a) Before packaging optical image. (b) After oven test image of the same TLM. Only contact 4 shows electrical failure as can be seen in the plot of R_{12}, R_{23}, and R_{34} in (c). A crack in the dielectrics that allowed for the oxidation of the $TaSi_2$ which causes discoloration can be seen in both (b) and (d).

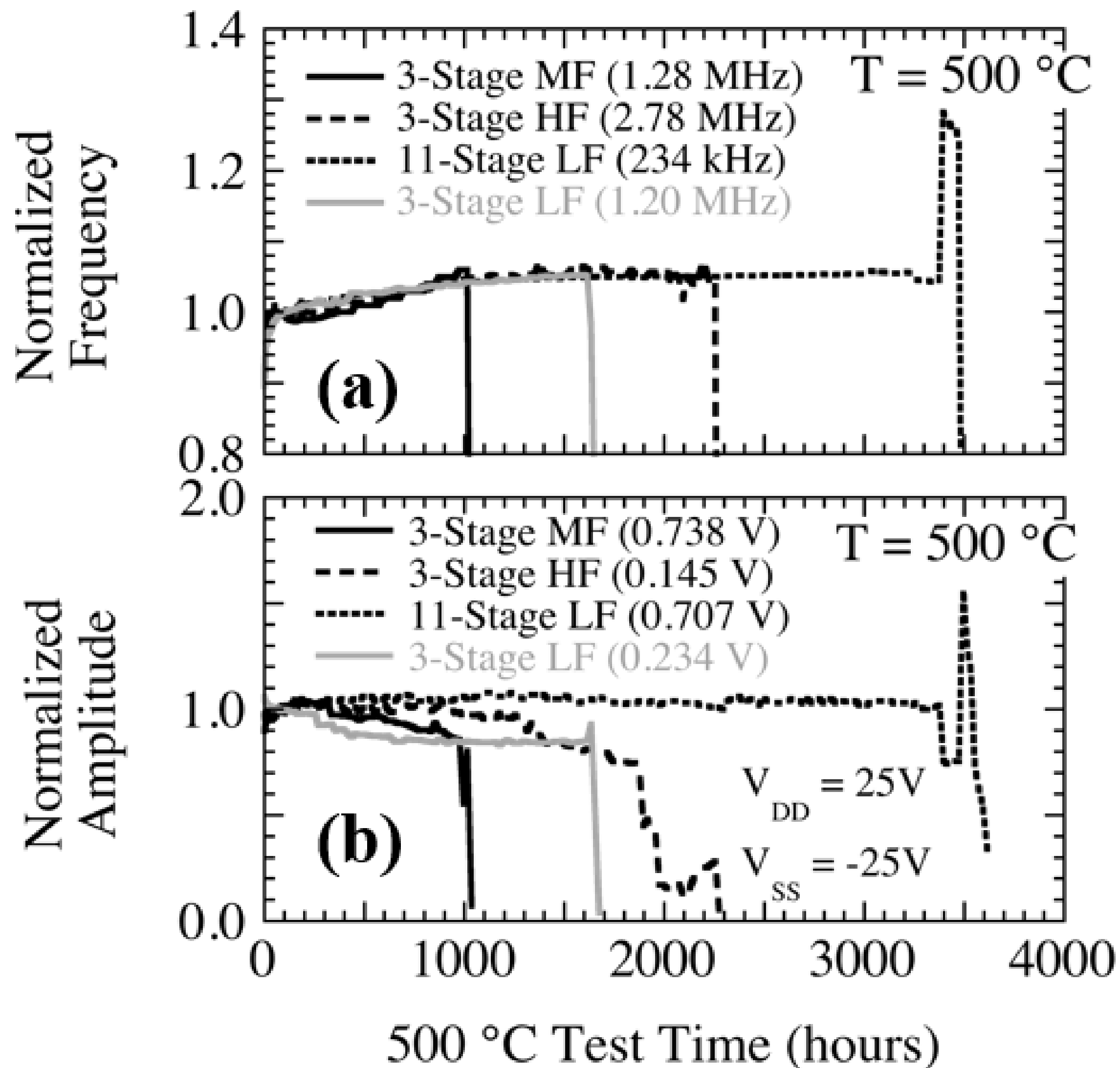
Logic Devices at 500 °C vs. Time





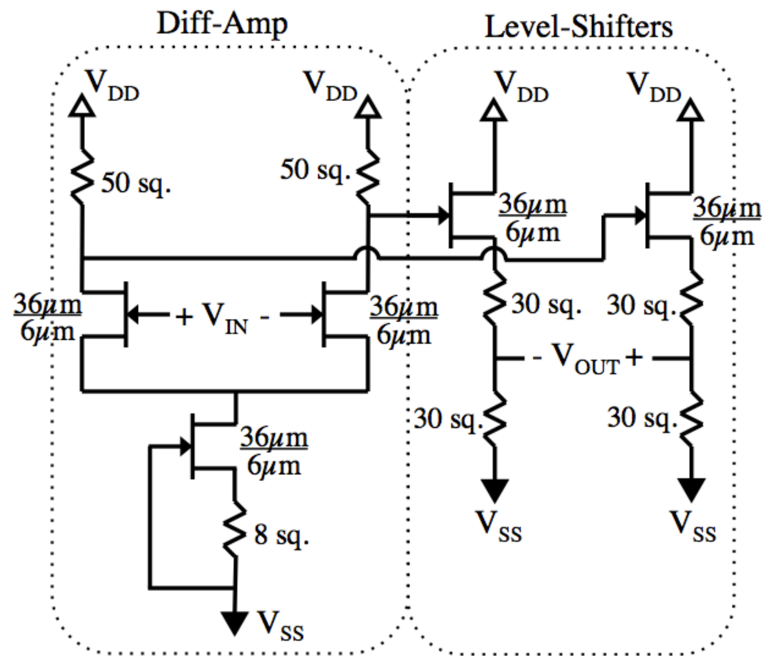
Measured 500 °C (a) MF NOT gate V_{OUT} vs. V_{IN} transfer characteristics at selected test times, and (b) V_{OH} and V_{OL} for all oven-tested logic gates vs. 500 °C test time.

Ring Oscillators at 500 °C



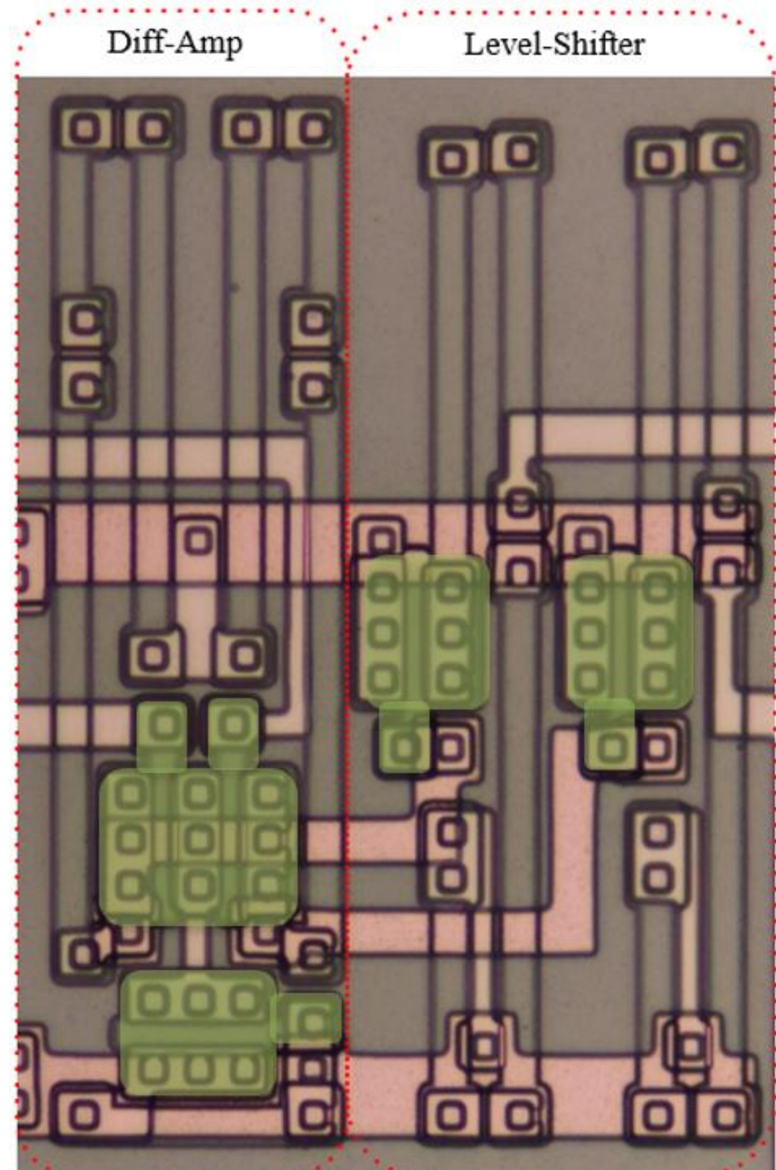
(a) Ring oscillator frequency and (b) ring oscillator amplitude vs. 500 °C testing time for all high temperature packaged oscillators, normalized to each oscillator's frequency 96 hours into the 500 °C test (shown in parenthesis).

Amplifiers

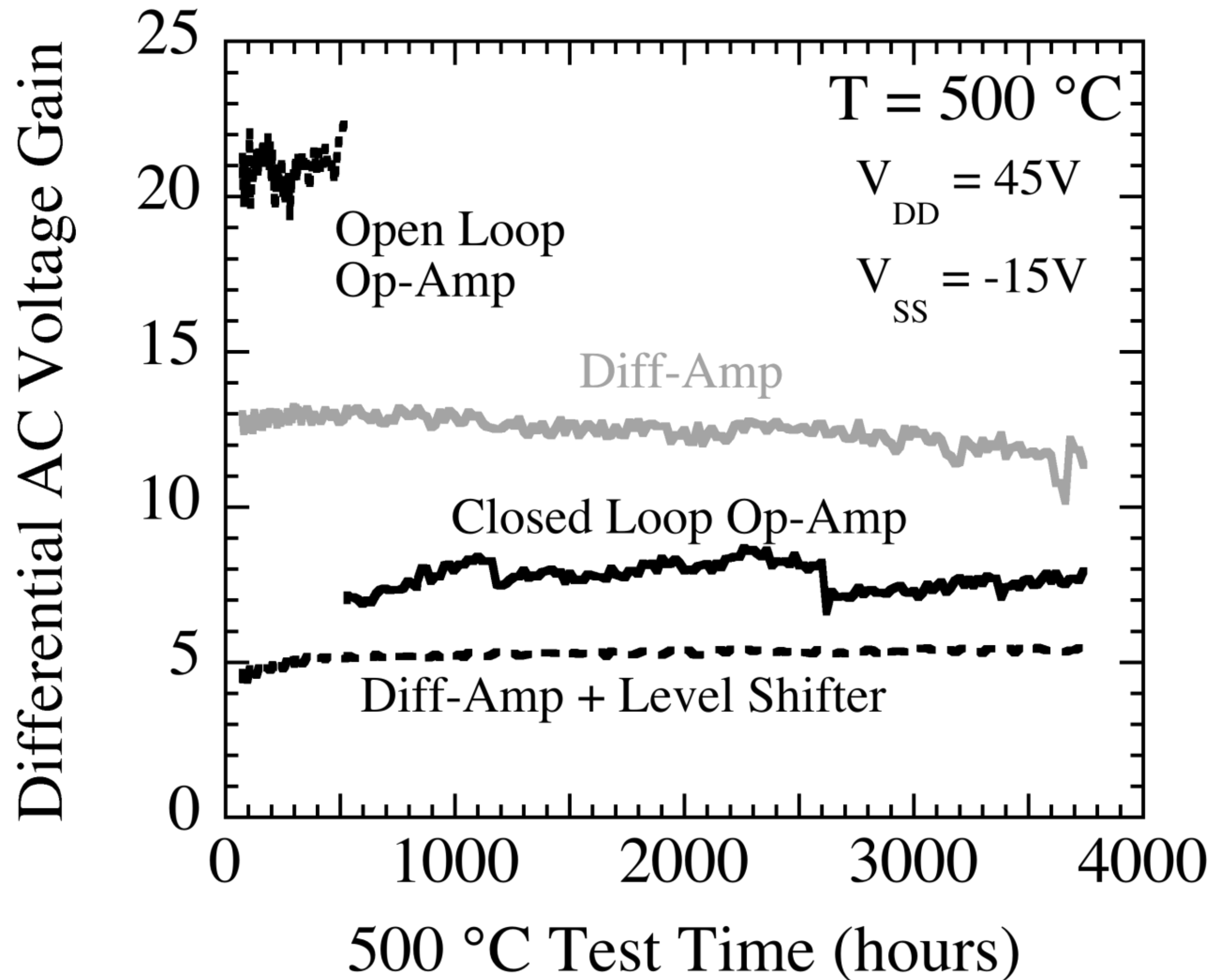


(Above) Schematic diagram of diff-amp and level shifters.

(Right) Optical image of diff-amp and level shifter. JFETs are highlighted in green.

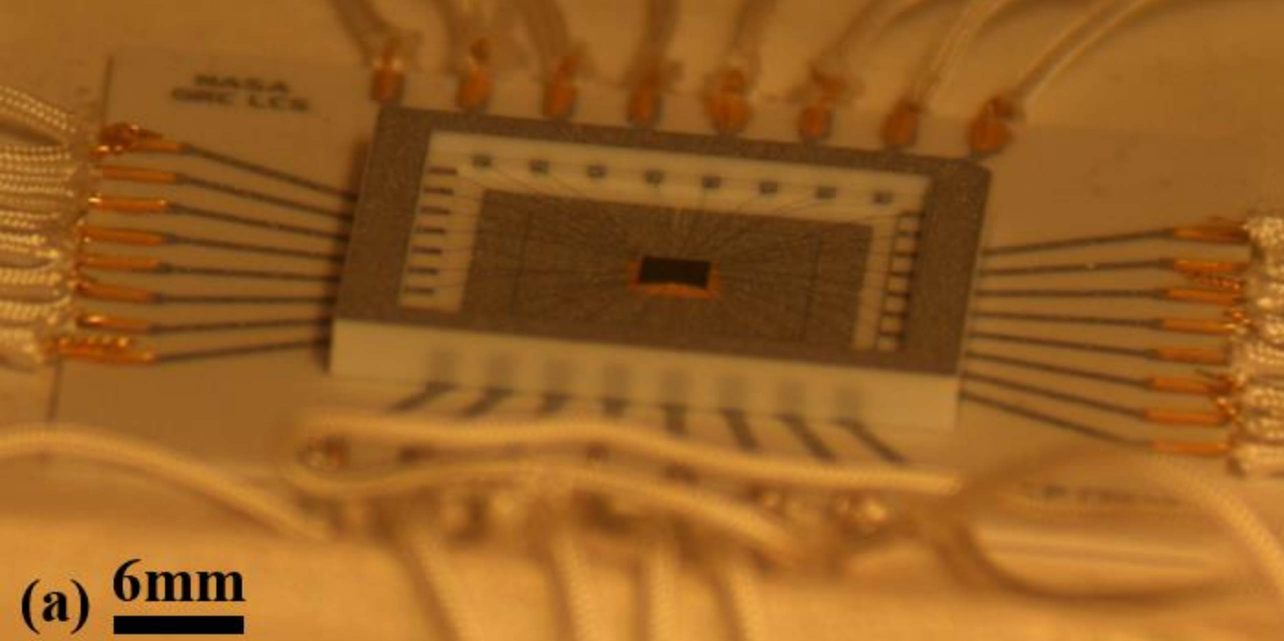


9.2 Amplifiers at 500 °C vs. Time

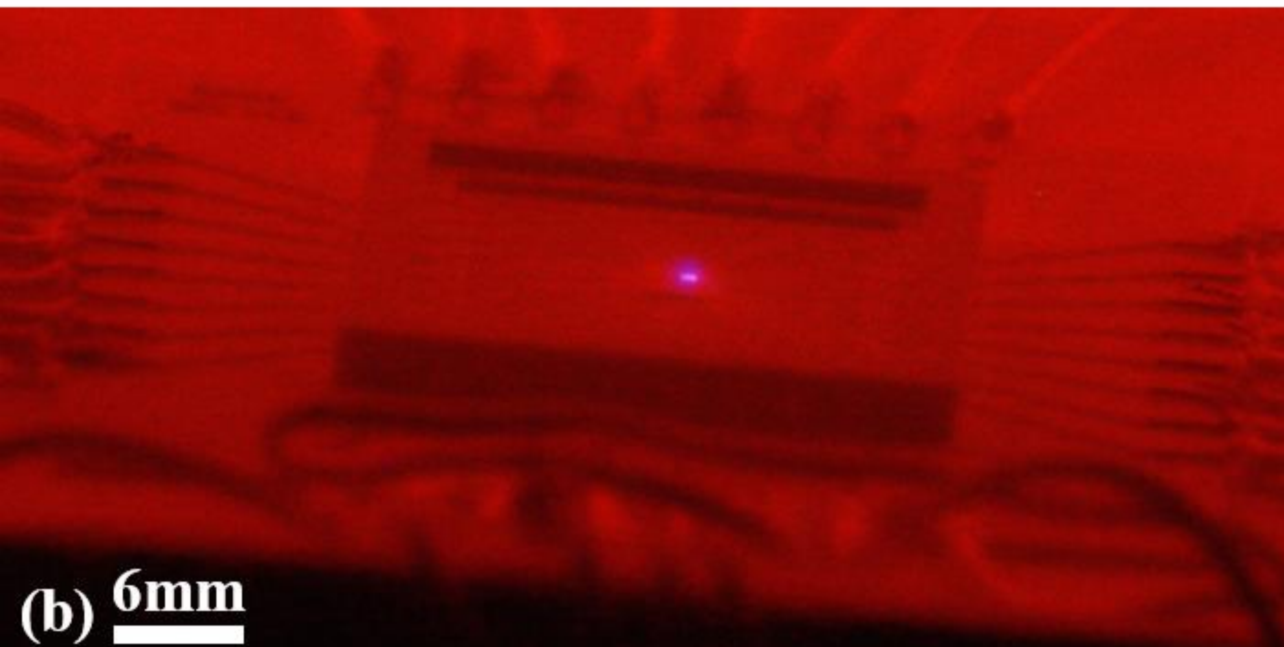


Measured differential small-signal voltage gain vs. 500 °C amplifier testing time.

650 °C Test



Optical image of packaged device with room light illumination.



Optical image at 650 °C of packaged device with a large JFET under forward bias of the gate-channel junction resulting in blue light emission. Three ring oscillators and a MF NOT are also operating while the image is taken.

Conclusion

- This work has initially demonstrated two-level interconnect digital and analog integrated circuits consistently operating past 1000 hours at 500 °C with better than 80% yield.
- These results significantly advance prospects for realizing complex and 500 °C durable ICs for sensing and control circuits in combustion engine, planetary, deep-well drilling, and other extreme-environment applications.
- While further failure analysis studies are needed, the basic dielectric cracking followed by metal oxidation failure mechanism could be responsible for the majority of long-term 500 °C circuit failures for chips from this wafer.
- Continued temperature testing/analysis, degradation/failure analysis, and further up-scaling of IC transistor counts are planned.

Acknowledgements

Funded by **NASA Transformative Aeronautics Concepts Program**

HX5 Sierra

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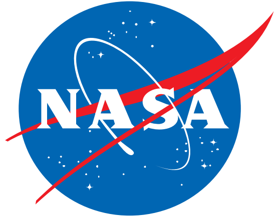
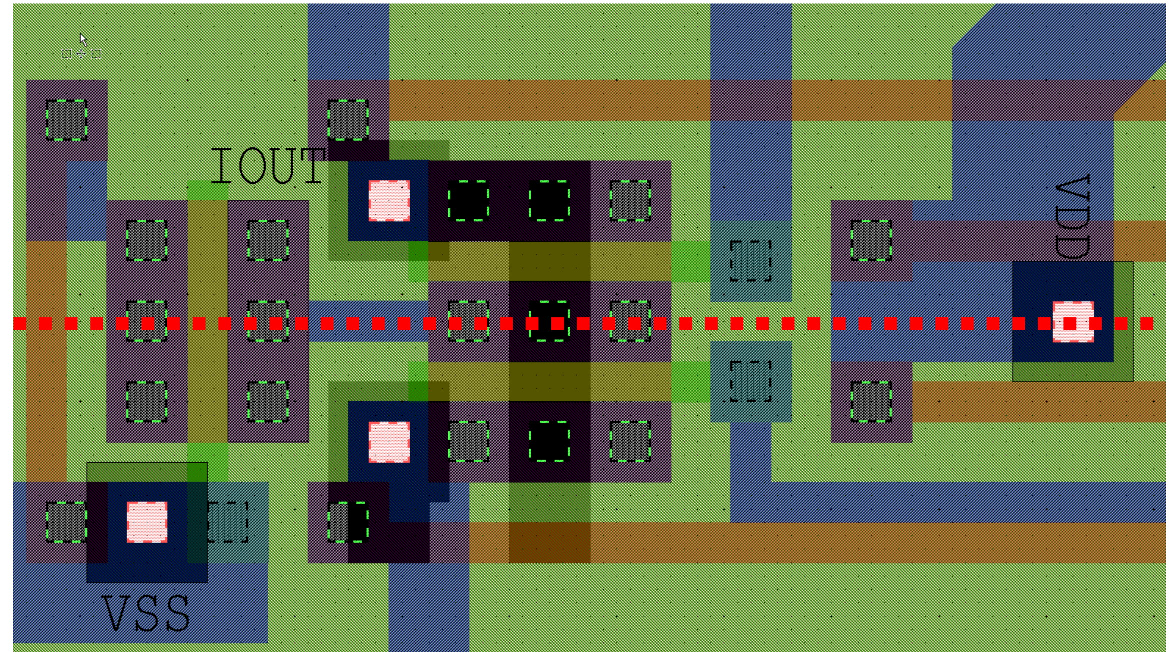
- Amir Avishai



Integrated circuits in fabrication

Circuit	Inputs	Outputs	Transistors, I/O Pads	Comments
4-Bit A/D	Analog voltage signal, optional external clock, output type select	4 bit parallel digital latch, pulse width modulated (PWM)	203 JFETs, 23 I/Os	Internal ring-oscillator clock circuit
4X4 Bit Static RAM	Read, Write, Data Lines, Address Lines	4 bit parallel digital latch, pulse width modulated (PWM)	220 JFETs, 30 I/Os	Address decoder, sense amplifiers
Source Separation Sensor Signal Transmitter	Capacitive sensor	Frequency modulated with address code	301 JFETs, 20 I/Os	Each sensor signal is tagged with unique address code
Ring Oscillators	Capacitive sensors	Frequency modulated signals (up to 500 MHz)	10-12 JFETs, 6 I/Os	On-chip large transistors for power amplification
Binary Amplitude Modulation RF Transmitter	Low power binary signal	High-Power RF signal to antenna		Could connect with PWM from A/D
Op Amp, 2-Stage	Differential	Voltage gains to 50 w/ on-chip resistors	10 JFETs	For piezoelectric SiC pressure sensors
4-Bit D/A	4 digital	1 analog	20 JFETs	

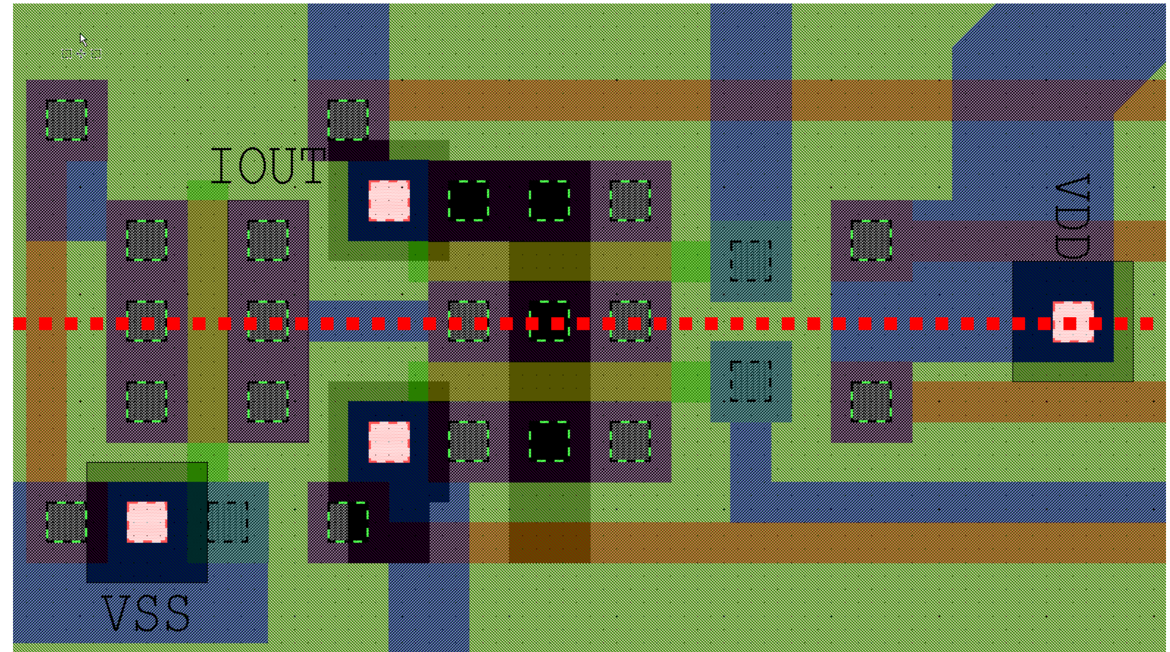
Process with two levels of metal interconnect



- Gate $N_A > 2 \times 10^{20}$ cm^{-3} at 0.17µm thick
- n-channel 1×10^{17} cm^{-3} at ~0.5 µm thick
- Lower p material $< 3 \times 10^{15}$ cm^{-3} at ~6-8 µm thick.

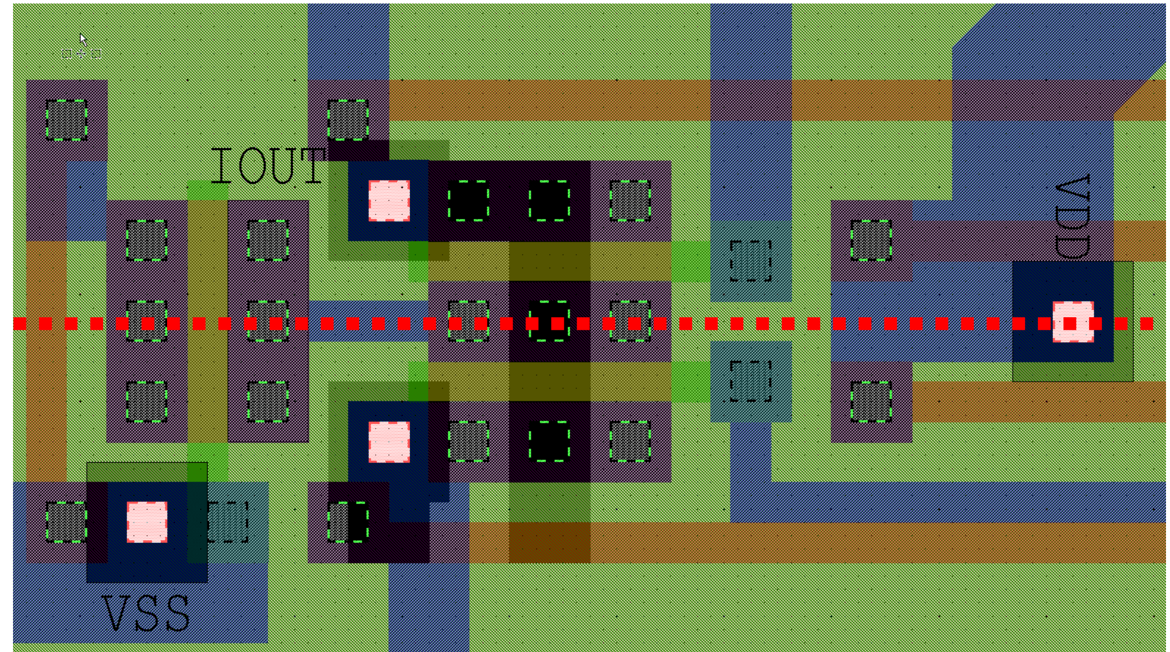
Process with two levels of metal interconnect

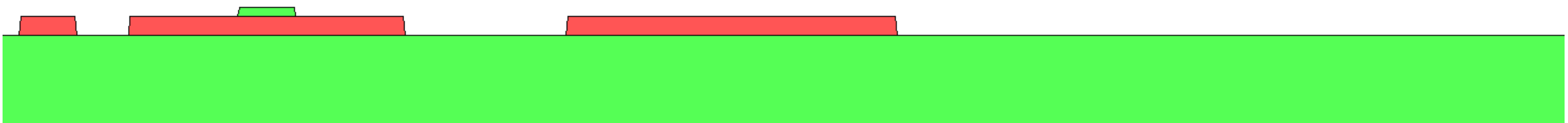
- Ti/Ni etch mask for gate.
- Self align nitrogen implant of dose 7.0 x 10^{12}cm^{-2} at 70 KeV.



Process with two levels of metal interconnect

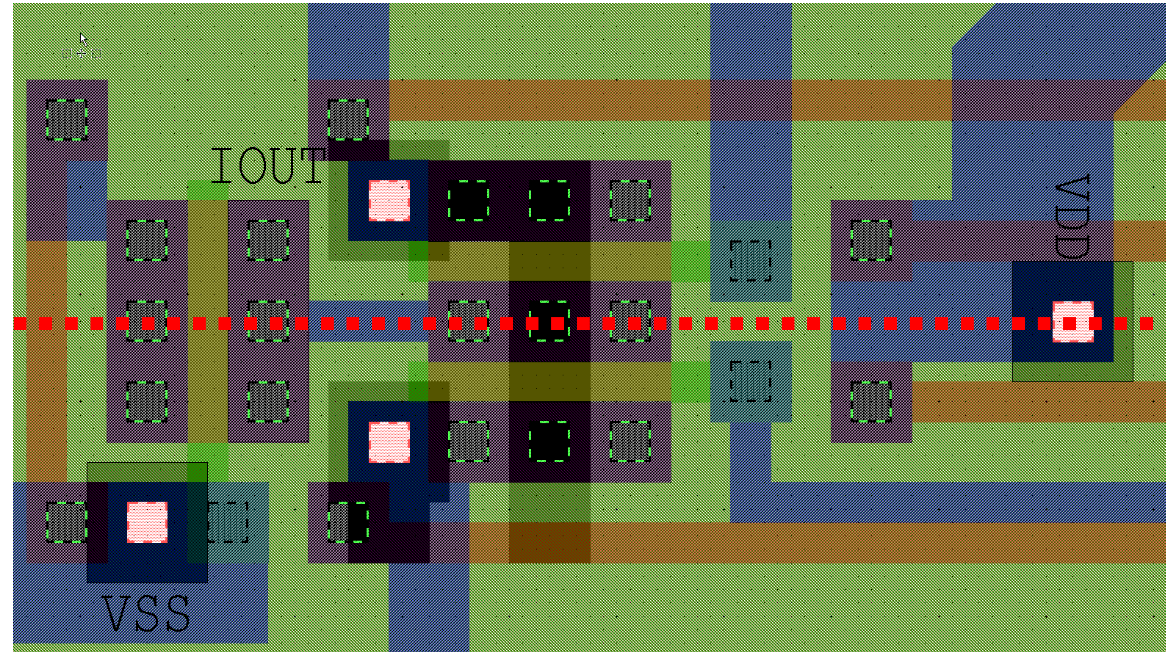
- Ti/Ni mask use to define resistors and channels.





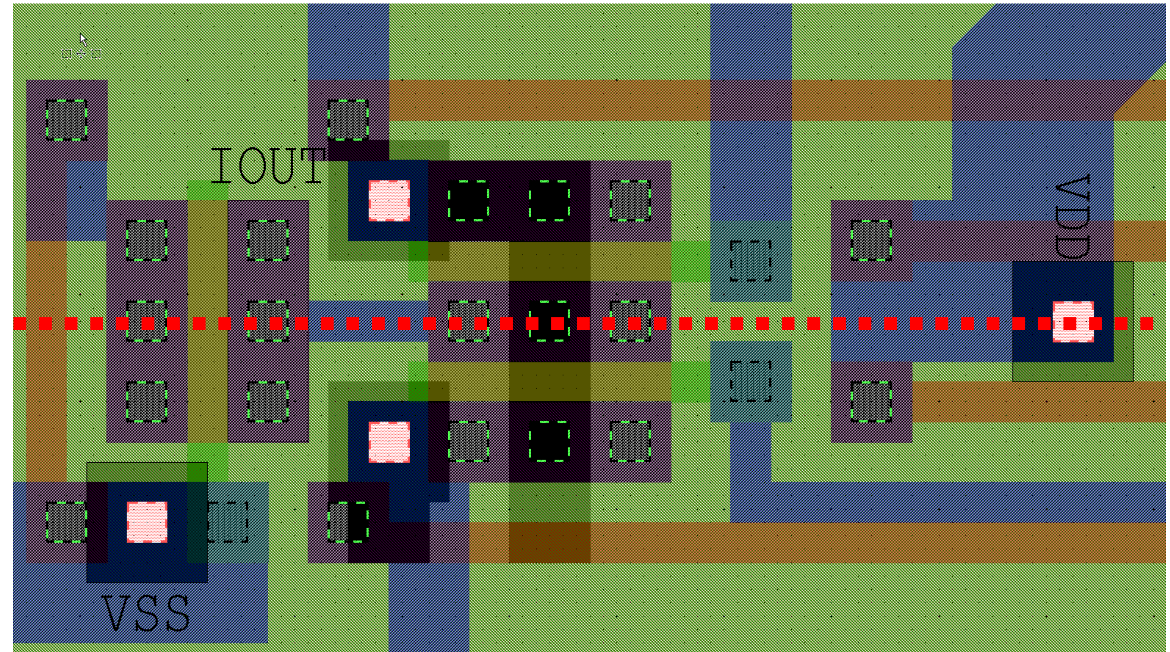
Process with two levels of metal interconnect

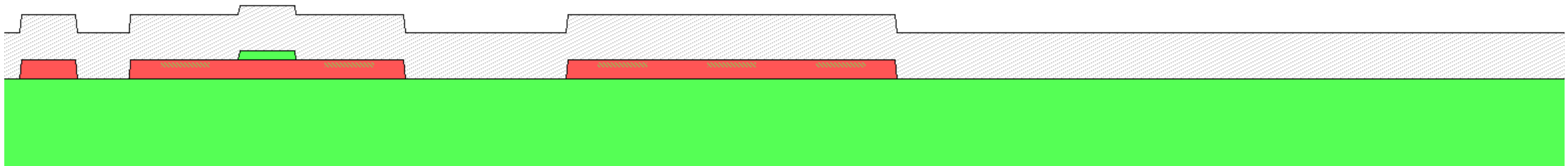
- Si mask was used for box implant of 1.6 x 10^{15} cm^{-2} while heated to 873 K.
- Capped and annealed at 1633 K for 4 hours in N_2.



Process with two levels of metal interconnect

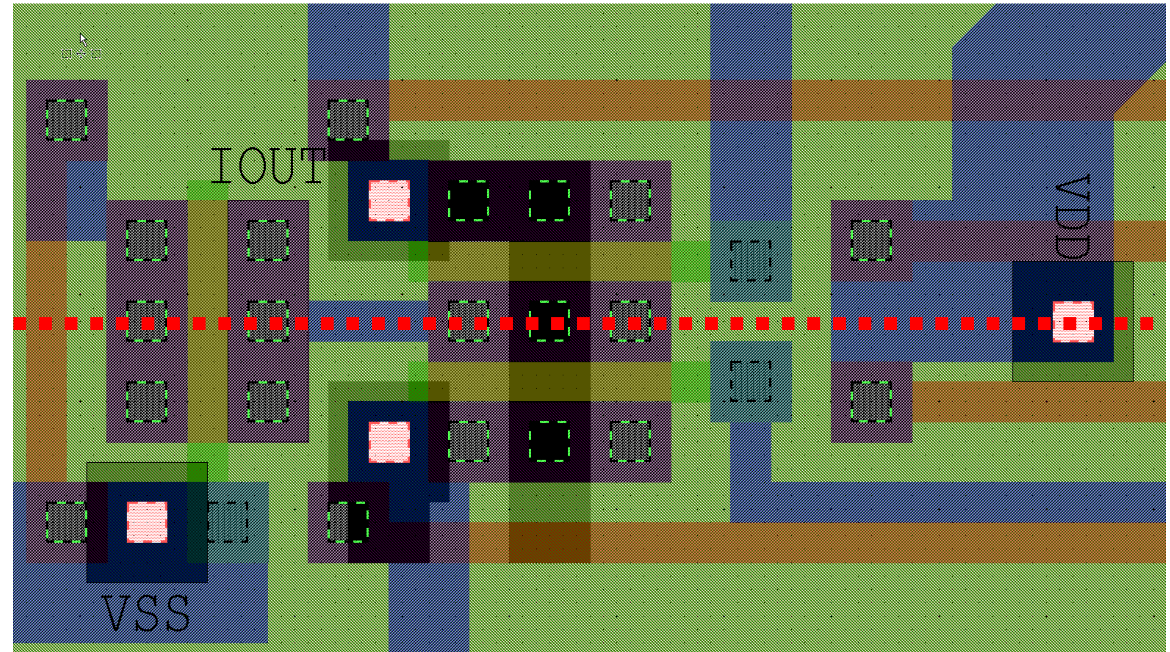
- Thermal and deposited oxide.

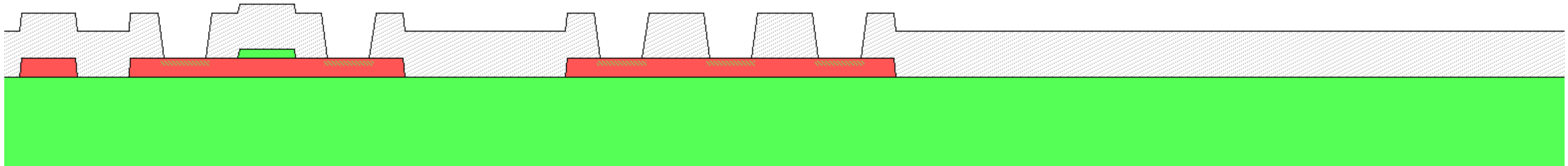




Process with two levels of metal interconnect

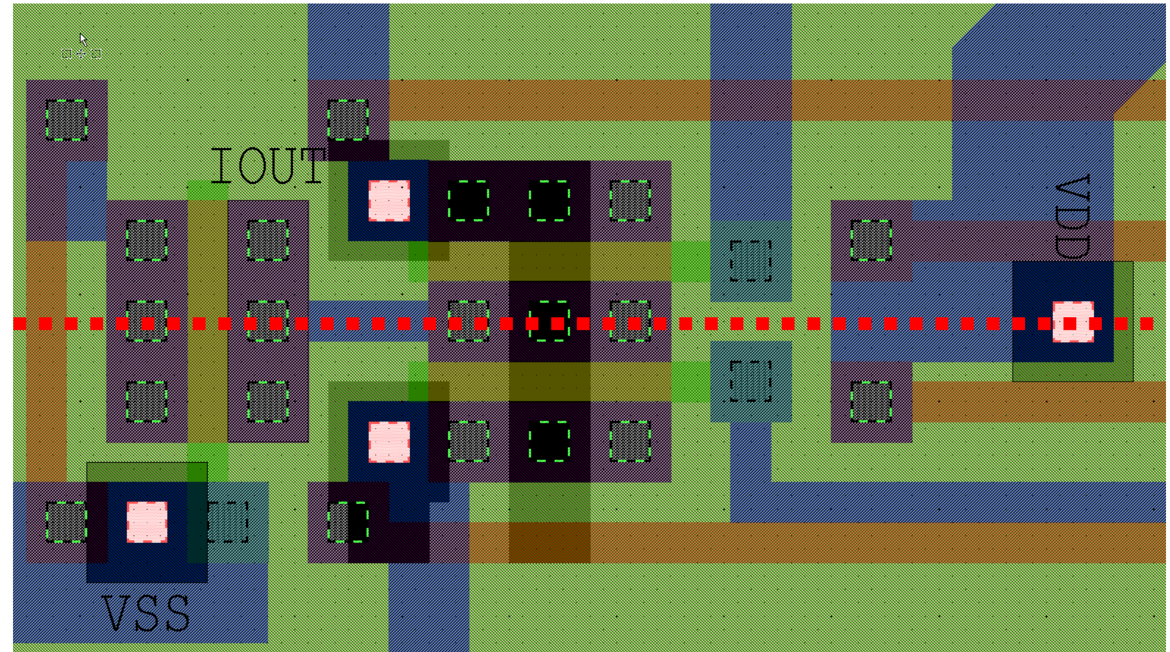
- Dry and wet etch of via 1.

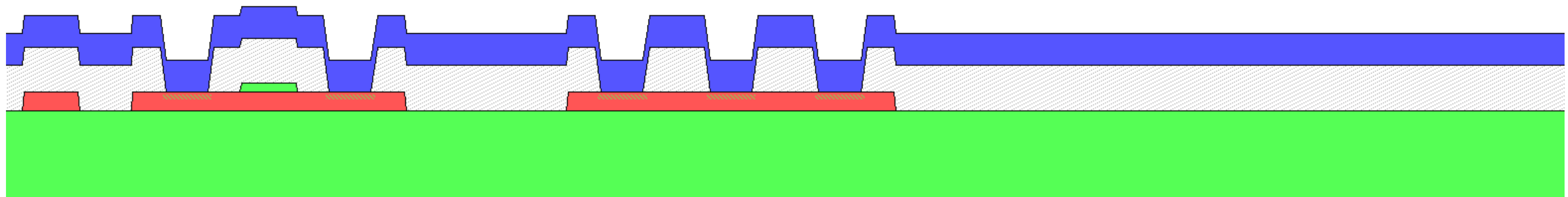




Process with two levels of metal interconnect

- Bake out and sputter deposition of metal 1.





Process with two levels of metal interconnect

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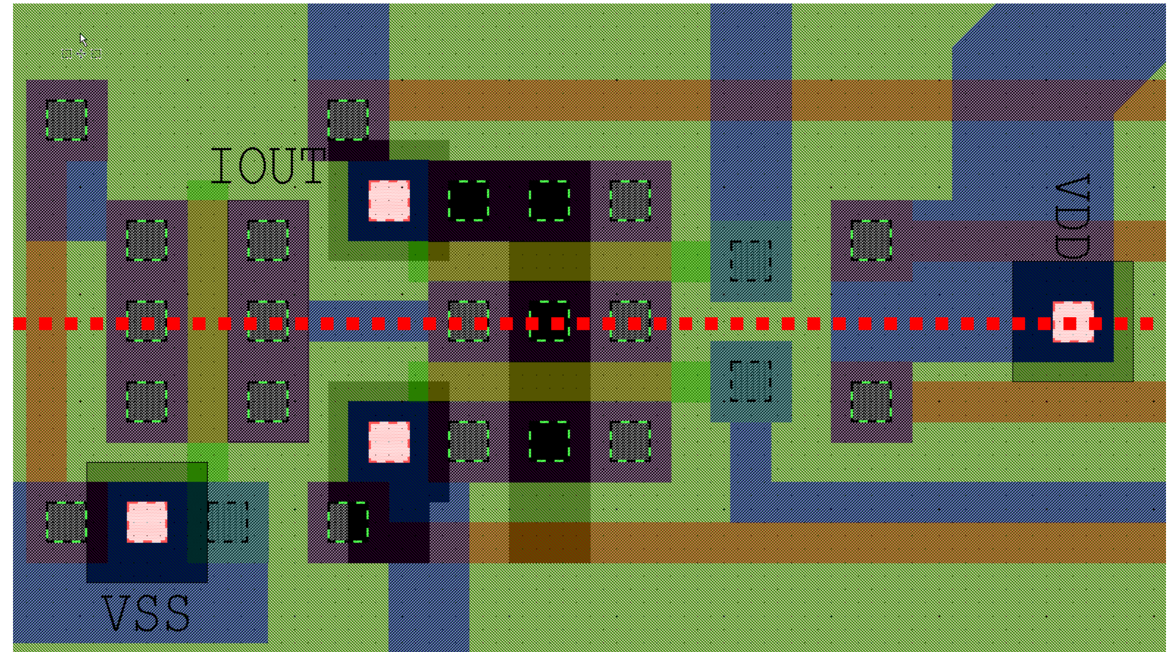
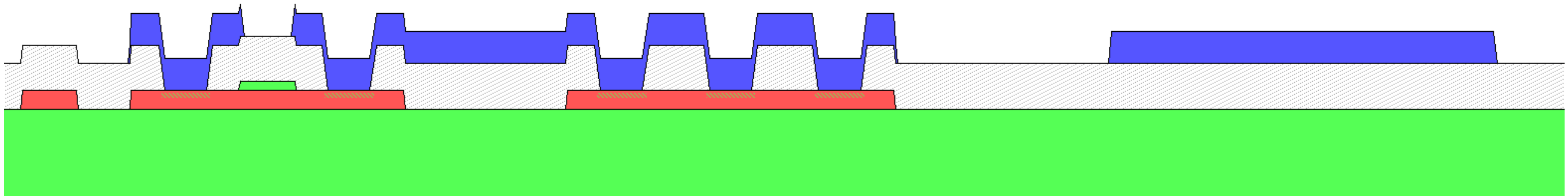
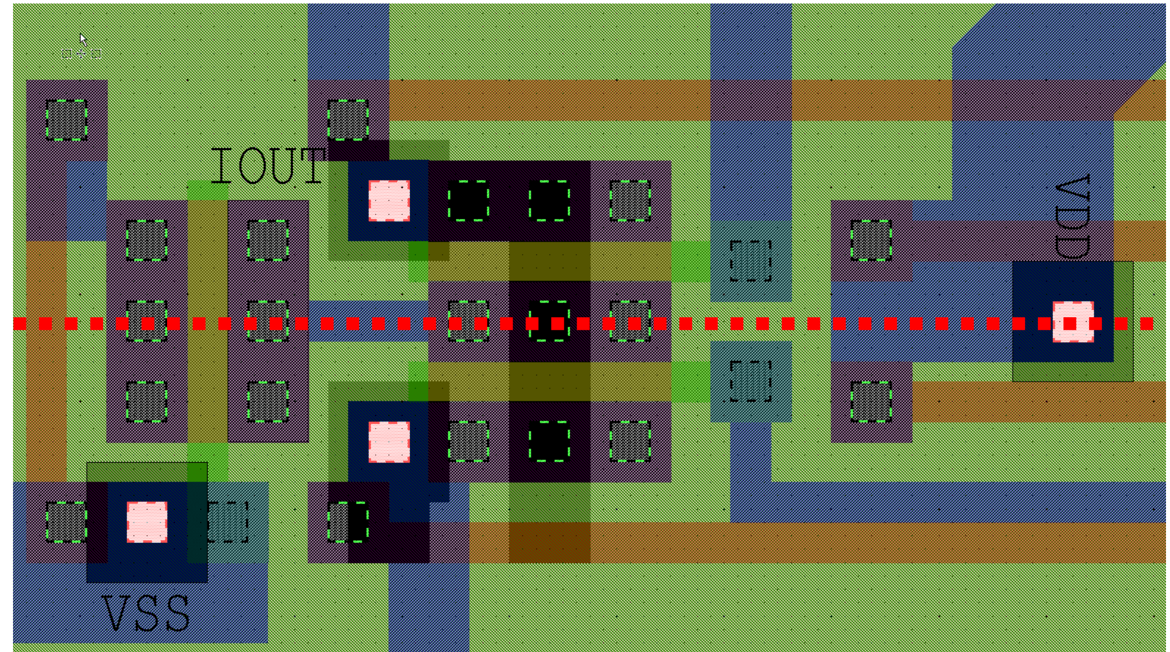
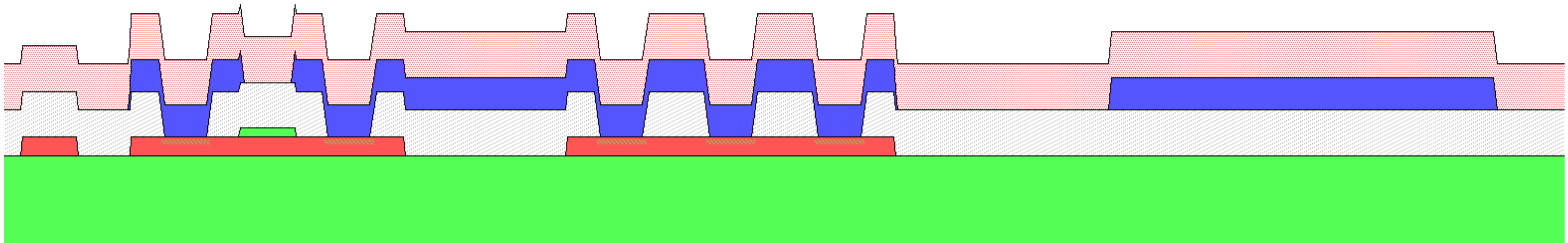




Process with two levels of metal interconnect

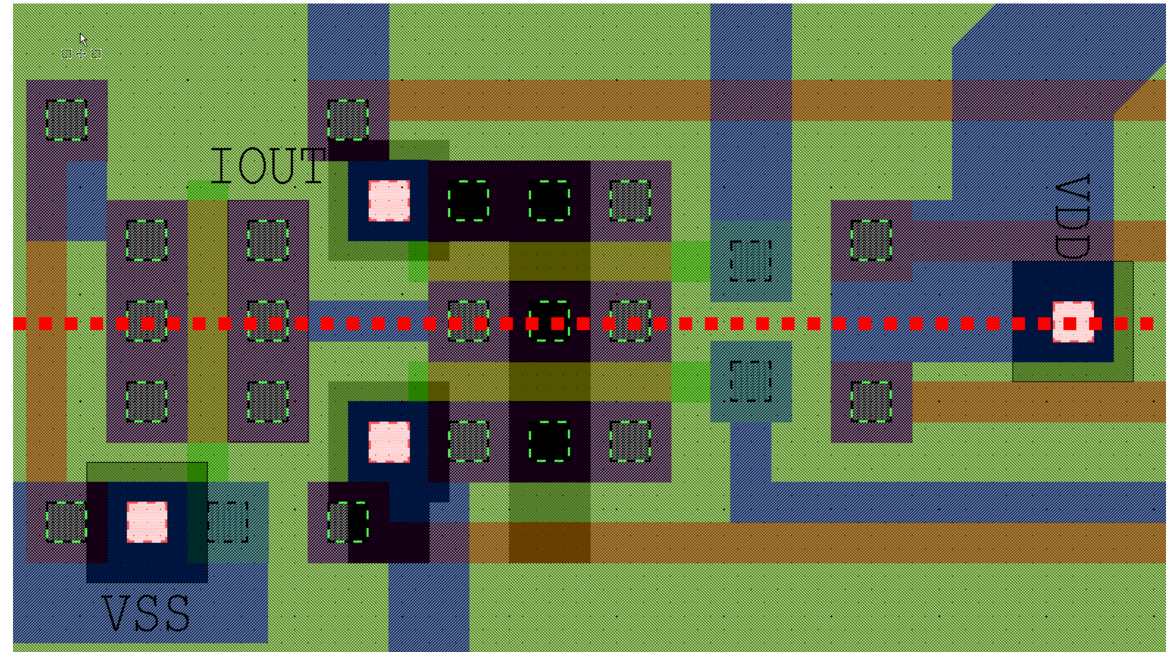
- Deposited oxide 2.

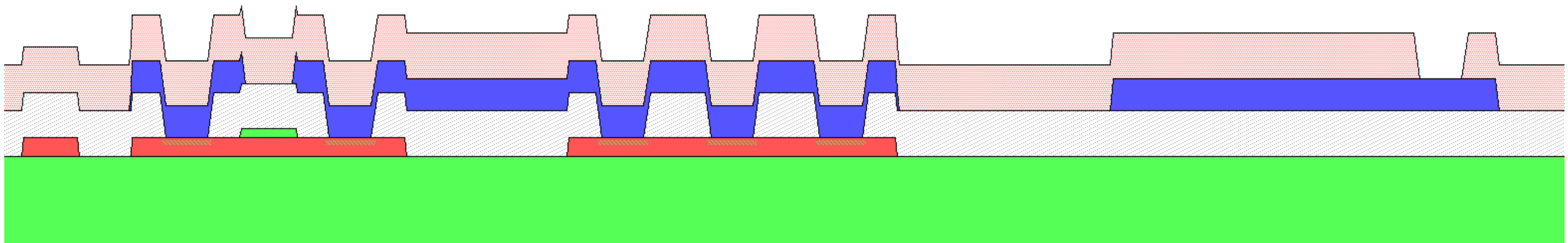




Process with two levels of metal interconnect

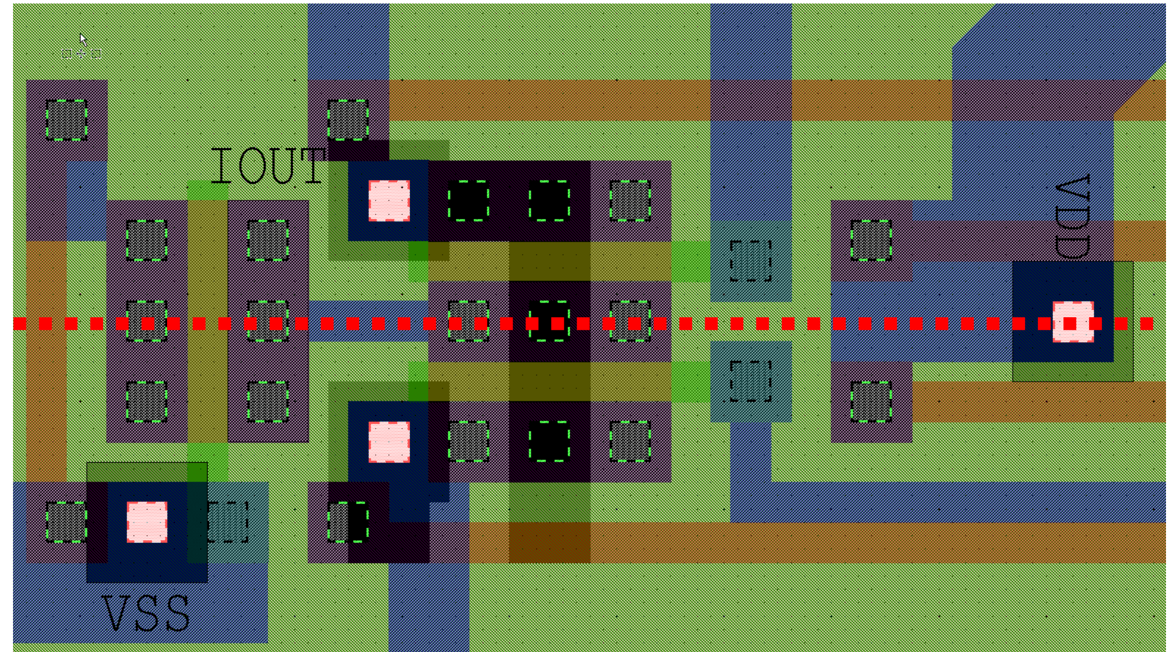
- Dry etch of via 2.

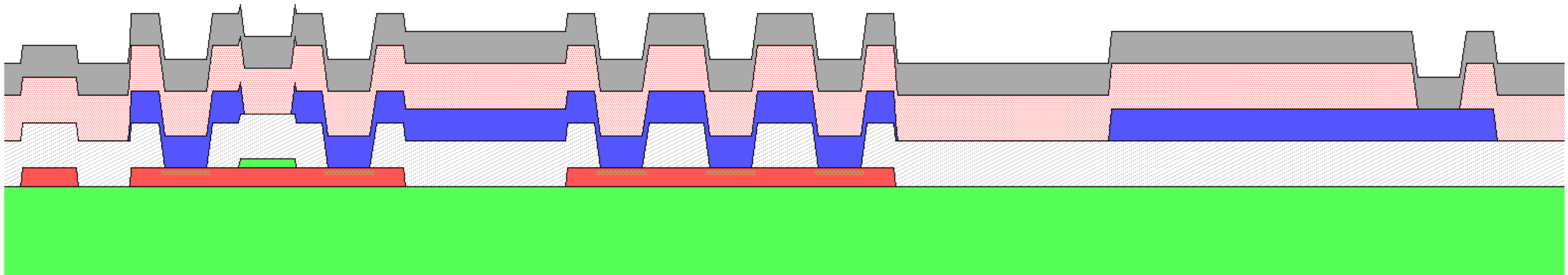




Process with two levels of metal interconnect

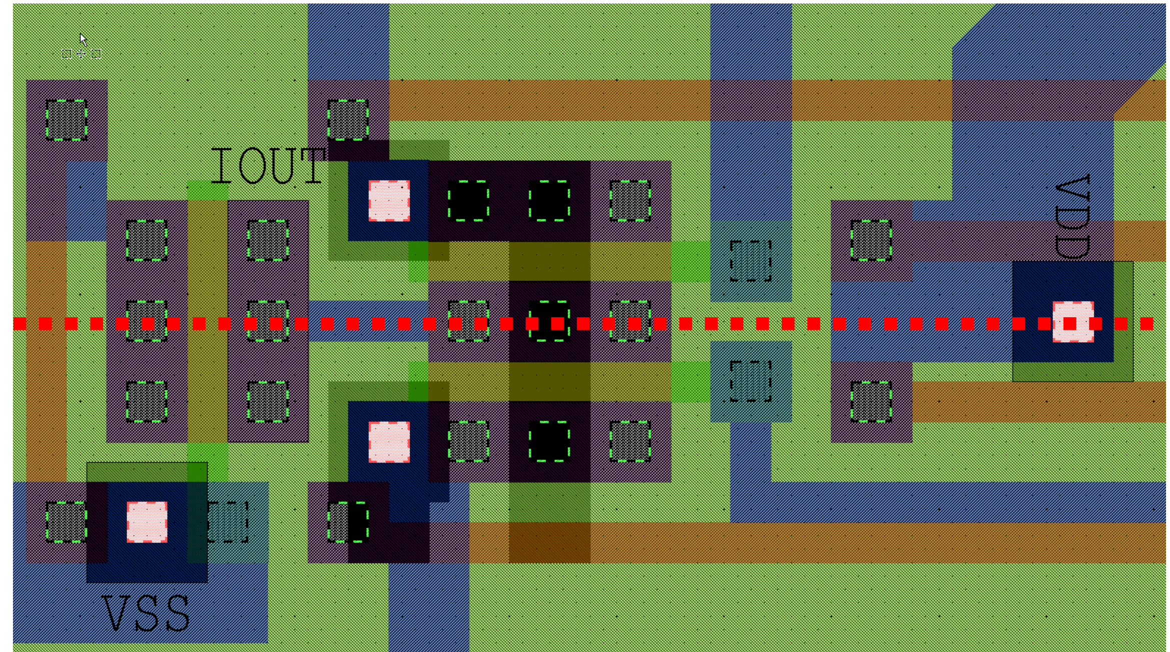
- Bake out and sputter deposit of metal 2.

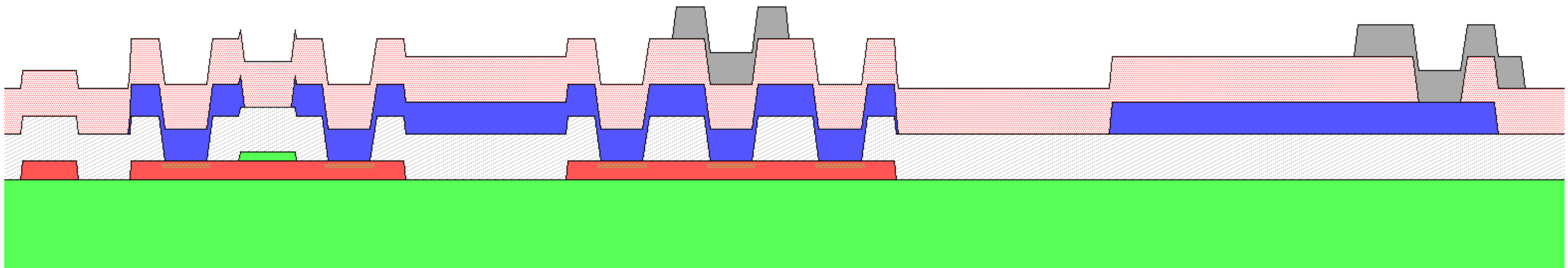




Process with two levels of metal interconnect

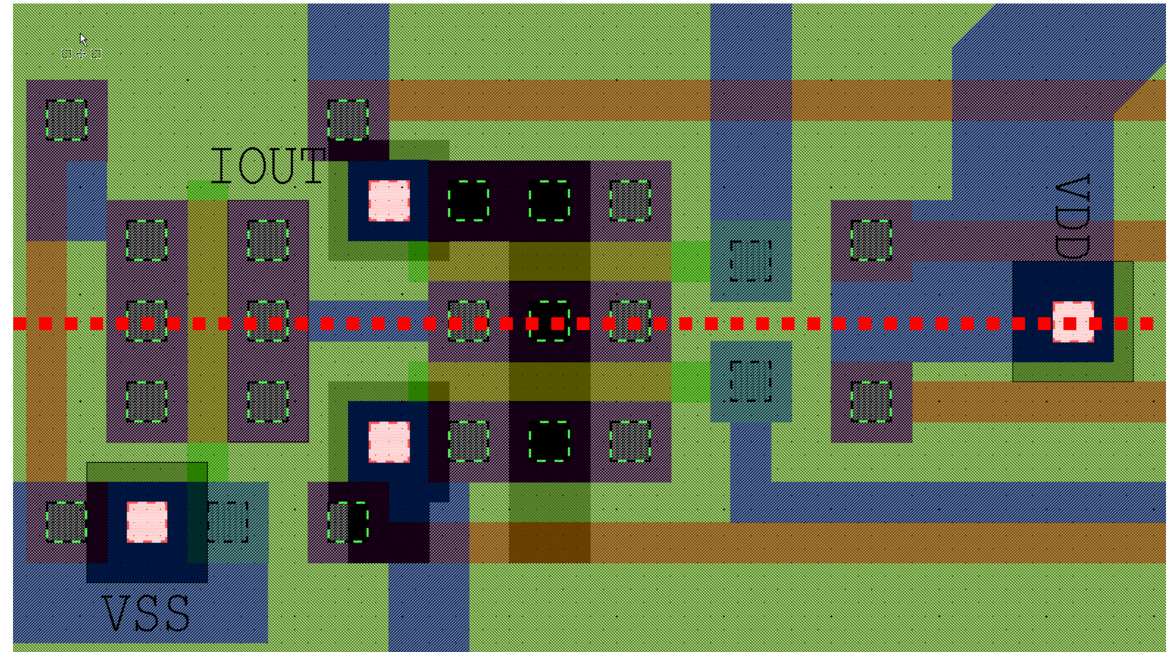
- Dry etch metal 2.

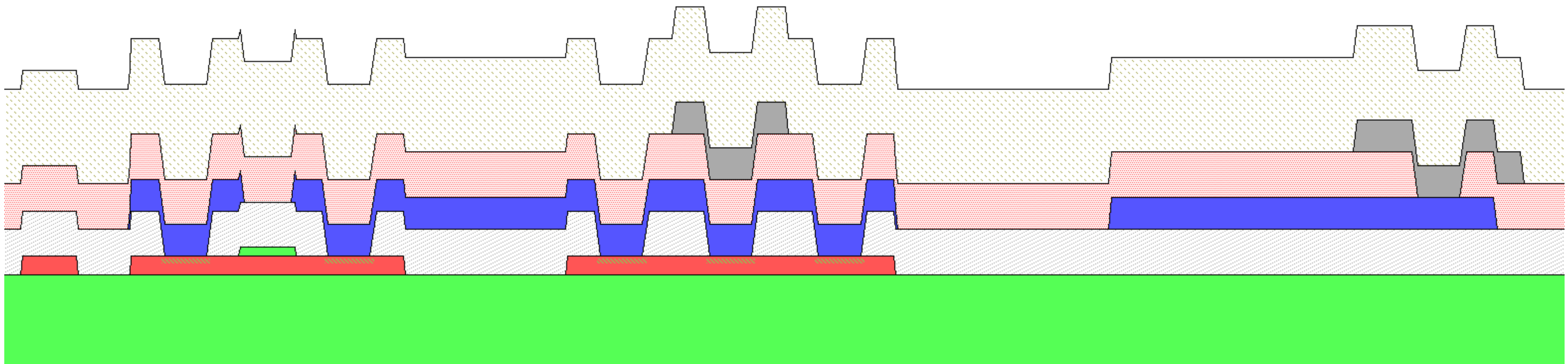




Process with two levels of metal interconnect

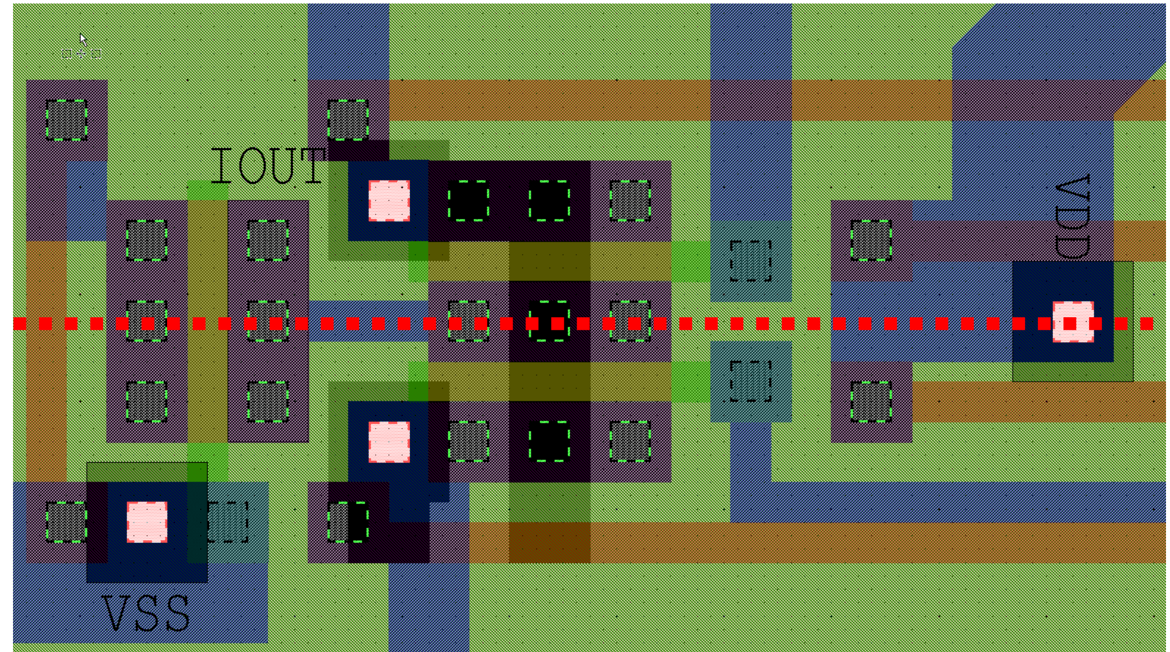
- Deposit oxide 3.
- Dry and wet etch of via 3 (not shown and only used for bond pads).

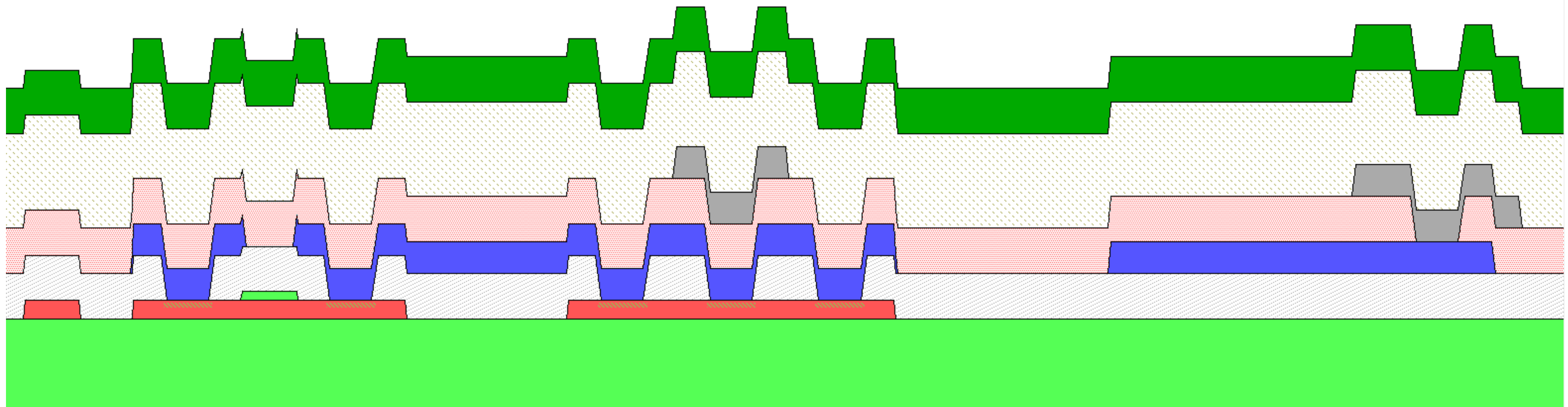




Process with two levels of metal interconnect

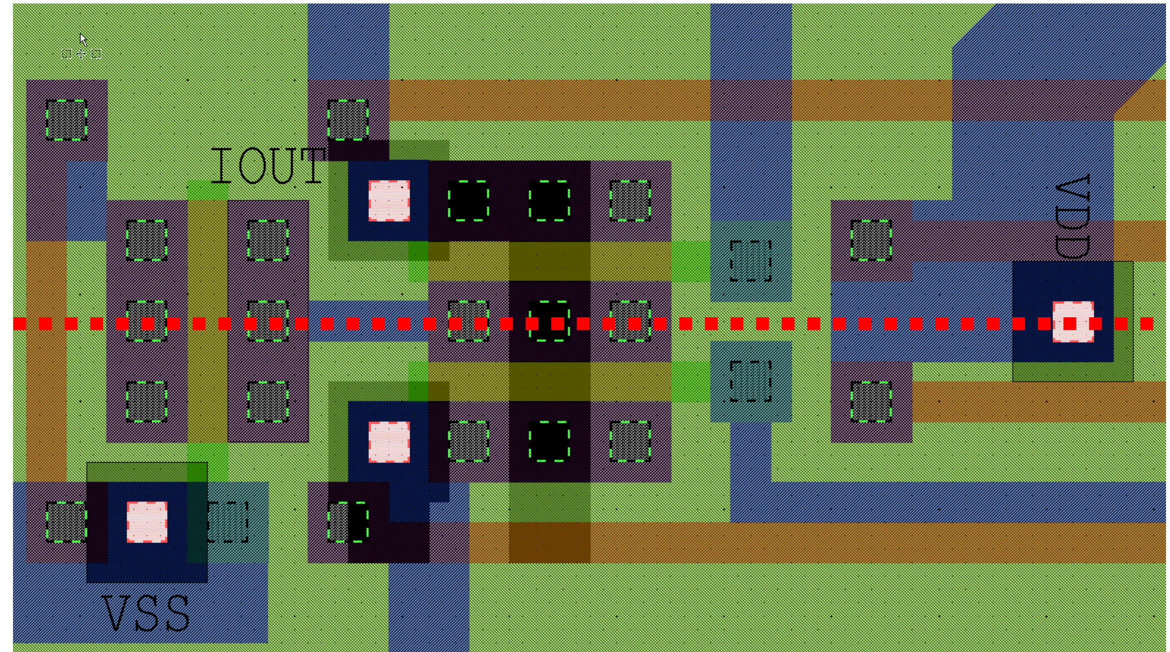
- Bake out and deposit of metal 3

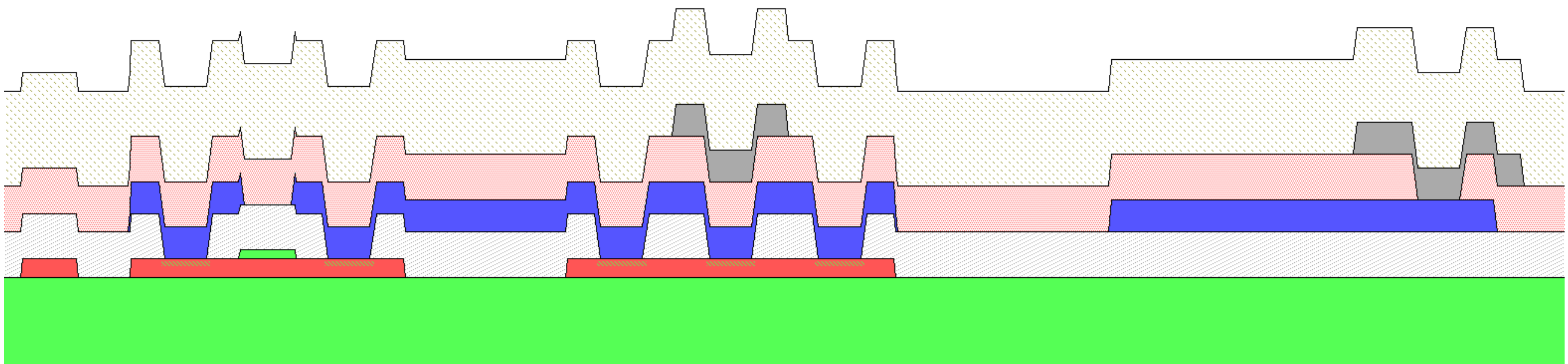


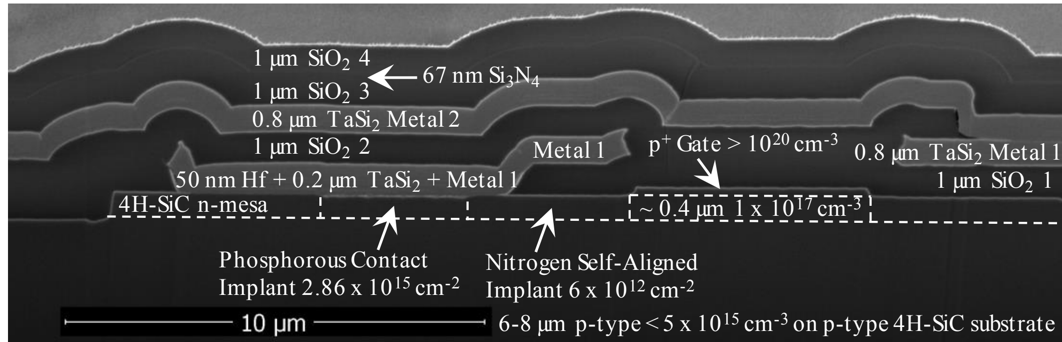


Process with two levels of metal interconnect

- Dry etch of metal 3.







1 µm SiO_2 4
67 nm Si_3N_4
1 µm SiO_2 3
0.8 µm $TaSi_2$ Metal 2
1 µm SiO_2 2
Metal 1
p^+ Gate > 10^{20} cm^{-3}
0.8 µm $TaSi_2$ Metal 1
1 µm SiO_2 1
50 nm Hf + 0.2 µm $TaSi_2$ + Metal 1
4H-SiC n-mesa
~ 0.4 µm 1 x 10^{17} cm^{-3}
Phosphorous Contact
Implant 2.86 x 10^{15} cm^{-2}
Nitrogen Self-Aligned
Implant 6 x 10^{12} cm^{-2}
10 µm
6-8 µm p-type < 5 x 10^{15} cm^{-3} on p-type 4H-SiC substrate