Total Ionizing Dose Test Report for the MB85AS4MT ReRAM

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I. Introduction

The purpose of this test is to determine the total-ionizing dose (TID) susceptibility of the MB85AS4MT Resistive Random Access Memory (ReRAM) manufactured by Fujitsu Semiconductor.

II. Device UnderTest

The MB85AS4MT is a 4 Mbit ReRAM with Serial Peripheral Interface (SPI). The maximum operating frequency is 5 MHz. The memory array is based on ReRAM technology, while the peripheral circuits are built on a standard complementary metal oxide semiconductor (CMOS) process.

Table I shows the device specifications for some common parameters. Figure 1 shows a schematic diagram of the pin configuration. Table II describes the function of each pin. Figure 2 shows a schematic block diagram of the internal elements. Other device parameters and functional descriptions can be found in the datasheet [1]. Table III shows additional part and test information.

Table I
Device specification.

Parameter	Specification
Supply Voltage V_{cc}	1.65 to 3.6 V
Read supply current	0.2 mA (typical)
Rewrite supply current	1.3 mA (typical)
Standby current	10 µA (typical) 45 µA (maximum)
Sleep current	2 µA (typical)
Operation temperature range	-40°C to 85°C
Endurance	1.2×10^6 per byte
Retention	10 years at 85°C

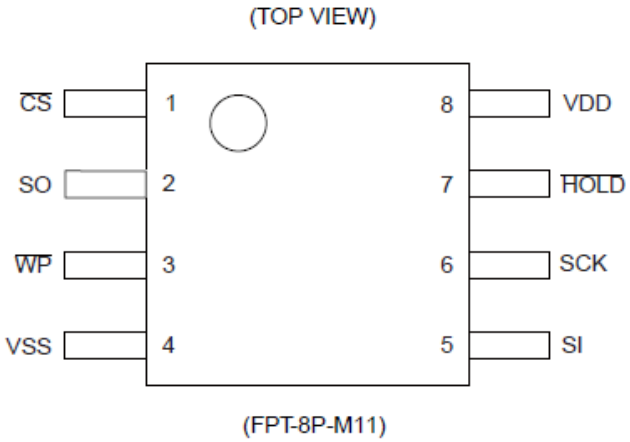

Figure 1. Pin configuration for the RM24C64.

Table II
Pin/signal description.

Pin No.	Pin Name	Functional description
1	$\overline{CS}$	Chip Select pin This is an input pin to make chips select. When $\overline{CS}$ is "H" level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When $\overline{CS}$ is "L" level, device is in select (active) status. $\overline{CS}$ has to be "L" level before inputting op-code.
3	$\overline{WP}$	Write Protect pin This is a pin to control writing to a status register. The writing of status register (see "■ STATUS REGISTER") is protected in related with $\overline{WP}$ and WPEN. See "■ WRITING PROTECT" for detail.
7	$\overline{HOLD}$	Hold pin This pin is used to interrupt serial input/output without making chips deselect. When $\overline{HOLD}$ is "L" level, hold operation is activated, SO becomes High-Z, SCK and SI become do not care. While the hold operation, $\overline{CS}$ has to be retained "L" level.
6	SCK	Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge.
5	SI	Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data.
2	SO	Serial Data Output pin This is an output pin of serial data. Reading data of ReRAM memory cell array and status register data are output. This is High-Z during standby.
8	VDD	Supply Voltage pin
4	VSS	Ground pin

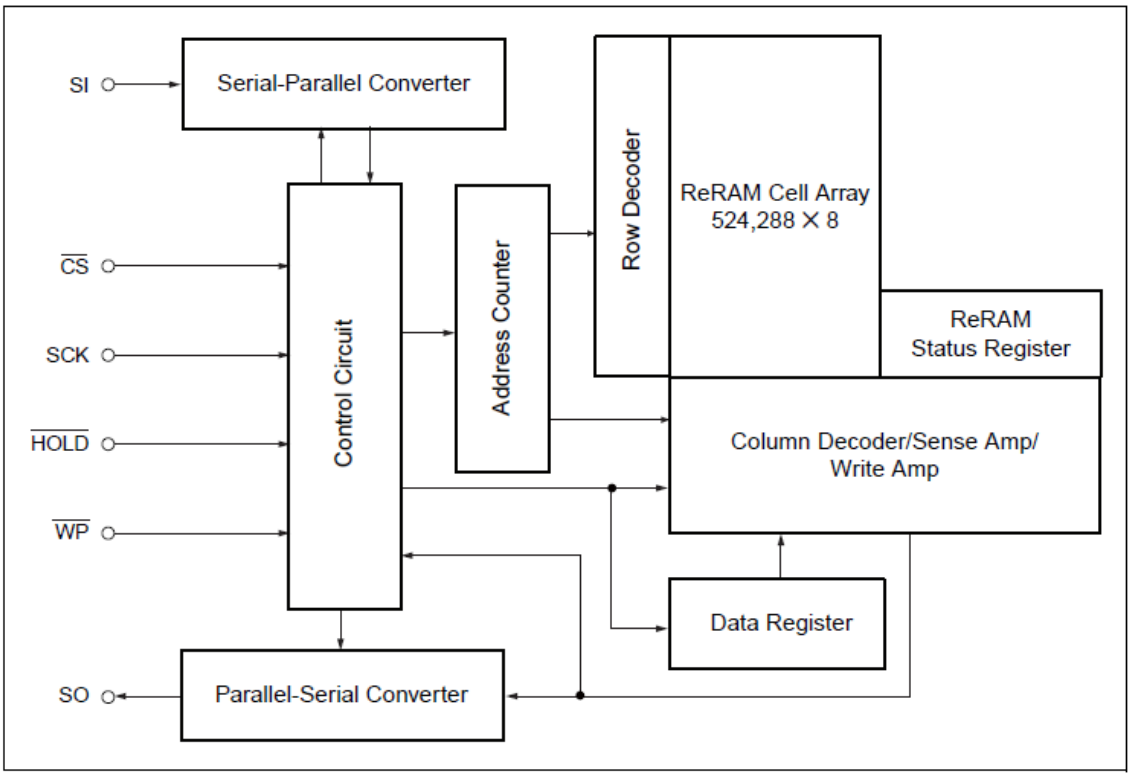

Figure 2. Schematic block diagram.

Table III
Part and test information.

Generic Part Number:	MB85AS4MT
Manufacturer:	Fujitsu
Lot Date Code (LDC):	1638
Quantity Tested:	10 + 2 controls
Part Function:	Random Access Memory
Part Technology:	ReRAM and CMOS
Package Style:	8-pin Small Outline Integrated Circuit (SOIC)
Test Equipment:	Microcontroller tester Power supply

III. Test Method

A. Irradiation Procedure

The irradiation procedures and dosimetry requirements conformed to MIL-STD-883-H Test Method 1019 [2]. The irradiation was carried out in a room air source gamma ray facility. Active dosimetry was performed using air ionization probes. The device-under-test (DUT) was placed inside a standard Pb/Al filter box.

B. Test setup and procedure

The DUTs were soldered onto printed circuit boards (PCB), which were then connected to the microcontroller tester. Figure 3 shows a photograph of the test setup. The DUTs were biased in standby mode during irradiation. All test samples were programmed to checkerboard AA pattern prior to irradiation. Five parts were read-only at each dose step. Another set of five parts were exercised with read/write operations and reprogramed to different patterns at each dose step. Procedure for the exercised parts are as follows:

1. Verify AA
2. Program to 55
3. Verify 55
4. Program to 00
5. Verify 00
6. Program to FF
7. Verify FF
8. Program to AA
9. Verify AA

The planned TID steps were 10, 20, 50, 100, 200, 500, 1000 krad(Si) or until functional failure. The parts were annealed for 1 week under the same bias configuration as the irradiation bias mode following the final dose step.

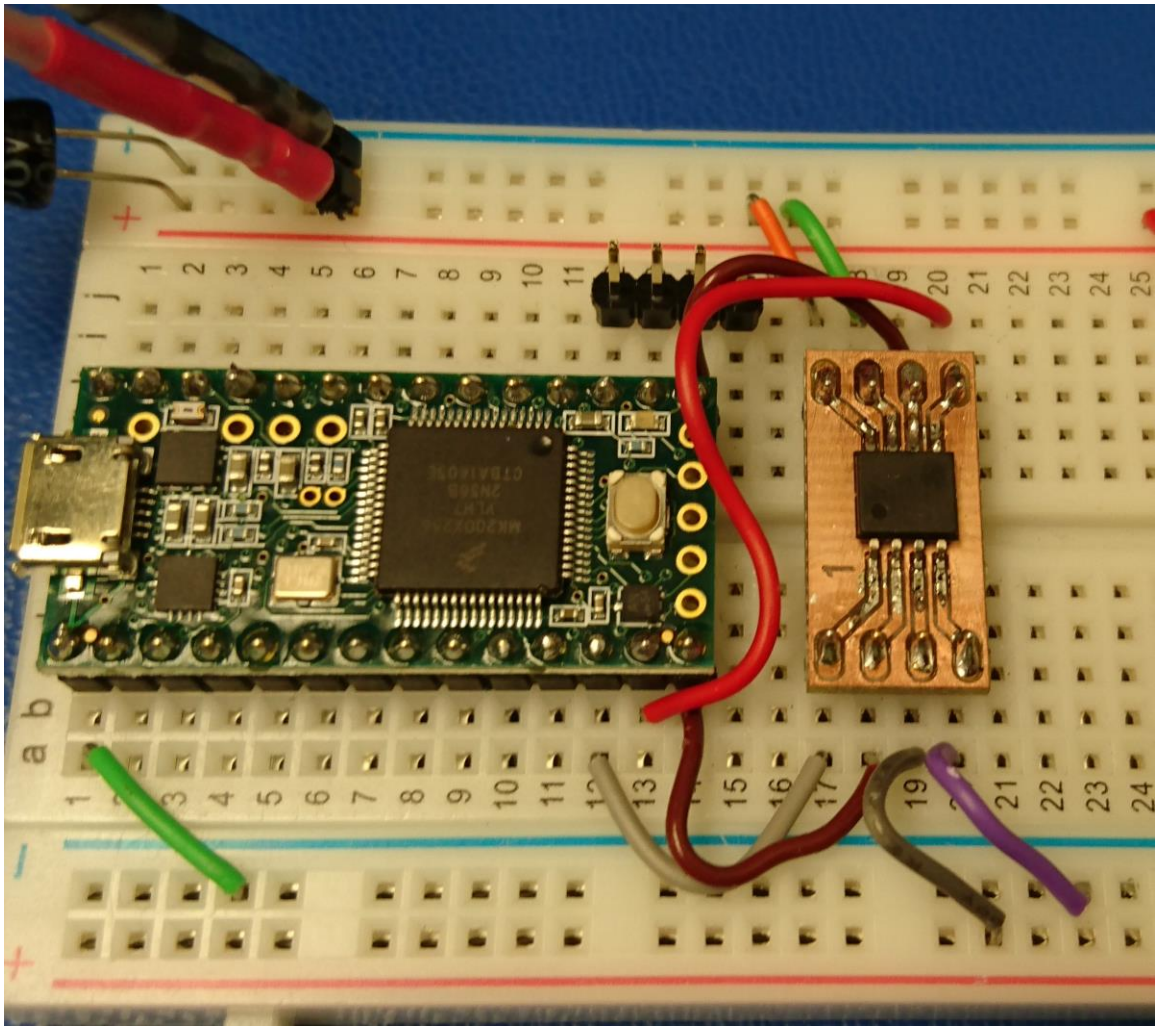

Figure 3. Photograph of the measurement setup showing the Teensy 3.2 microcontroller tester on the left and the MB85AS4MT ReRAM on the right.

C. Test Conditions

Test Temperature: Ambient temperature
Power Supply: 3.3 V
Parameters: 1) Supply voltage
2) Supply current
3) Address and byte information

IV. Results

The parts showed functional failure between 20 to 50 krad(Si). The functional failures are characterized by loss of communication. There was no error from the memory array prior to the functional failure. So the ReRAM cells are relatively robust at these TID levels, while the CMOS control circuits are more sensitive.

Figure 4 shows the highest surviving TID and the failing TID levels for the two sets of test samples. In general, the read-only samples showed a higher surviving dose than the samples that were read/write cycled. 4 out of 5 read-only samples remained functional up to 50 krad(Si). The samples that were read/write cycled showed a wider spread in the surviving TID level, with 3 out of 5 samples functional up to 20 krad(Si) and 1 sample functional up to 75 krad(Si).

Figure 5 shows the average standby current in milliamps as a function of TID for samples that were read-only and read/write cycled. The error bars indicate part-to-part variability. In general, the test samples that were read/write cycled in between dose steps showed higher standby current than the read-only samples.

Figure 6 shows the standby current characteristics for all samples, including the annealed data after 168 hour of bias annealing. Note that functional failure can occur even if the standby current is below the specification limit of 45 µA. However, all failures occurred as the standby current increased beyond the nominal level of ~10 µA. Only 2 parts recovered functionality, even though 4 parts annealed to within the specification range for the standby current. The raw data file can be accessed from the Appendix.

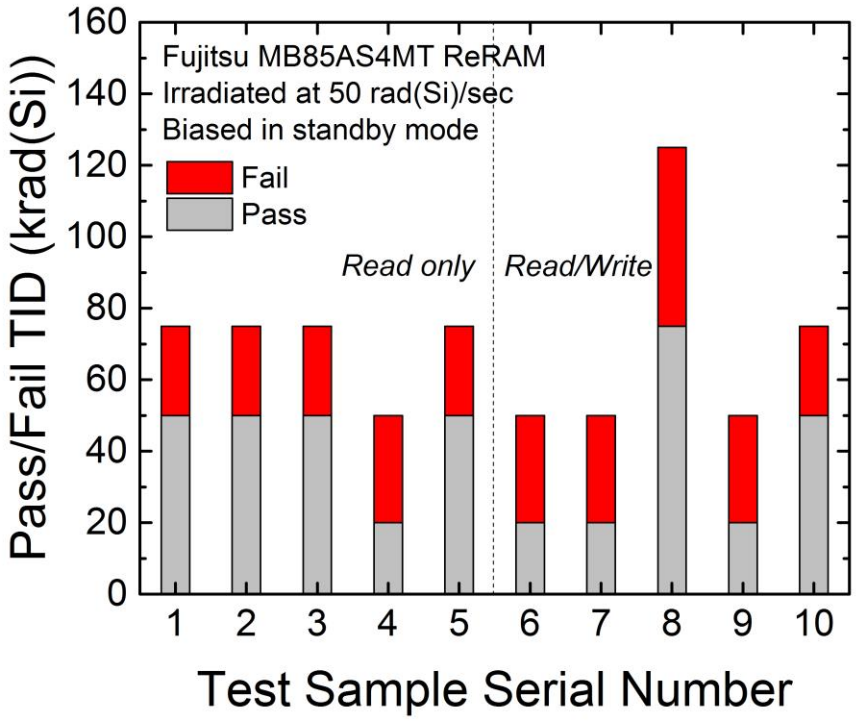

Figure 4. Pass/fail TID level for all test samples. Each stacked column bar indicate the highest passing TID and the subsequent dose step where the part was characterized and failed.

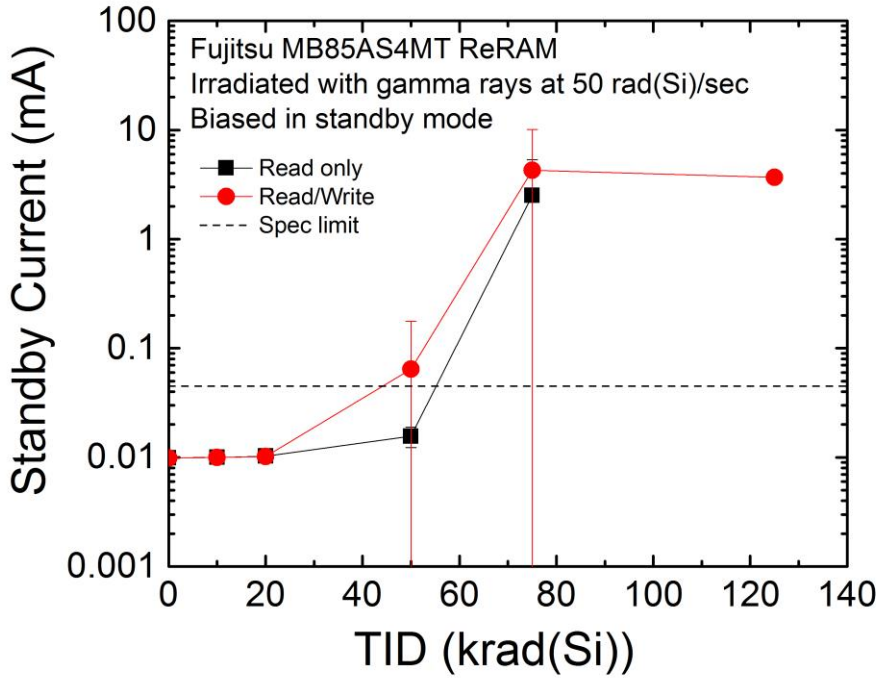

Figure 5. Average standby current as a function of TID for the Fujitsu MB85AS4MT ReRAM irradiated with gamma rays at 50 rad(Si)/sec biased under standby mode.

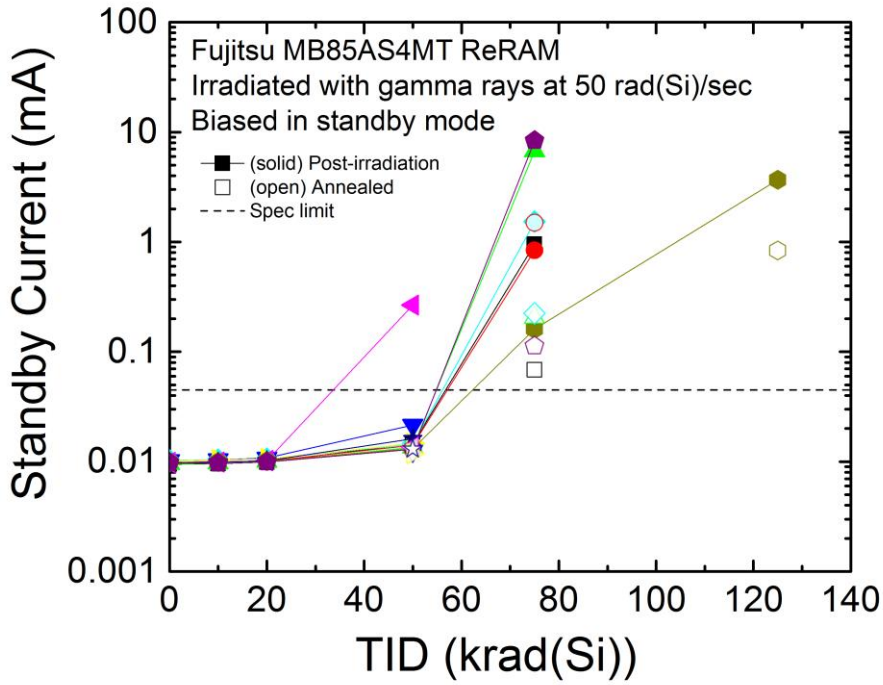

Figure 6. Standby current as a function of TID for the Fujitsu MB85AS4MT ReRAM irradiated with gamma rays at 50 rad(Si)/sec biased under standby mode. Parts were bias annealed for 168 hours following irradiation.

V. Reference

[1] Fujitsu Semiconductor, “Memory ReRAM: 4M (512K × 8) Bit SPI MB85AS4MT” MB85AS4MT datasheet, Dec. 2016.
[2] MIL-STD-883-H, Test Method 1019.8, Ionizing Radiation (Total Dose) Test Procedure Feb. 26, 2010.

Appendix

Summary of Device Performance

DUT	Type of Test	Last Passed (krad (Si))	Failed (krad(Si))	Type of Failure
1	Read Only	50	75	Cannot communicate
2	Read Only	50	75	Cannot communicate
3	Read Only	50	75	Cannot communicate
4	Read Only	**20**	50	Cannot communicate
5	Read Only	50	75	Cannot communicate
6	R/W	**20**	50	Cannot communicate. Intermittent operation -- occasionally able to read and write multiple data patterns cleanly, usually unresponsive to any command.
7	R/W	**20**	50	First 256 bytes seemed unusable. Rest of mem R/W ok. Comm is ok. Came back after testing other parts and now couldn't comm at all.
8	R/W	75	125	Cannot communicate
9	R/W	**20**	50	First 256 bytes seem unusable. Rest of mem R/W ok. Comm is ok.
10	R/W	50	75	Cannot communicate
C11	Read Only			None
C12	R/W			None

After annealing for 168 hours under bias, DUTs 4 and 6 (each saw only 50 krad(Si)) were operating normally. Remainder of parts still failed, including DUTs 7 & 9 which also only got 50 krad(Si).

Accumulated Dose (rad)	DUT_1	DUT_2	DUT_3	DUT_4	DUT_5	DUT_6	DUT_7	DUT_8	DUT_9	DUT_10	DUT_C11	DUT_C12	MAX
0	0.0095	0.0099	0.0096	0.0102	0.0103	0.0098	0.0101	0.0099	0.0097	0.0098	0.0100	0.0101	0.045
10000	0.0096	0.0100	0.0097	0.0104	0.0104	0.0099	0.0104	0.0099	0.0099	0.0097	0.0099	0.0101	0.045
20000	0.0099	0.0101	0.0100	0.0108	0.0106	0.0102	0.0106	0.0101	0.0102	0.0099	0.0099	0.0101	0.045
50000	0.0146	0.0141	0.0135	0.0215	0.0144	0.2660	0.0147	0.0131	0.0162	0.0130	0.0100	0.0101	0.045
75000	0.9540	0.8390	6.7400		1.5300			0.1610		8.3900	0.0099	0.0101	0.045
125000								3.6700			0.0100	0.0102	0.045
125000	0.0688	1.4990	0.2050	0.0125	0.2240	0.0136	0.0118	0.8370	0.0130	0.1130	0.0100	0.0102	0.045 *

*this is after anneal

Raw Data Logs:

0krad					
	WRITE	READ	STBY	VERIFY	TIDRWCYCLE
DUT1	1.27	0.267	0.0095	ok	
DUT2	1.28	0.275	0.0099	ok	
DUT3	1.23	0.272	0.0096	ok	
DUT4	1.22	0.266	0.0102	ok	
DUT5	1.26	0.273	0.0103	ok	
DUT6	1.24	0.275	0.0098		ok
DUT7	1.27	0.272	0.0101		ok
DUT8	1.24	0.274	0.0099		ok
DUT9	1.25	0.271	0.0097		ok
DUT10	1.27	0.274	0.0098		ok
DUT11	1.26	0.276	0.01	ok	
DUT12	1.25	0.274	0.0101		ok

10krad				
WRITE	READ	STBY	VERIFY	TIDRWCYCLE
	0.27	0.0096	ok	
	0.276	0.01	ok	
	0.273	0.0097	ok	
	0.278	0.0104	ok	
	0.276	0.0104	ok	
1.34	0.277	0.0099		ok
1.3	0.274	0.0104		ok
1.31	0.275	0.0099		ok
1.32	0.273	0.0099		ok
1.31	0.269	0.0097		ok
	0.275	0.0099	ok	
1.22	0.274	0.0101		ok

20krad				
WRITE	READ	STBY	VERIFY	TIDRWCYCLE
	0.271	0.0099	ok	
	0.277	0.0101	ok	
	0.275	0.01	ok	
	0.28	0.0108	ok	
	0.277	0.0106	ok	
1.37	0.279	0.0102		ok
1.36	0.275	0.0106		ok
1.37	0.277	0.0101		ok
1.35	0.274	0.0102		ok
1.38	0.276	0.0099		ok
	0.2755	0.0099	ok	
1.22	0.274	0.0101		ok

50krad						
	WRITE	READ	STBY	VERIFY	TIDRWCYCLE	
DUT1		0.29	0.0146	ok		
DUT2		0.298	0.0141	ok		
DUT3		0.293	0.0135	ok		
DUT4		0.0358	0.0215	FAILED		entire memory zero'd out. Note that read current probably unreliable due to lower duty cycle (time spent shooting out error msgs). Part appears properly seated in correct socket
DUT5		0.29	0.0144	ok		
DUT6		0.0863	0.266		FAILED	Verified part seated correctly. All zeros on initial readback.
DUT7	1.66	0.291	0.0147		FAILED	Looks like a single block is stuck at all AA?
DUT8	1.54	0.3	0.0131		ok	Ran cycle twice and worked great
DUT9	1.57	0.242	0.0162		FAILED	Initial AA's verified ok but rewrite failed to rewrite the first block
DUT10	1.62	0.291	0.013		ok	worked fine
DUT11		0.275	0.01	ok		
DUT12	1.22	0.273	0.0101		ok	
DUT4_rep		0.299	0.0158	NOW OK		re-tried after testing #5, and now it's fine? Did NOT re-write memory.
DUT6_rep	1.59	0.306	0.0206		FAILED THEN (	total re-cycle of power to everything, brought tester back up and wrote AA to memory (but it happened fast). Then reads failed on TIDRWCYCLE (all FF). When it tried to program a 55 it readback ok. 00 ok. FF ok. AA ok. Seated part again, now I can't even read device ID.
DUT7_rep	1.61		0.0181		FAILED	Looked like it was going to work when I wrote 0 and verified all 0, but the TIDRW cycle failed again. Note it doesn't always fail in the same way -- sometimes only part of memory is stuck. After finishing everything came back and started over again with this part and couldn't even read device ID, tried 2Mhz clock instead of 5 and nothing changed.
DUT9_repeated						This wasn't logged, but tried going back to device 9 again and I could get device ID, but same issue with not re-writing block 1, even at 2MHz SPI clock
DUT4_yet again					FAILED	Went back again and dead again. Both control are GOOD.

75krad						
	WRITE	READ	STBY	VERIFY	TIDRWCYCLE	
DUT1		1.059	0.954	FAILED		Cannot read ID or data
DUT2			0.839	FAILED		Cannot read ID or data
DUT3		6.86	6.74	FAILED		Cannot read ID or data
DUT4						
DUT5		1.63	1.53	FAILED		Cannot read ID or data
DUT6						
DUT7						
DUT8	1.24		0.161		ok	Works great!
DUT9						
DUT10		8.53	8.39		FAILED	Cannot read ID or data
DUT11		0.274	0.0099	ok		Read at 2Mhz (which made current look low), then repeated at 5Mhz for consistency with previous mx
DUT12	1.22	0.272	0.0101		ok	Normal

125krad						
	WRITE	READ	STBY	VERIFY	TIDRWCYCLE	
DUT1						
DUT2						
DUT3						
DUT4						
DUT5						
DUT6						
DUT7						
DUT8		3.25	3.67		FAILED	Cannot read ID or data
DUT9						
DUT10						
DUT11		0.275	0.01	ok		
DUT12	1.22	0.273	0.0102		ok	

3.3v anneal, started at 25ma, finished at 20ma (should be almost 0, even with 10 parts)

168 hours anneal with bias						
	WRITE	READ	STBY	VERIFY	TIDRWCYCLE	
DUT1		0.144	0.0688	FAILED		Data and device ID read all zeroes. Attempted to prog this part for first time and it failed (still all zeros)
DUT2		1.55	1.499	FAILED		Data and device ID read all zeroes.
DUT3		0.272	0.205	FAILED		Data and device ID read all zeroes.
DUT4		0.288	0.0125	OK		
DUT5		0.321	0.224	FAILED		Data and device ID read all zeroes.
DUT6	1.53	0.288	0.0136		OK	
DUT7	1.54	0.279	0.0118		FAILED	Just 256 errors on init readback.
DUT8	1.12	1.08	0.837		FAILED	Looks like nothing happening
DUT9	1.52	0.0184	0.013		FAILED	Communicated at first and R/W a couple times, but FF step seems to have completely killed it.
DUT10	0.205	0.166	0.113		FAILED	Data and device ID read all zeroes.
DUT11		0.275	0.01	ok		
DUT12	1.22	0.273	0.0102		ok	