The Application of Hardware in the Loop Testing for Distributed Engine Control

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Outline

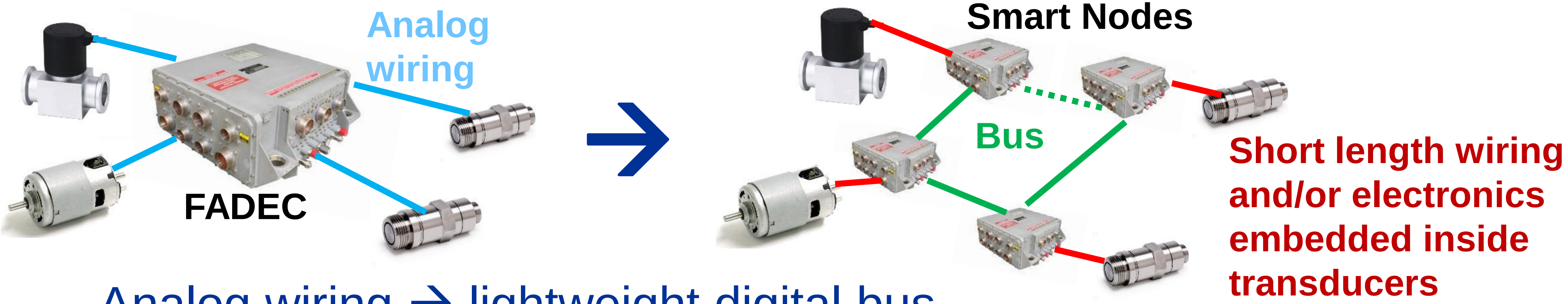
- **Introduction**
- HIL Test Implementation
- HIL Test Results
- Ancillary High Bandwidth Pressure Signal Modeling
- Conclusions
- Future Work

Introduction

- Push in industry to meet future design goals (N+2/N+3)
  - Fuel economy, noise, emissions
- Research on technologies to meet goals
  - Main technologies
    - Ultra high bypass
    - Hybrid electric
    - etc.
  - Support technologies
    - Distributed engine control (DEC)
    - etc.

Introduction

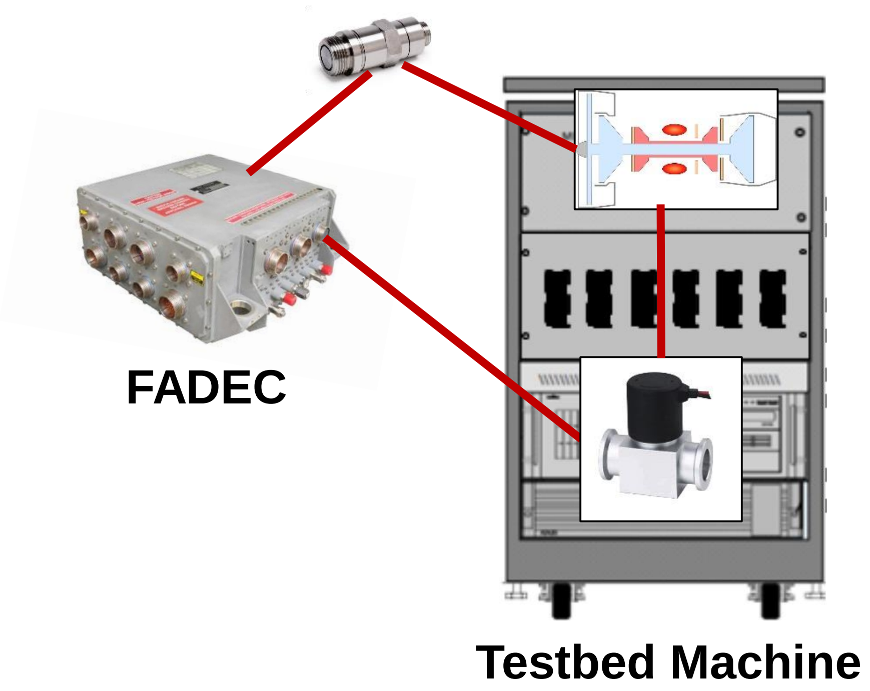
- Distributed engine control (DEC)
  - Replaces centralized control (FADEC)

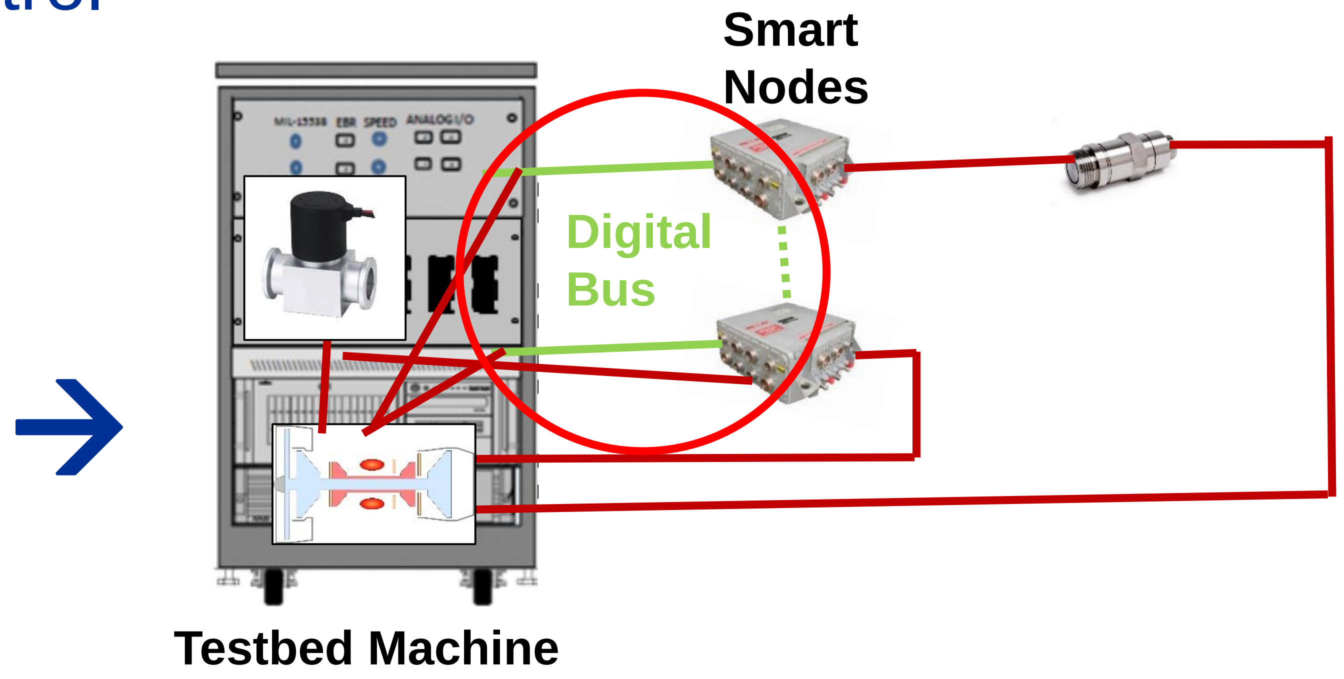


  - Analog wiring → lightweight digital bus
    - Reduced weight = better fuel economy
    - Better scalability, easier certification process and overhauls
  - Support advanced control (Active surge / combustion control)
  - Electronics limited by high temperature environment!
  - Needs different test techniques than centralized systems

Intro – How Does DEC Change HIL Testing?

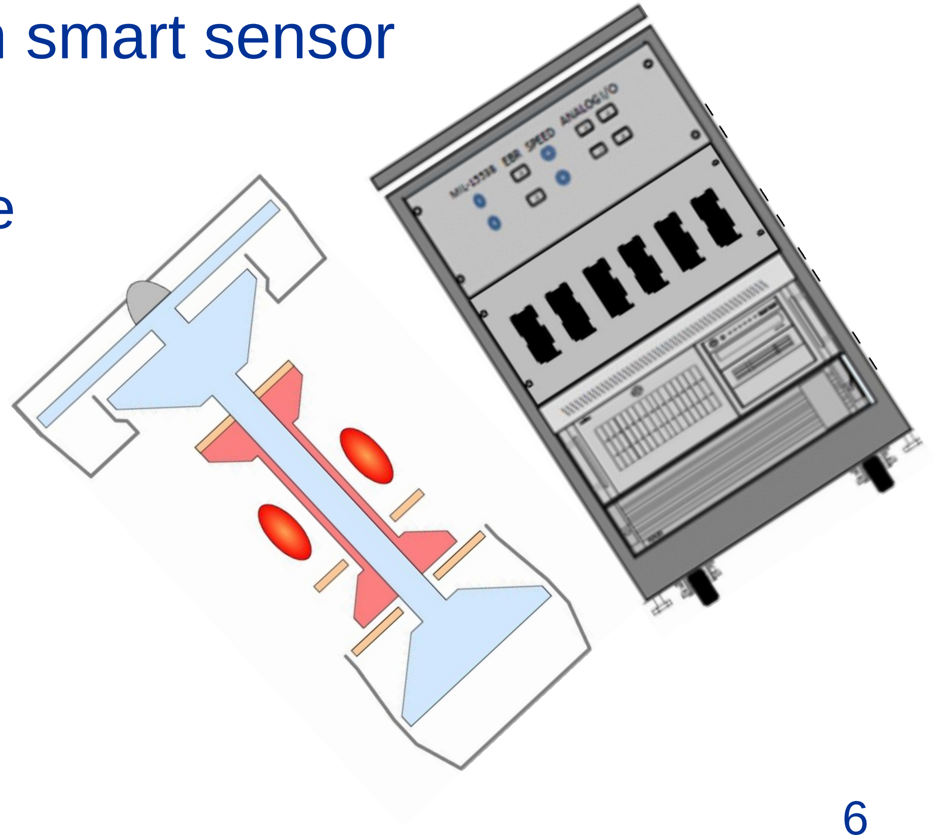
- Testing centralized control
  - Just a FADEC and/or analog transducers
- Testing distributed control
  - More complicated





Intro – HIL Testing of DEC Devices

- Research goals
  - Demonstrate modular DEC HIL test techniques and testbed
    - Smart sensor via Sporian Microelectronics serves as test case
  - Investigate applications of high bandwidth smart sensor
    - Active surge/stall control
    - Stall precursors are audible → Audio range



- Research tools
  - C-MAPSS40k (Distributed)
  - DEC System Simulator (DECSS)
    - 16 core real-time computer with IO
  - Simulation (Sim) Workbench

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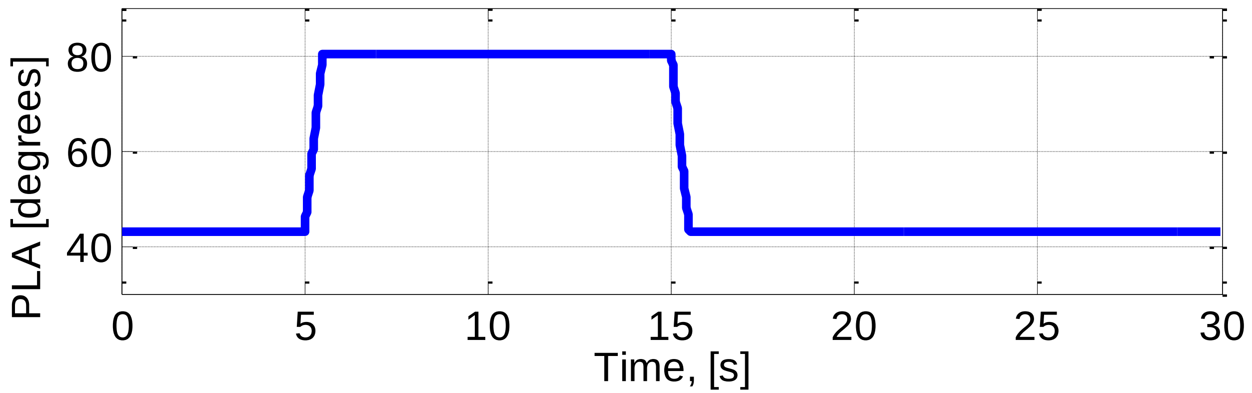
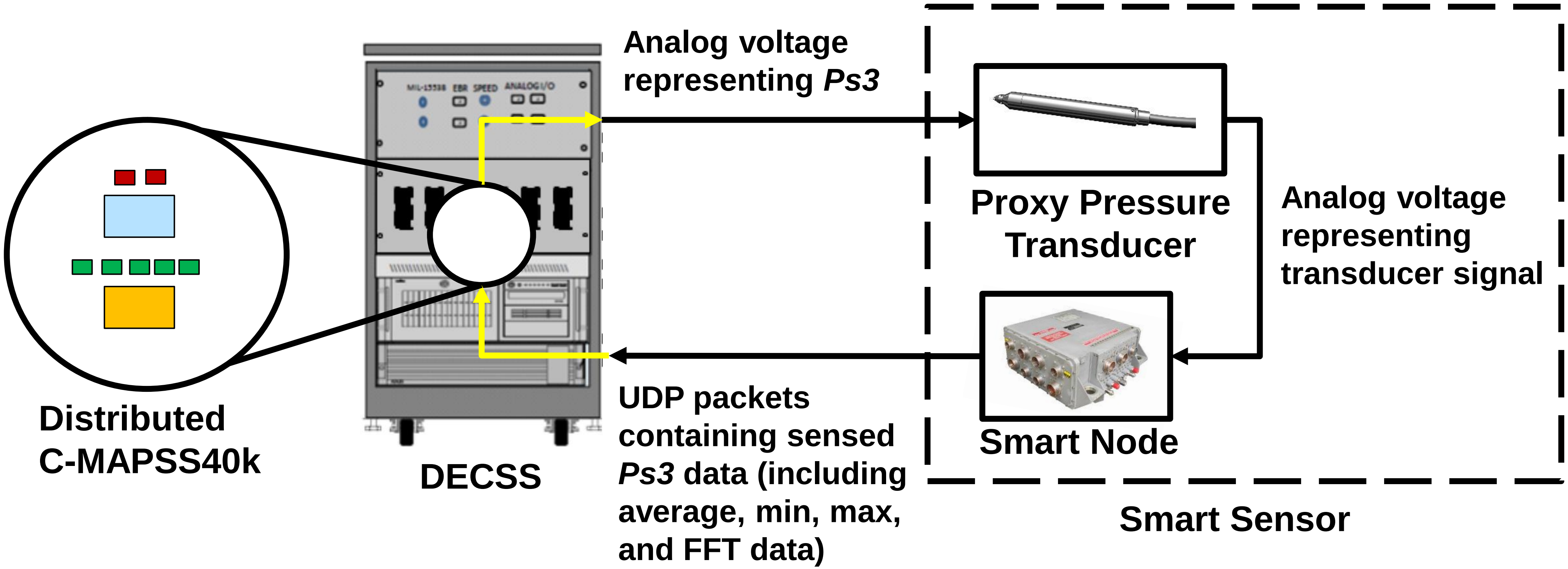
HIL Test Implementation

- What is our HIL test?
  - Smart P3 sensor in C-MAPSS40k simulation loop running on DECSS
  - Replaces C-MAPSS40k Ps3 sensor for feedback
  - Test is low bandwidth (signal $f < 1/(2T_S)$; $f < 33.3$ Hz)
- Test conditions
  - Throttle (PLA) burst and chop (idle to full power and back)
  - Sea-level-static (SLS)

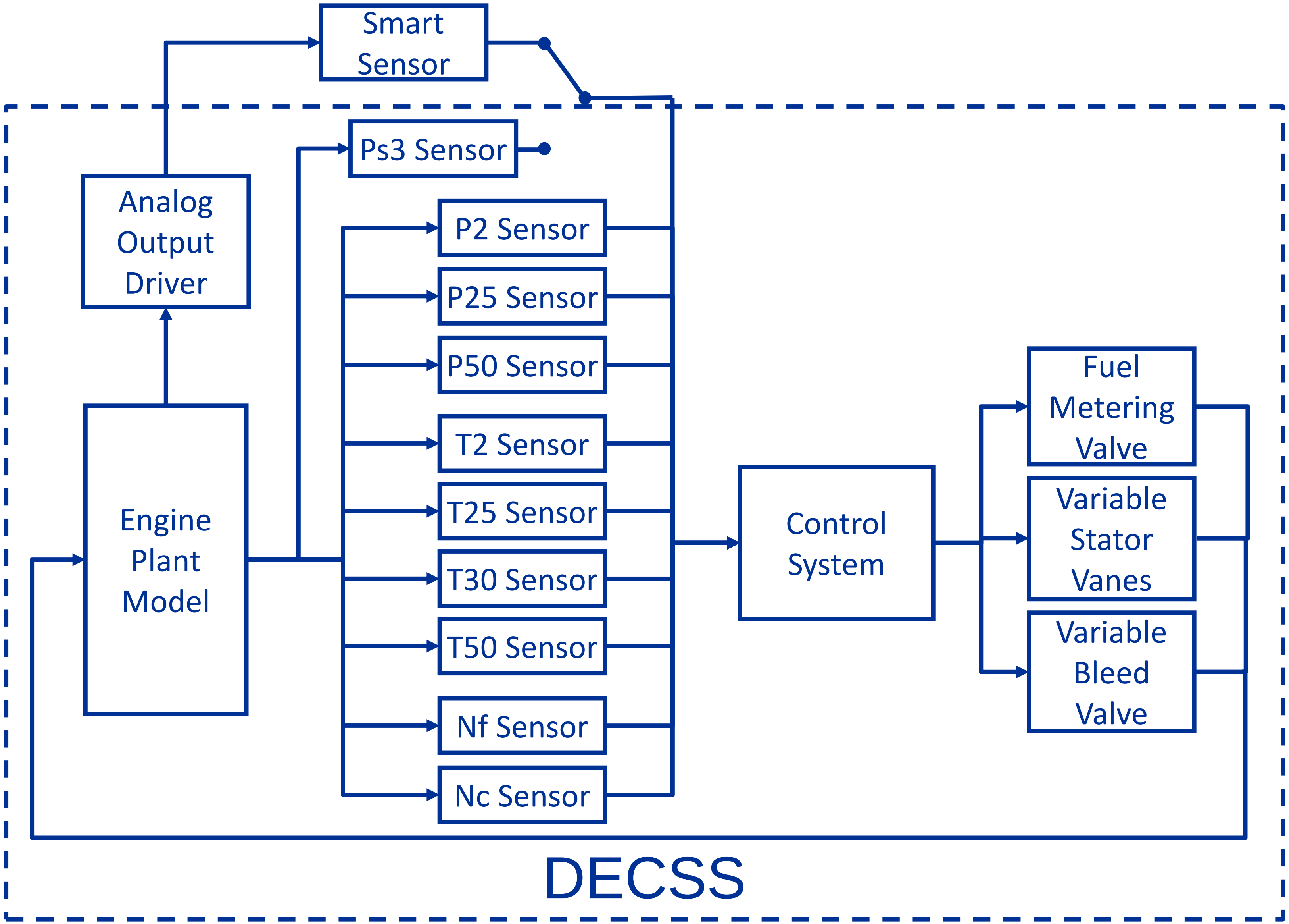


HIL Test Implementation

- HIL Test Loop



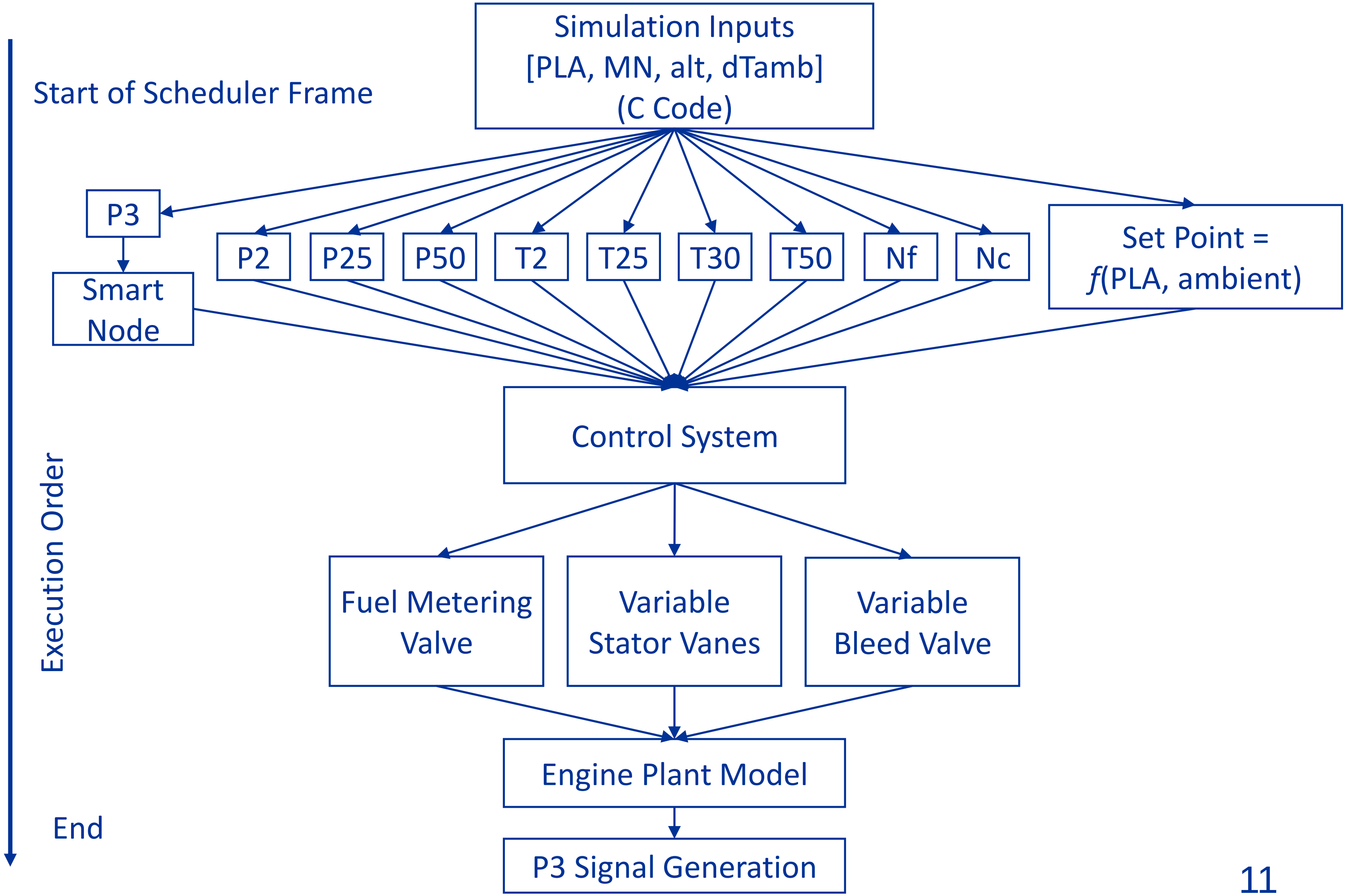
HIL Test Implementation



- Distributed C-MAPSS40k as implemented on DECSS
- Also shown: smart sensor substitutes simulated Ps3 sensor

HIL Test Implementation

- Sim Workbench “test” construction
- i.e. Programs and execution order for HIL test



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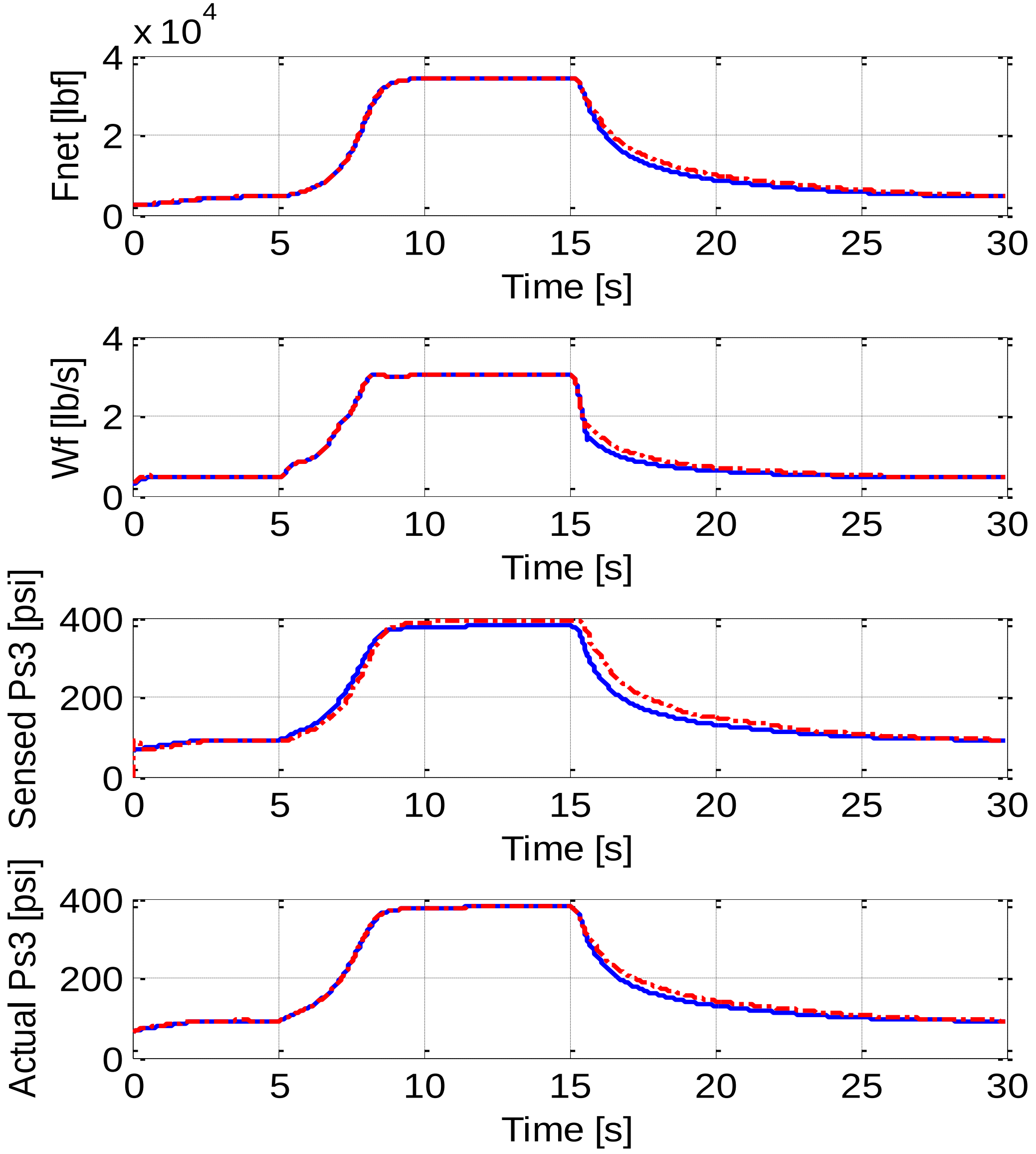
HIL Test Results

- Net thrust, fuel flow, sensed Ps3, and actual Ps3
  - Blue = Baseline (simulation only)
  - Red = HIL test (w/ smart sensor)
- Smart sensor Ps3 has 100 ms lag
- Actual and closed-loop response only change during decel
  - Wf/Ps3 (R/U) overestimated
  - More conservative limiting
- All limits protected in both cases



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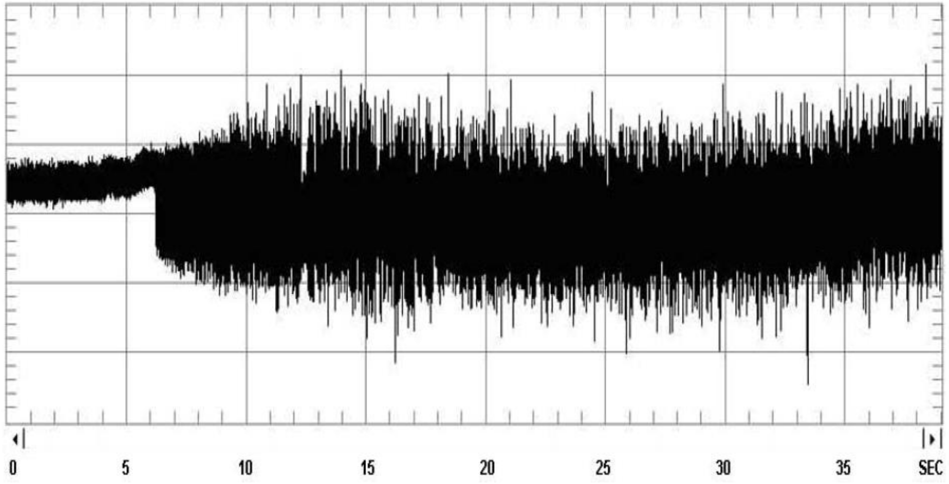
Ancillary $P3_{HB}$ Signal Modeling

- Data from literature about stall/surge are often taken with high bandwidth Kulite sensors, but DC levels and scales not shown
  - Limitation of sensors
- Data suggest that pressure disturbances due to blades passing by stator vanes are picked up and that their magnitude correlates to compressor stall (and surge often comes after stall inception)



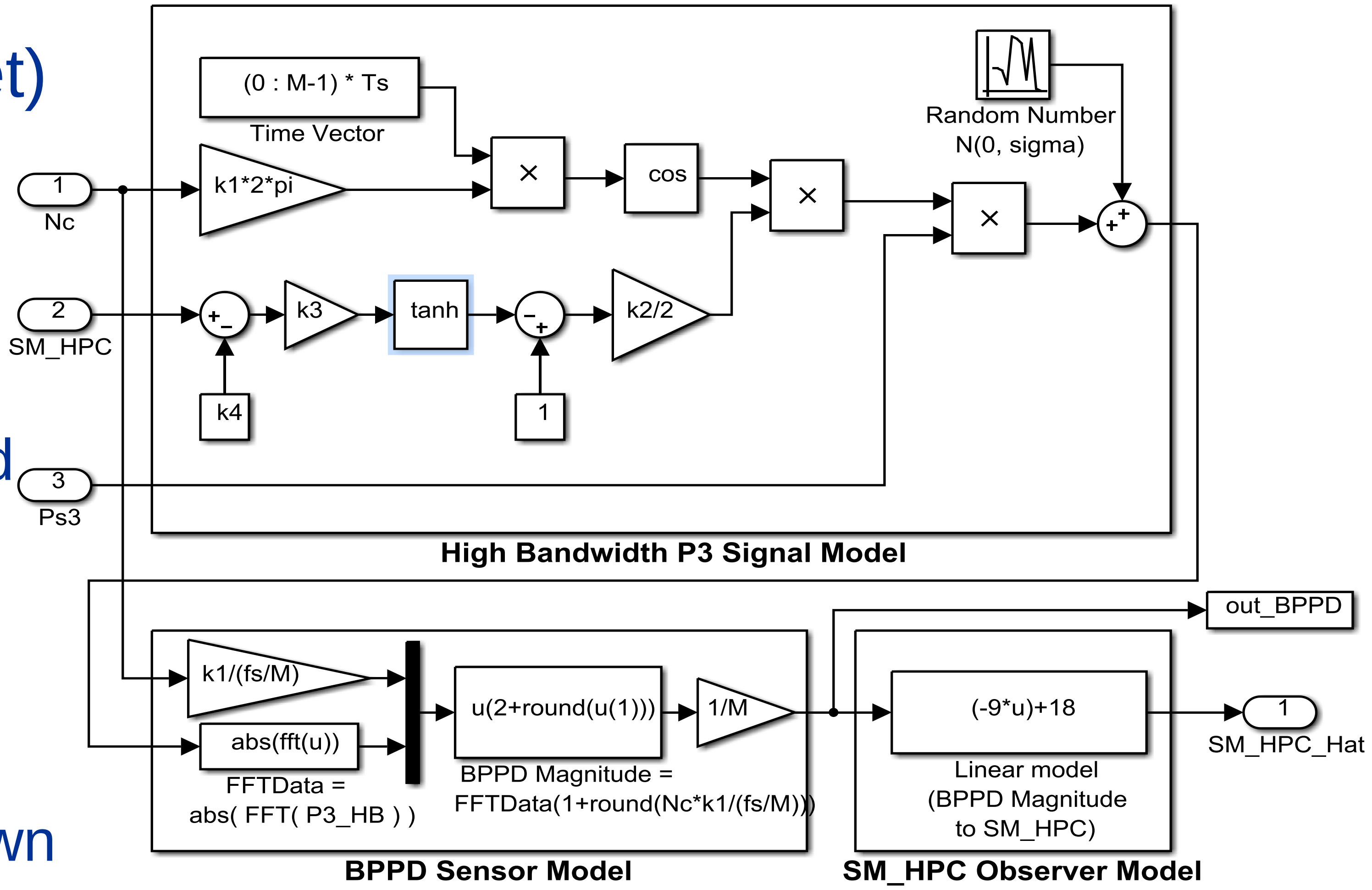
Compressor stall inception as HPC flow is throttled: Abdel-Fattah, A. M. and Vivian, A. S., "Development of the Larzac Engine Rig for Compressor Stall Testing," Defense Science and Technology Organization, Victoria, Australia, DSTO-RR-0377, 2010.

Ancillary $P3_{HB}$ Signal Modeling

- Preliminary high bandwidth P3 model added to C-MAPSS40k
- Assumptions
  - $P3_{HB} = Ps3$ + blade passing pressure disturbances (BPPD)
  - BPPD is sinusoidal, comes from one compressor stage only
  - BPPD magnitude is nonlinear, sigmoidal function of HPC surge margin
  - BPPD frequency is proportional to HP shaft speed times number of blades in that stage
  - All noise in P3HB measurement is lumped together and is AWGN
- $P3_{HB} = Ps3 + \left(\frac{k_2\left[1 - \tanh\left(k_3 * (\mathrm{SM_{HPC}} - k_4)\right)\right]}{2} \cdot \cos(k_1 \cdot 2\pi Nc \cdot t)\right) + \mathrm{N}(0, \sigma^2)$
- Goal: HPC SM can be estimated from P3HB measurement and used for closed-loop surge control

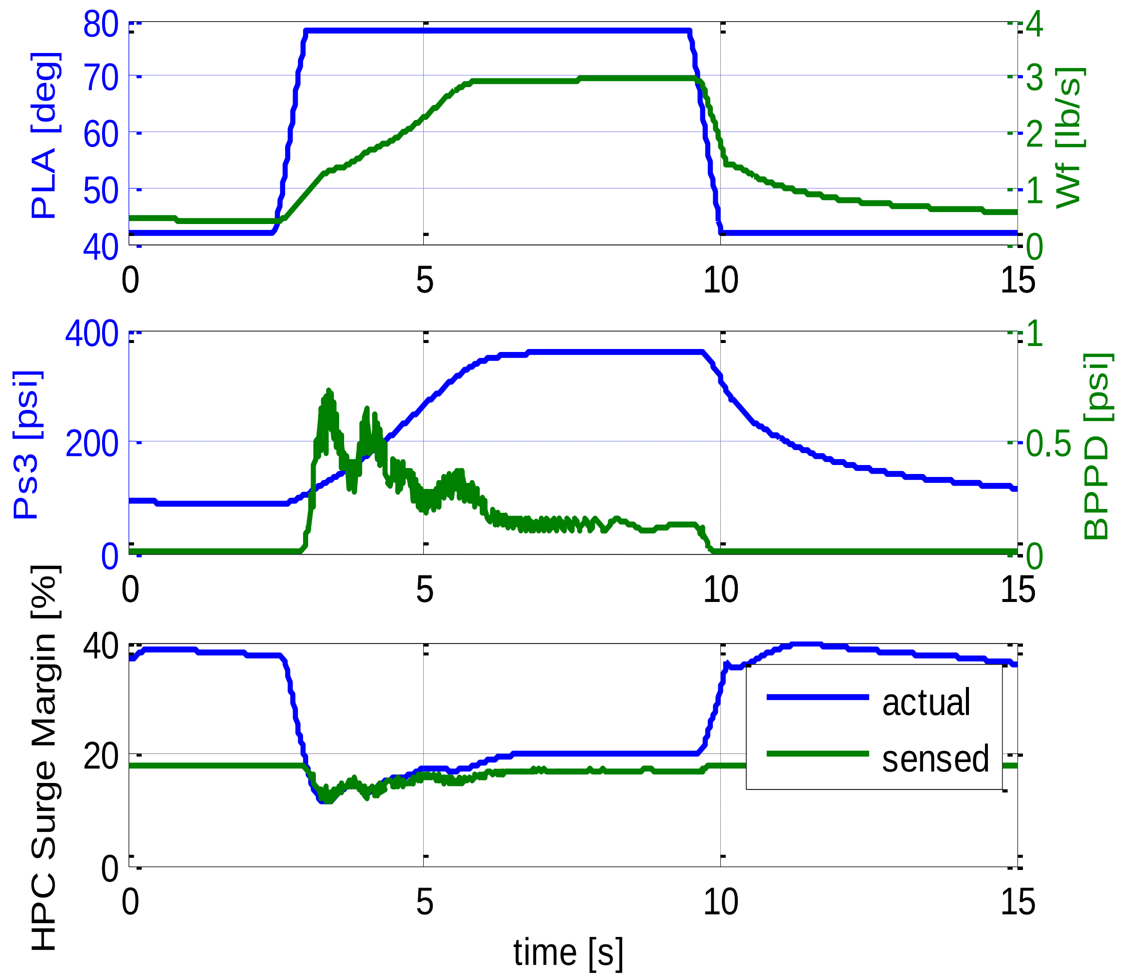
Ancillary $P3_{HB}$ Signal Modeling

- Initial Simulink-only test (HIL test not performed yet)
  - P3HB signal model – implementation of previous equation
  - BPPD sensor model – BPPD magnitude recovered from FFT of sensed $P3_{HB}$
  - HPC SM observer model – surge margin backed out from BPPD magnitude
  - HPC SM limit logic not shown



Ancillary $P3_{HB}$ Signal Modeling

- Simulink-based simulation test results
- HPC surge margin limit is protected
- Limiter state chatters on/off
  - Can retune
- Response is very slow
  - Needs improvement
- Extend to entire flight envelope



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Conclusions

- Demonstrated HIL test of smart P3 sensor on DECSS in C-MAPSS40k Simulation loop
  - HIL test is modular, allows nodes to be added or subtracted from test loop
  - Smart sensor works as intended except lag, not characterized yet
    - May be due to UDP channel, sensor dynamics, delays in signal generator HW
- P3HB signal model + active surge control models
  - Demonstrate potential modeling approach for active surge control
  - Need better data for validated empirical model

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Future Work

- Apply HIL test development techniques to DEC and other problems
- Obtain high quality compressor data to improve model
- Extend active surge control logic to entire flight envelope

Done! Questions?