500°C Electronic Packaging and Dielectric Materials for High Temperature Applications

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Presenter

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- Senior Scientist
- Ohio Aerospace Institute (OAI) / NASA Glenn Research Center
- Ph.D. in experimental solid state physics/Case Western Reserve University
- Research Interests
  - Packaging materials, process, design, and testing for high temperature SiC electronics and sensors for aerospace applications
- Currently supporting high temperature electronics/sensor packaging research at NASA Glenn Research Center

Outline

- Background
  - SiC and SOI electronics and sensors, aerospace applications
  - Packaging/integration concepts/functions
    - Conventional electronics packaging material system issues
- High temperature ceramic packaging systems
  - Dielectric properties of selected alumina and aluminum nitride
  - Metallization for high temperature applications
  - Prototypes of packages and PCBs
  - Results of laboratory tests, space and flight test with SiC electronics
  - SOI circuits for Distributed Engine Control
    - Circuit level test above commercial temperature limit
    - Specifications vs T and derating?
- Sensor packaging – capacitive pressure sensor
- Dielectric for high temperature capacitors
- Summary
- Acknowledgements

Background

500°C SiC electronics and MEMS sensors have been demonstrated

- JFET ICs, MEMS based pressure sensor and Schottky diode based gas chemical sensors
- Applications include aerospace engine control and long term Venus probes

Commercial SOI ICs for 225°C, operable at T > 225°C for Distributed Engine Control ?

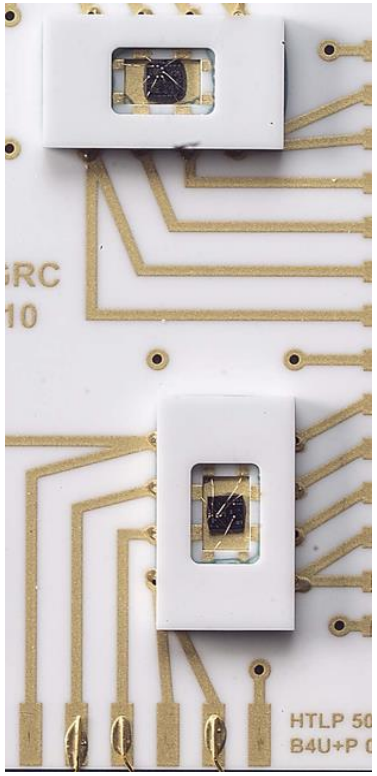
Conventional packaging technologies

- Plastic materials melt, de-polymerize, and burn at high temperatures
- Conductor and alloys (solder) melt and oxidize rapidly at high temperatures
- High thermal stress due to thermal expansion mismatch - mechanical failure at structure level
- Challenges at material and structure levels

Background: Packaging Concepts

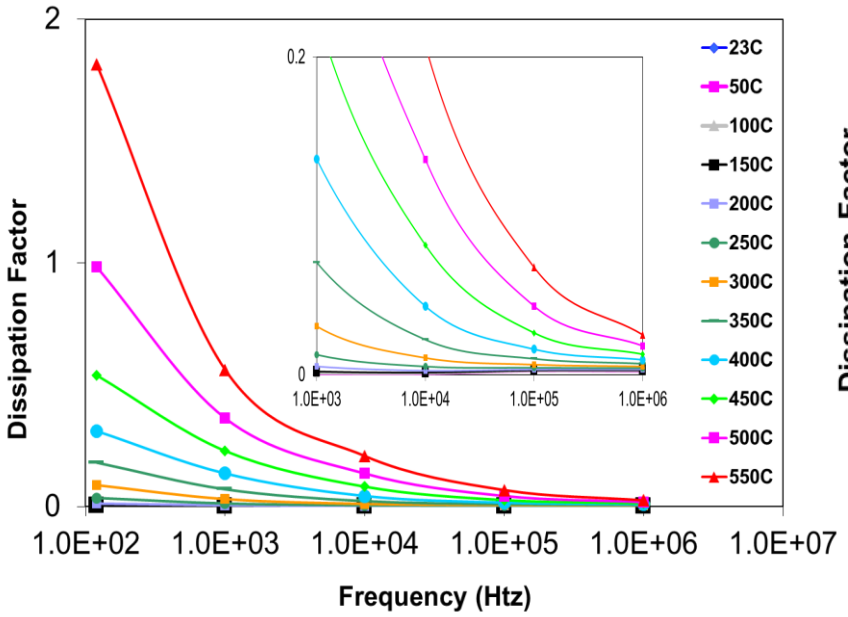
Packaging Technology for Electronics/Sensors

- Packaging is essential to microelectronics and sensors
  - Mechanical support
  - Electrical interconnection
  - Electromagnetic, chemical environment
- Chip-level packaging
  - Substrate and metallization
  - Die-attach
  - Wire-bonding
- Printed Circuit Board (PCB)
  - Interconnecting packaged chips and passives
- PCB edge connectors
  - Subsystem level packaging
- Capacitive pressure sensor packaging
  - Spark-plug type
  - High differential pressure environment

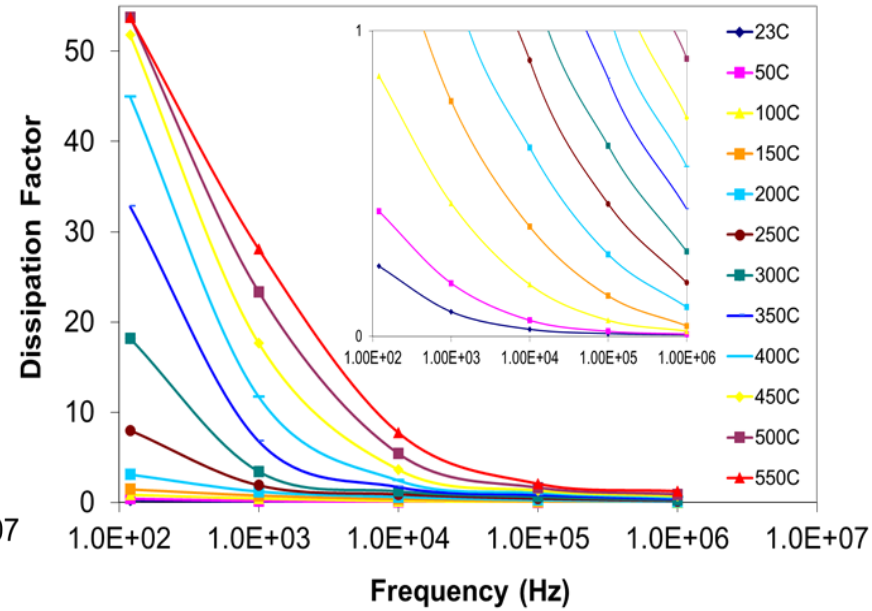


Background: Temperature Dependent Dielectric Properties of Polycrystalline Al_2O_3 Substrates

Dissipation Factor of selected 96% Al_2O_3 substrate at various frequencies



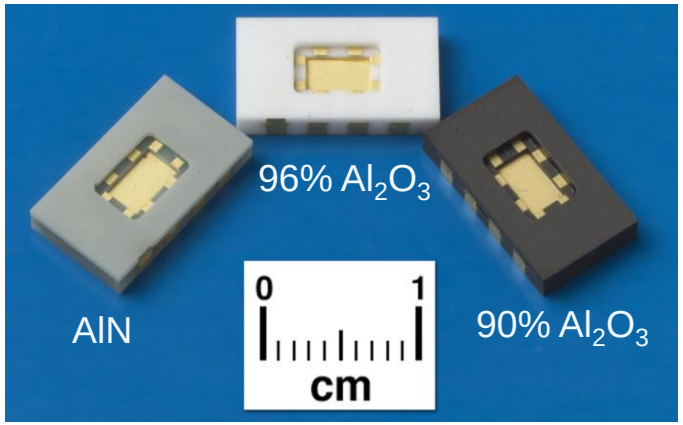
Dissipation Factor of selected 92% Al_2O_3 substrate at various frequencies



- Dissipation factors changes with T and f significantly
- Dissipation factor is purity/impurity dependent
- Dissipation factor of selected 96% is lower compared with selected 92%

Ceramic Packaging Systems for 500°C SiC Electronics

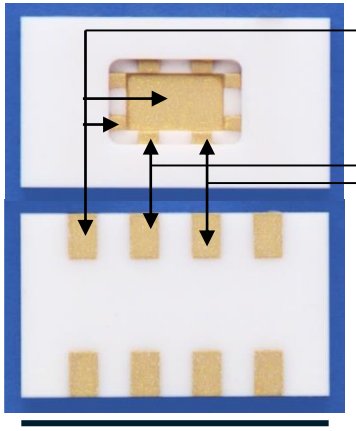
Ceramic Chip-level Packages and PCBs



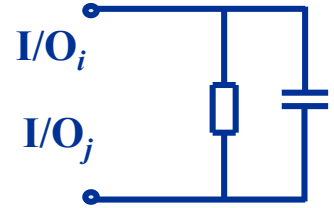
- Three types of ceramics and Au thick-film metallization based chip-level packages and printed circuit boards (PCBs)
- Chip-level packages characterized between room temperature and 500°C
- Tested with SiC ICs at 500°C and thermal cycled

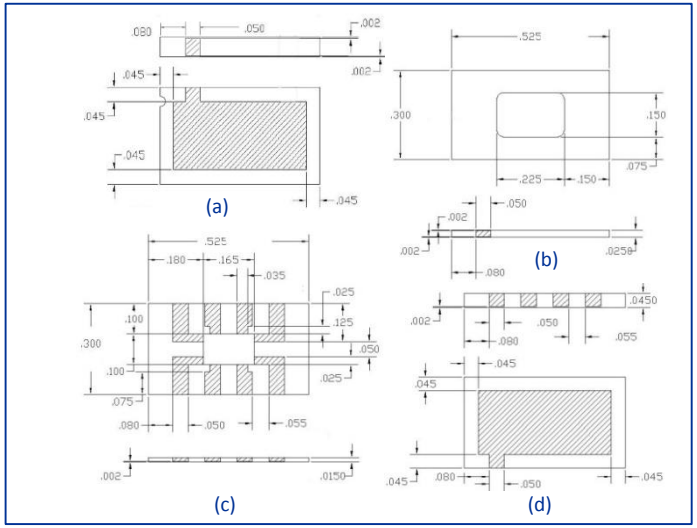
Packaging Systems for 500°C SiC Electronics
- 96% alumina packaging system - laboratory test

96% Alumina Chip-level Packages



Parasitic Equivalent





Parasitic Capacitance and Conductance of Neighboring I/Os

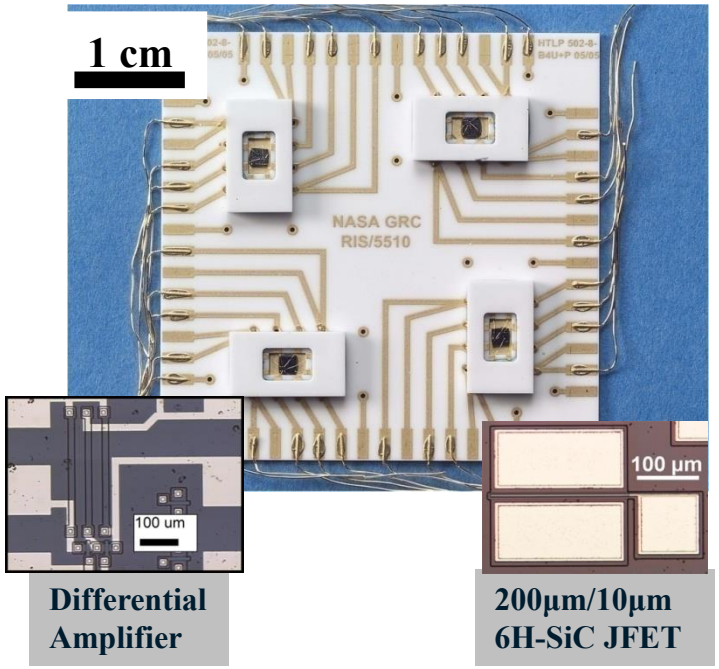
T (ºC) / f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550
100	0.00nF	0.00nf	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	0.00nF	< 5	5
	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.005	0.00	0.00
120	0.5	0.5	0.5	1	1	1	1.5	1.5	1.5	1.5	2
	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.0005	0.001	0.001
1K	0.5	0.5	0.5	0.5	0.5	0.5	0.6	0.7	0.7	0.8	0.95
	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.001	0.001	0.002	0.0025
10K	0.49	0.50	0.50	0.490	0.49	0.52	0.53	0.58	0.59	0.65	0.69
	0.001	0.000	0.000	0.000	0.000	0.001	0.002	0.003	0.004	0.006	0.008
100K	0.492	0.486	0.497	0.493	0.487	0.517	0.539	0.535	0.563	0.585	0.57
	0.005	0.006	0.0015	0.002	0.003	0.005	0.007	0.011	0.015	0.022	0.030
1M	0.501	0.497	0.485	0.506	0.499	0.529	0.533	0.55	0.556	0.544	0.55
	-	-	-	-	-	-	-	-	-	-	-

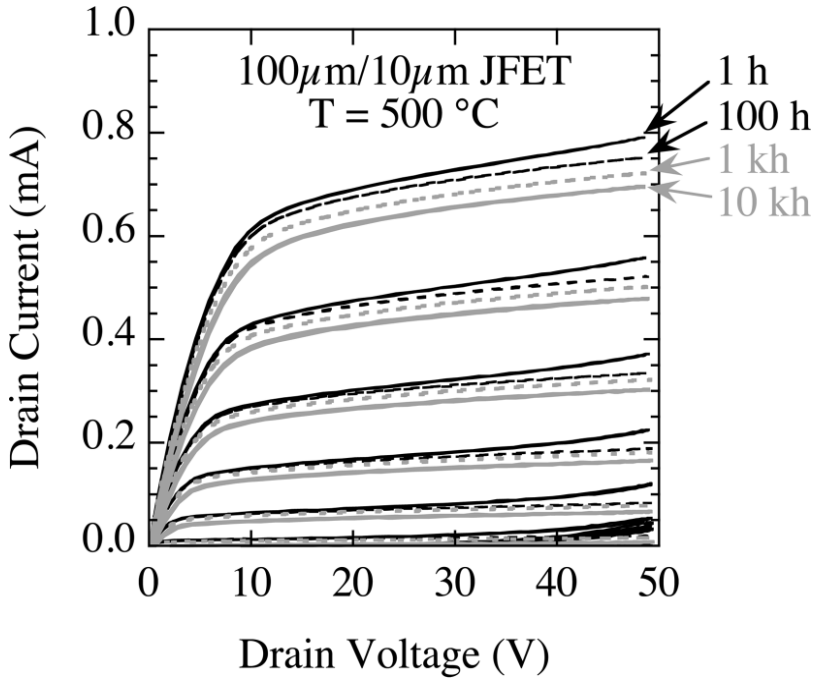
Usable for packaging many envisioned low power 500°C devices/ circuits

pF
µS

Packaging Systems for 500°C SiC Electronics
- 96% alumina packaging system - laboratory test

Test Results of Packaged SiC JFET

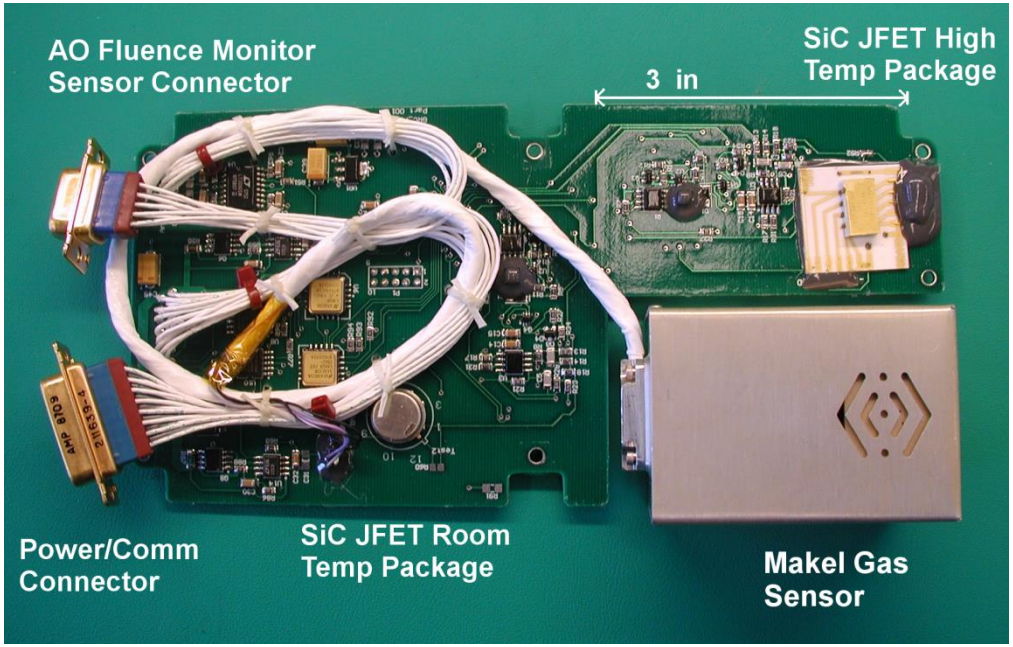




- A packaged SiC JFET characterized at 500°C
- Less than 7% change in the JFET characteristics in first 6000 hours
- Tested at 500°C for over 10,000 hrs
- Demonstrated for long term operation at 500°C for the first time

Packaging Systems for 500°C SiC Electronics
- 96% alumina packaging system – space and flight test

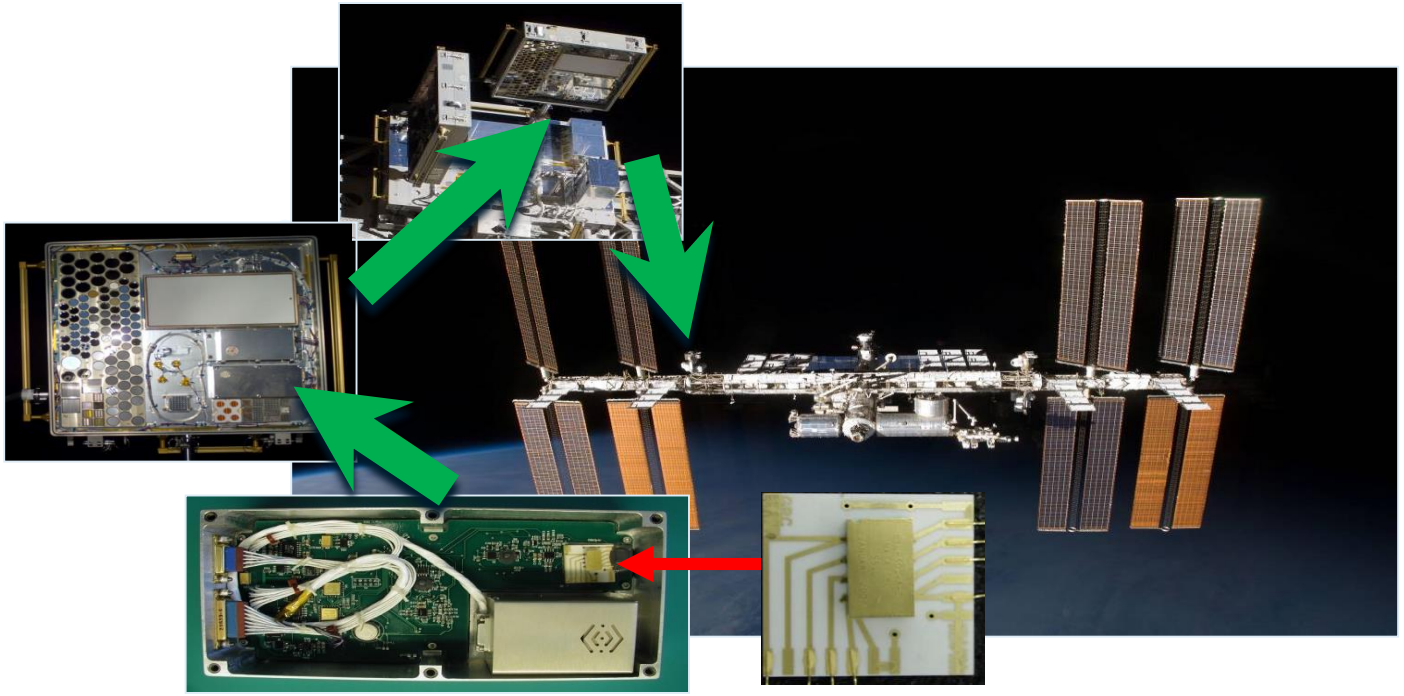
Space and Flight Test of 96% Alumina Packaging System



- 96% alumina chip-level packaging, PCB, and joining materials
- First flight and space test of 96% alumina high temperature harsh environment packaging system
- Monitor packaged SiC JFET DC parameter and compare with a SiC JFET in a conventional package

Packaging Systems for 500°C SiC Electronics
- 96% alumina packaging system – space and flight test

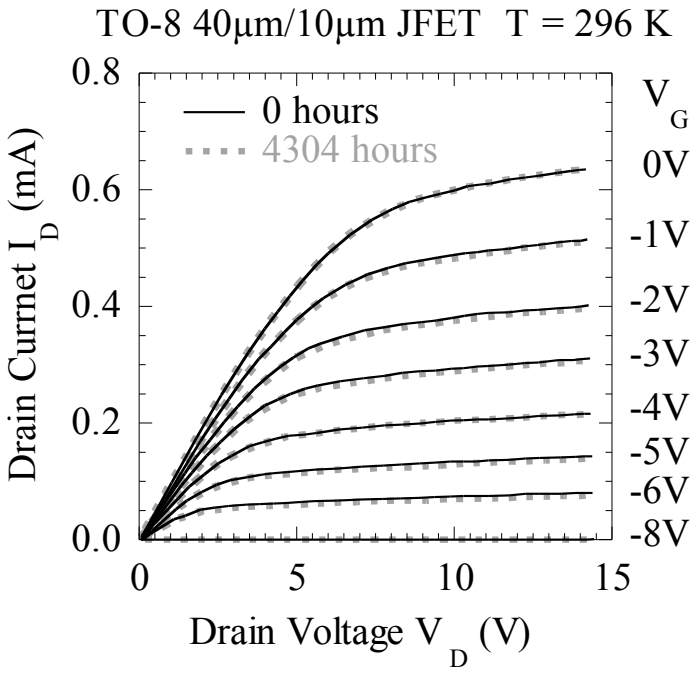
Space and Flight Test of 96% Alumina Packaging System

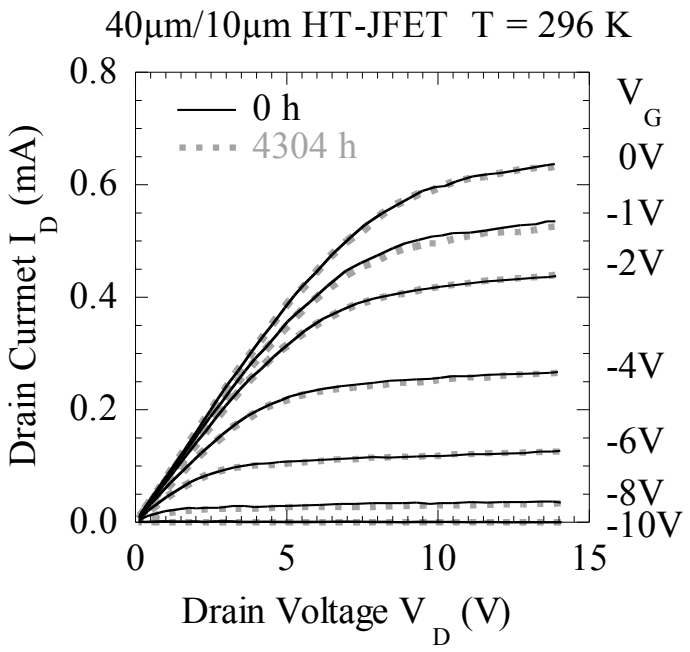


- MISSE7 suite exposed to Shuttle launch, atomic oxygen, space radiation, thermal cycling, and reentry
- In an aluminum box
- Eighteen months on ISS orbit

Packaging Systems for 500°C SiC Electronics
- 96% alumina packaging system – space and flight test

On-orbit I-V Data of Packaged SiC JFETs





- I-V data acquired every hour with temperature measurement
- Eighteen months on orbit
- Latest set of V_{DS} vs. I_D curves shows no degradation
- No packaging degradation/failure detected after space and flight tests

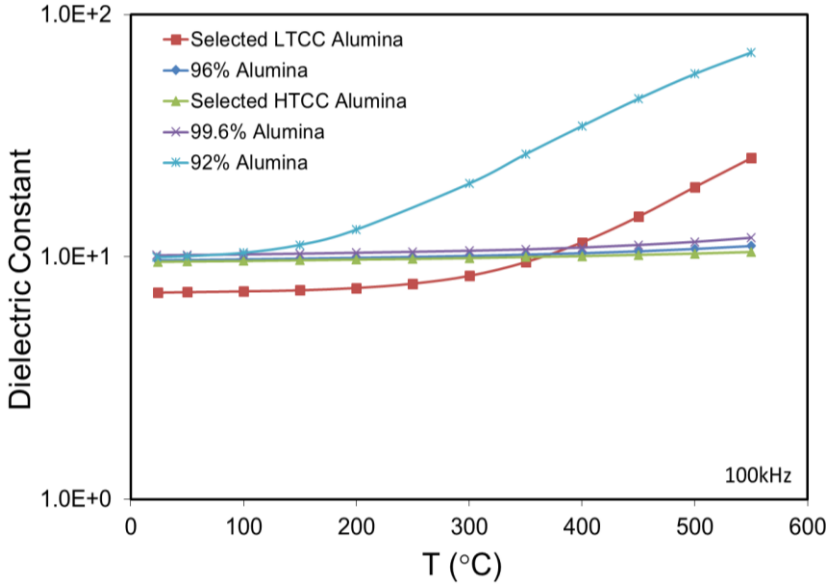
Co-fired Alumina

- 96% alumina substrate based packaging system
  - Dielectric properties of 96% alumina measured at temperatures up to 550°C
  - Excellent electrical and dielectric properties as substrate for conventional electronics
  - Thin-film and thick-film metallization available
  - 96% alumina packaging system long term tested with SiC electronics at 500ºC
  - Chip-level packages not fabricated with co-fired process

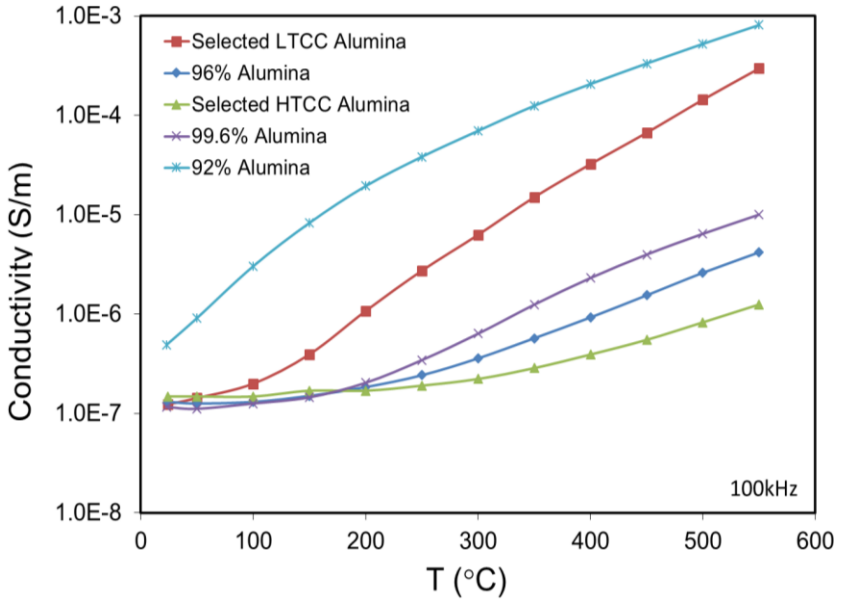
- Low temperature and high temperature co-fired (LTCC and HTCC) alumina substrates ?
  - A few percent of glass used in co-fired alumina systems
  - Suitable for large scale commercialization
  - Dielectric performance at high temperatures?
  - Co-fired metallization

Co-fired Alumina High Temperature Packaging System

Dielectric Constant



AC Conductivity



Dielectric constant of selected HTCC alumina stable below 300°C, increases slightly with T above 300°C – less compared with 96% alumina and selected LTCC alumina

AC conductivity of selected HTCC alumina is lower and increases less compared with selected 96% alumina and LTCC alumina

Co-fired Alumina High Temperature Packaging System

High temperature co-fired (HTCC) alumina

- Co-fired at T >1500°C
- A few percent of glass used in co-fired alumina systems
- Dielectric performance of selected HTCC alumina tested at high temperatures
- Pt metallization
  - Chemically stable at high temperatures
  - Low CTE (8.8×10^{-6}/C°)
  - Aluminum oxide for binder - Thermodynamically stable
  - Alloy with Au, Au is always surface rich at elevated temperatures

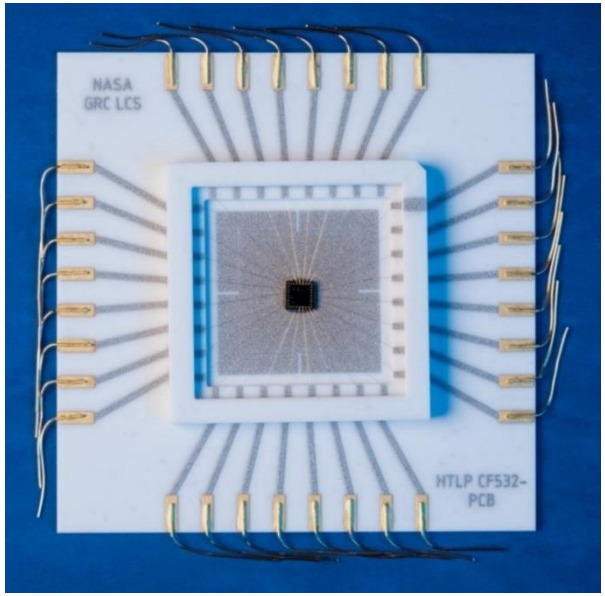
Compared with 96% alumina

- Dielectric constant of HTCC alumina is slightly lower and it increases less with temperature. AC conductivity of this material is also lower than that of 96% alumina at temperatures above 200°C
- Dissipation factor of HTCC alumina is always lower compared with that of 96% alumina at temperatures above 250°C

OAI

Co-fired Alumina Packaging System

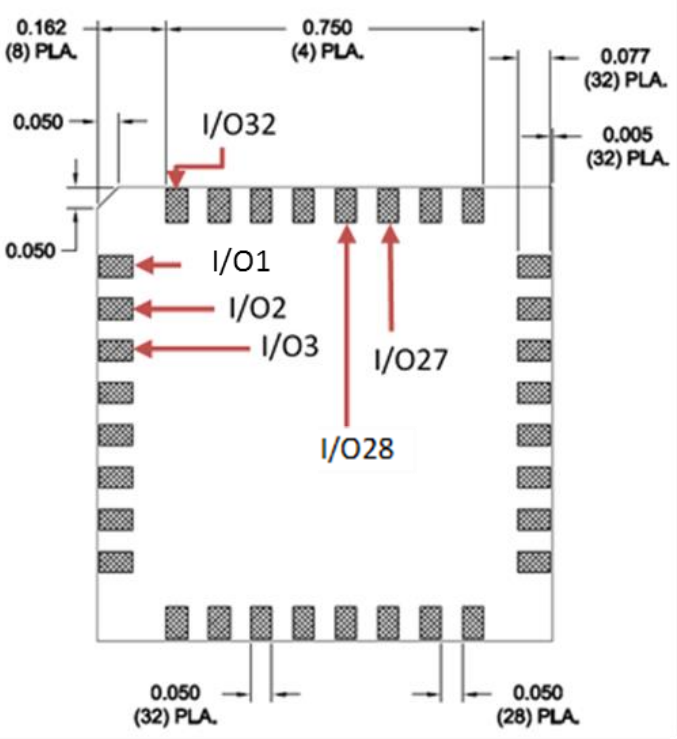
Test Assembly of a SiC IC with HTCC Alumina Packaging System



- Packaged SiC chip with Pt/HTCC alumina package and PCB
- PCB measures 2 inch x 2 inch, Pt traces co-fired with alumina
- 1 mil Au alloy wire thermo-sonically bonded
- High temperature die-attach

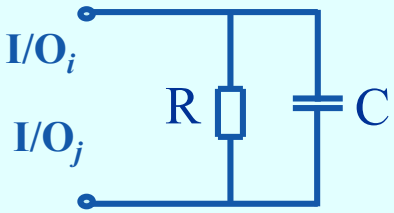
HTCC Alumina Package – Equivalent Circuit

Parasitic R//C of Neighboring I/Os



1.07 inches

Parasitic Equivalent



R//C model

R – DC leakage and AC dielectric loss

C – Dielectric polarization

$$1/Z(T,\omega) = G(T,\omega) + j\omega C(T,\omega)$$

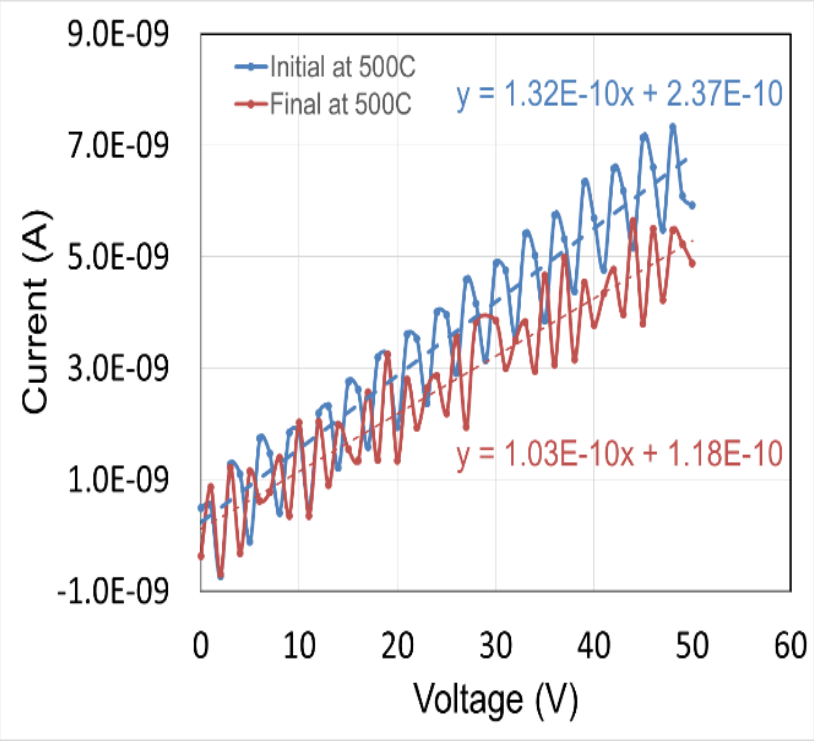
R//C measured between I/O1 - I/O2, and I/O2 - I/O3

- I/O1 connected to all five bias pads

DC resistance measured separately

HTCC Alumina Package – DC Resistance

DC Resistance of Neighboring I/Os



DC I - V Curves

- I-V curve between I/O27 and I/O28
- 500°C
- Wide DC bias range: 0 - 50V
- SMU: integration time 16.67 msec, time delay 0.1 sec
- I/O28 not connected to SiC die, I/O27 connected to isolated two-terminal test structure on SiC die
- Package mounted on PCB
- Slope of linear fits: 7.6 GΩ initially 9.7 GΩ after 69.4 hrs
- DC resistance slightly underestimate
- Noise from running oven

HTCC Alumina Package – AC Parasitic R//C

AC Parasitic Capacitance and Conductance of Neighboring I/O1 – I/O2

T (ºC) / f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550
120	1.0	0.7	0.6	0.4	0.3	0.5	0.4	0.6	0.7	1.4	1.4
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.001	<0.001
1K	0.4	0.2	0.5	0.5	0.3	0.4	0.5	0.5	0.5	0.5	0.4
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
10K	0.5	0.4	0.5	0.5	0.4	0.4	0.4	0.5	0.5	0.4	0.4
	<0.001	0.0013	<0.001	<0.001	<0.001	<0.001	<0.001	0.003	<0.003	<0.003	<0.003
100K	0.5	0.3	0.5	0.4	0.3	0.4	0.4	0.5	0.5	0.4	0.4
	0.01	0.016	0.014	0.016	0.016	0.011	0.014	0.029	0.035	0.026	0.045
1M	0.5	0.4	0.5	0.4	0.3	0.4	0.4	0.5	0.5	0.4	0.5
	<0.010	<0.010	0.013	0.012	0.011	0.006	0.009	0.018	0.021	0.022	0.026

> 50°C margin above 500°C

pF
µS

C < 1.5 pF, R > 20 MΩ

Usable for many envisioned 500°C SiC ICs

HTCC Alumina Package – AC Parasitic R//C

AC Parasitic Capacitance and Conductance of Neighboring I/O2 – I/O3

T (°C) / f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550
120	0.7	0.6	0.5	0.4	0.3	0.4	0.4	0.6	0.5	0.6	0.6
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
1K	0.3	0.3	0.4	0.4	0.2	0.4	0.3	0.5	0.3	0.5	0.5
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.0013	0.001	<0.001
10K	0.4	0.3	0.4	0.4	0.3	0.3	0.4	0.4	0.4	0.4	0.3
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
100K	0.3	0.3	0.4	0.4	0.2	0.3	0.3	0.4	0.4	0.4	0.3
	0.005	0.005	<0.005	<0.005	<0.005	0.005	0.013	<0.010	0.014	0.012	<0.010
1M	0.3	0.4	0.4	0.4	0.2	0.3	0.3	0.4	0.4	0.4	0.3
	<0.010	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020

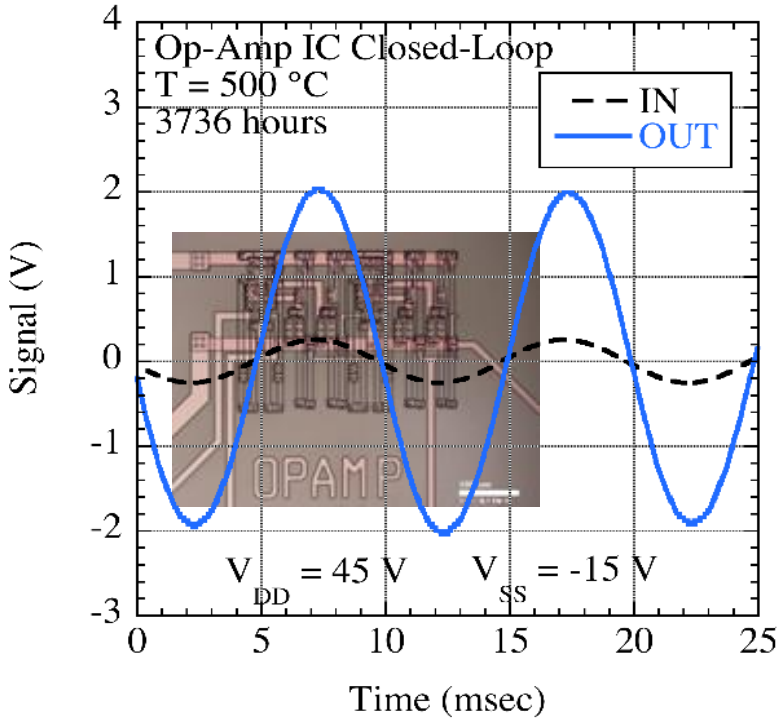
> 50°C margin above 500°C

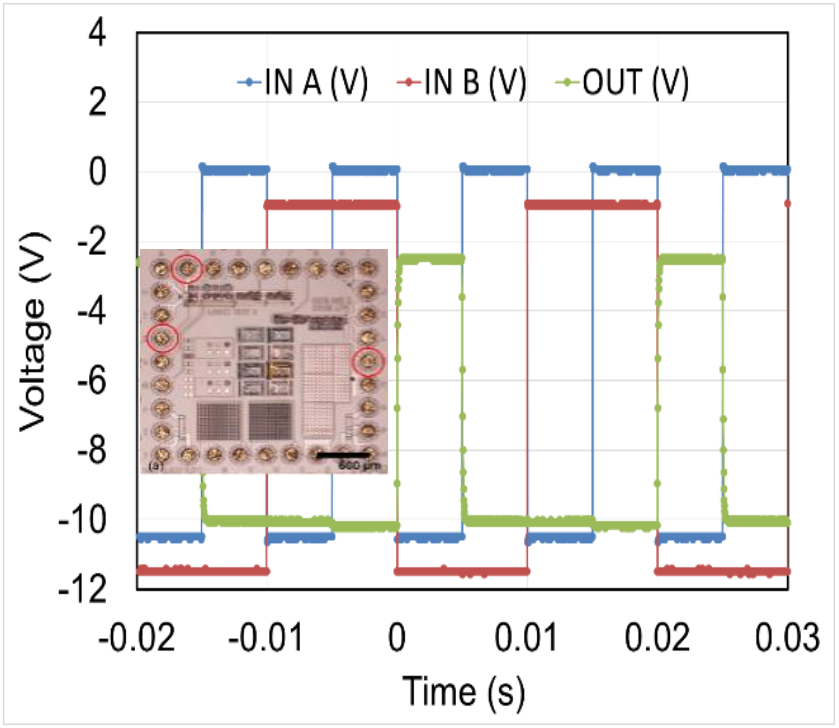
pF
µS

C < 1.5 pF, R > 20 MΩ

Usable for packaging many envisioned 500°C SiC ICs

Co-fired Alumina Packaging System - Test with SiC ICs at High Temperature





Input (dark) and output (blue) waveforms of OPAMP in closed loop with SiC epi-resistors of ratio of 8 to 1
500 °C air ambient after 3736 hours

Input (red and blue) and output (green) waveforms of a NOR logic gate after 143.5 hours test in 700 °C air ambient

Test of SOI 555 Timer and OPAMP with High Temperature Packaging

Commercial SOI ICs

- The oxide layer reduces junction leakages at elevated temperatures
- Maximum operation temperature for SOI circuits specified as 225°C
- Temperature limit by packaging

Can SOI ICs operate digitally above 225°C?

- Without packaging and passive limits
- Square wave oscillator based on SOI 555 Timer tested at elevated temperature using high temperature packaging, passives at T_R

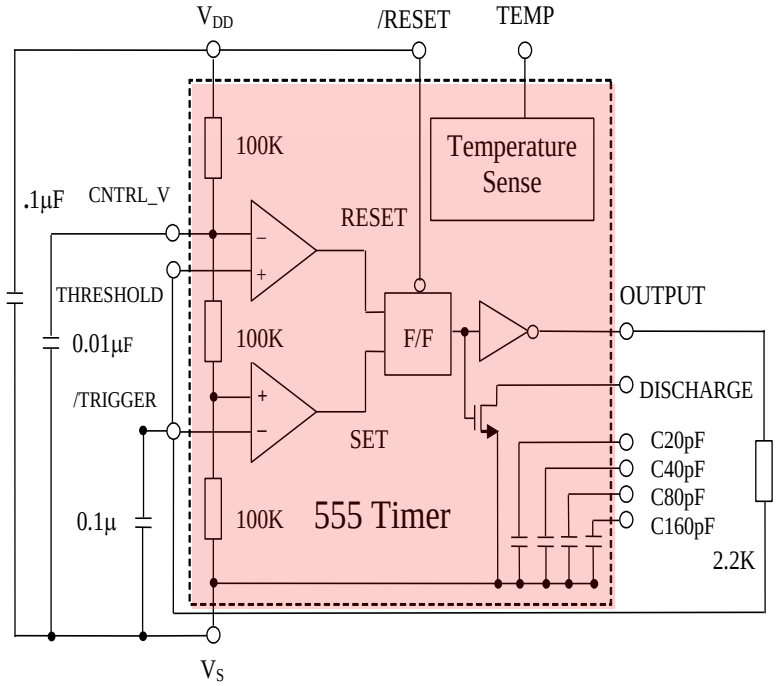
Can SOI analog ICs operate above 225°C?

- Without the limits of packaging and passives
- SOI OPAMP tested at cryogenic temperatures and 200°C
- Followers and inverters based on SOI OPAMP tested at high temperature using high temperature packaging, but passives at T_R

For Distributed Engine Control applications?

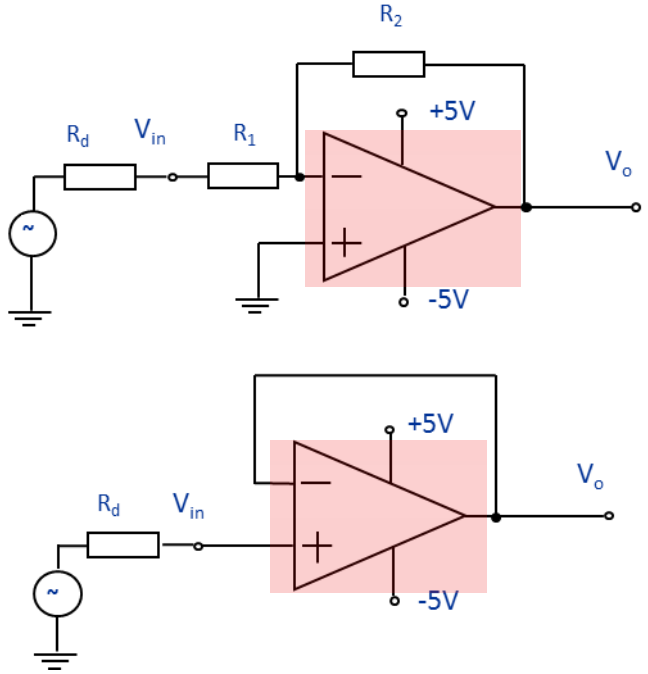
SOI 555 Oscillator and OPAMP Tests Facilitated by High Temperature Packaging

Oscillator Circuit with External Passives



- Square wave oscillator based on a SOI 555 Timer
- Oscillation frequency determined by RC charging and discharging time constant
- I_{DC}, f, duty cycle, output amplitude, and rise time measured against the temperature and time
- Timer can operate at T>225°C de-rating

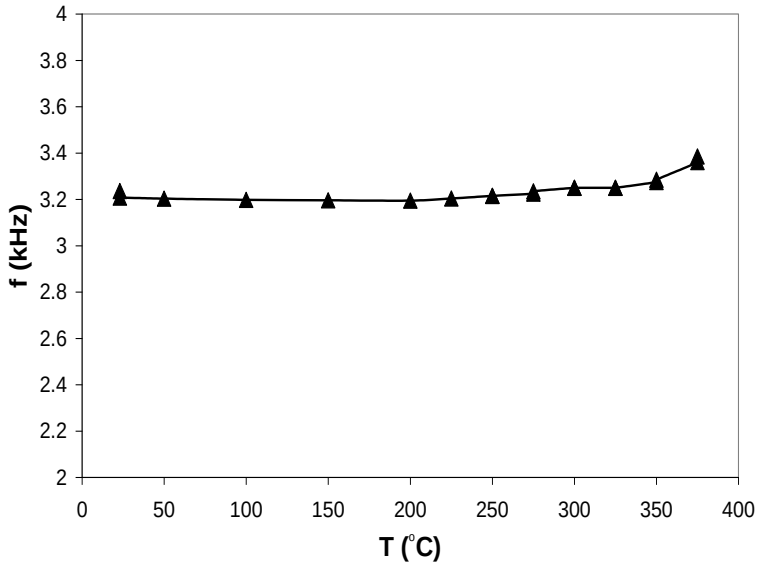
OPAMP based Followers and Inverters



- Follower and inverter based on SOI OPAMP
- Gain of inverter determined by $-R_2/R_1$
- I_{DC}, DC output offset, gain, phase shift, rise time, and noise level measured against temperature and test time
- OPAMP can operate at T>225°C with de-rating

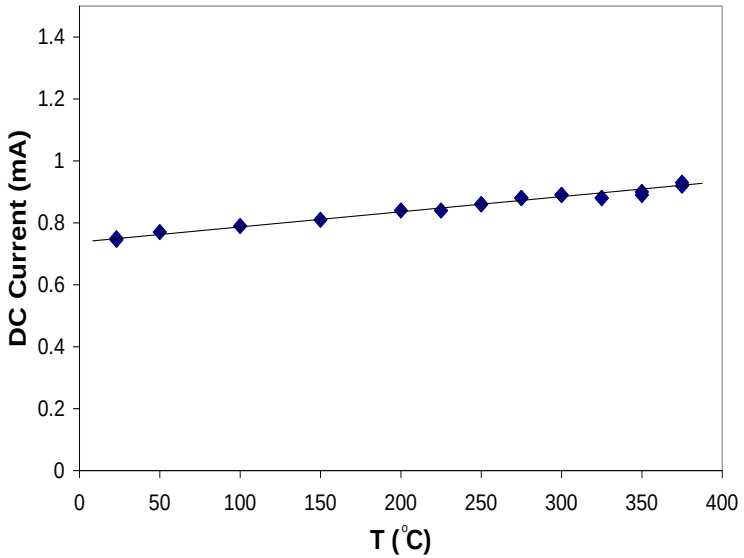
SOI 555 Oscillator Tests Facilitated by High Temperature Packaging

Frequency vs. T



- f shifts from 3.21 kHz to 3.36 kHz as temperature changes from 23°C to 375°C
- After 750 hours operation at 375°C, f shifts to 3.385 kHz
- After testing at elevated temperatures, f is 3.236 kHz at T_R - an increase of 0.87% from the initial frequency before heating

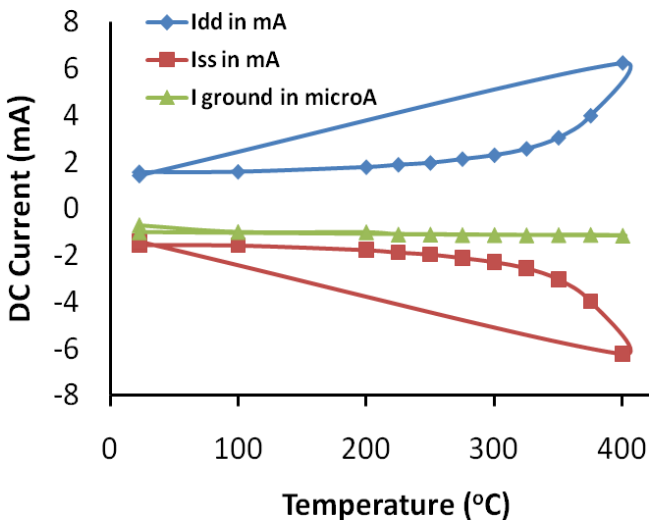
DC Current/Power vs. T



- Oscilloscope input as circuit load
- DC current increases with temperature at an linear rate of ~ 0.5 μA/°C
- DC current at T_R after testing at elevated temperatures is 0.745 mA vs. 0.75 mA initially at T_R
- Temperature dependence of the current is reversible

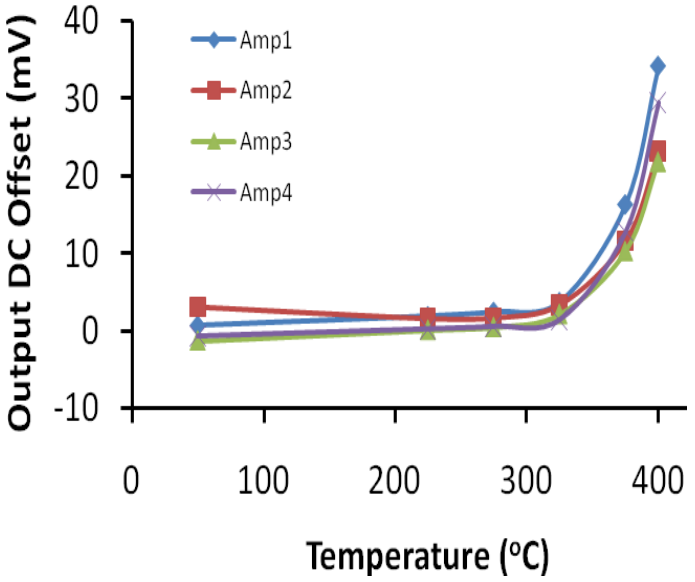
SOI OPAMP Tests Facilitated by High Temperature Packaging

DC Current vs. T



- I_{DD} and I_{SS} are symmetric
- The Ground current < 1.2 μA
- I_{DD} is 1.56 mA at 23°C, 1.88 mA at 225°C, 2.29 mA at 300°C, 3.04 mA at 350°C, 3.98 mA at 375°C, and 6.24 mA at 400°C.
- I_{DD} starts to increase from 325°C
- I_{DD} at 400°C is about 4 times of that at T_R
- Temperature effect recoverable

Output DC Offset vs. T



- T < 325°C: output DC offsets ~ mV
- Offsets increase with T above 325°C
- 400°C: between 22 and 34 mV
- Higher offsets for inverters
- Offsets of inverters ~ R_2/R_1 (gain)
- Offsets recoverable to temperature before the failure

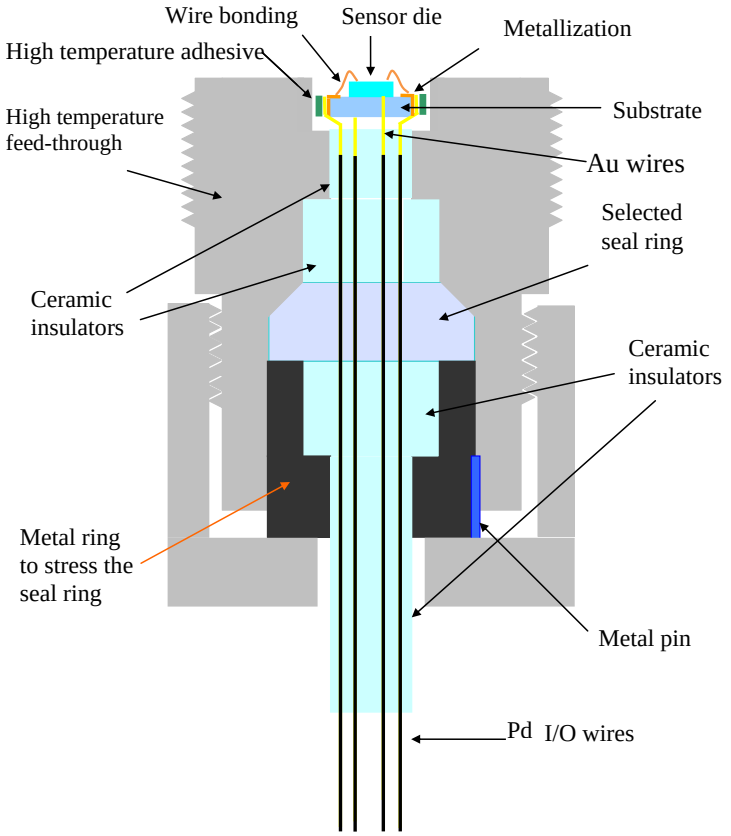
SOI for Operation at T > 225°C – Specifications and Stability

- SOI 555 Timer and OPAMP can operate at T > 225°C with de-rated specifications
- Many commercial SOI digital and analog ICs on market
- SOI ICs are useful to improve the operation temperature from military standard to T>225°C - Distributed Engine Control (DEC) system
- Questions for further investigation:
  - Systematic tests of SOI products at T>225°C facilitated by high temperature packaging
  - SOI IC product specifications vs T (>225°C)
  - Lifetime and thermal stability of de-rated specifications
  - Material level failure mechanisms and process improvement
  - Level I, II, III packaging technologies for commercial applications
- Limited efforts currently underway

Packaging System for SiC Capacitive Pressure Sensors

Spark - Plug Type Package for High Temperature Capacitive Pressure Sensors

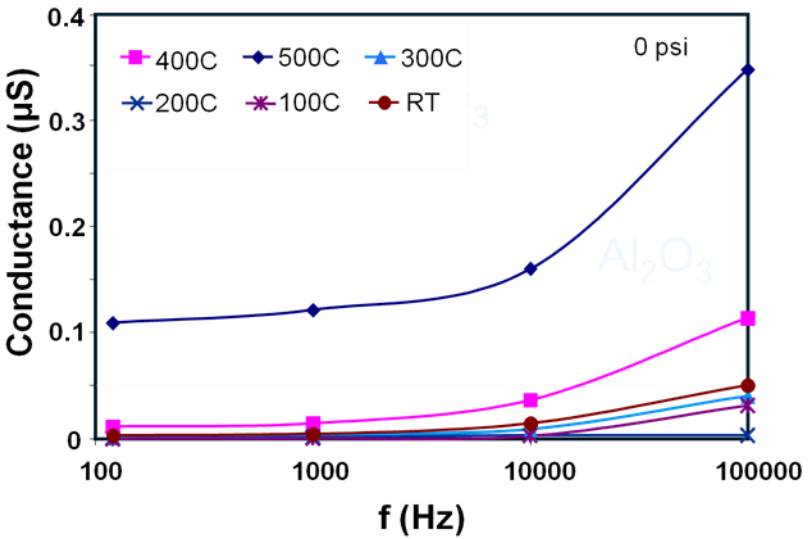
- 96% alumina substrate with Au thick-film metallization
- Four 10 mil diameter Au wires (I/Os) attached
- Au wires extended by four Pd wires
- Pd wires sealed in a commercial SS high temperature gland
- The gland operable up to 8000 psi
- Electrically characterized between RT and 500°C
- Low parasitic effects
- May apply to other micro-fabricated solid sensors



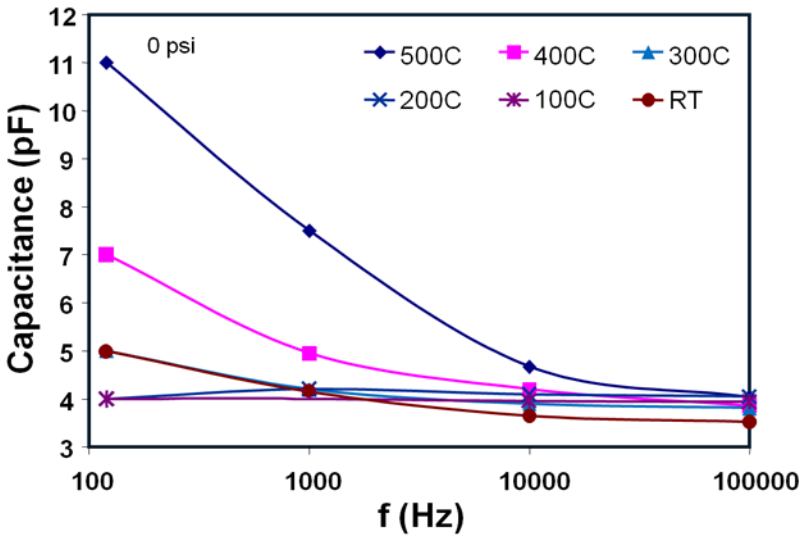
Packaging System for SiC Capacitive Pressure Sensors

Spark-plug Type Package for High Temperature Capacitive Pressure Sensors

Conductance between two wires



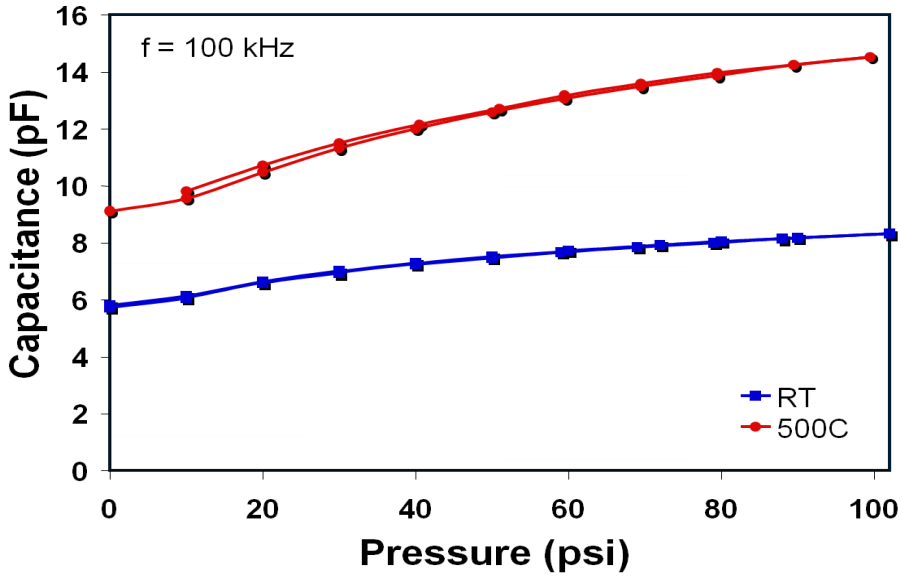
Capacitance between two wires



- Stainless steel sealing gland with LAVA seal
- Wiring configuration: two signal wires with third wire for “shield”
- Low parasitic capacitance at high frequencies > 10 kHz
- No direct impact on capacitance measurement results from parasitic conductance
- Usable for packaging some envisioned high temperature sensors

Packaging System for SiC Capacitive Pressure Sensors

Spark-plug Type Package for High Temperature Capacitive Pressure Sensors

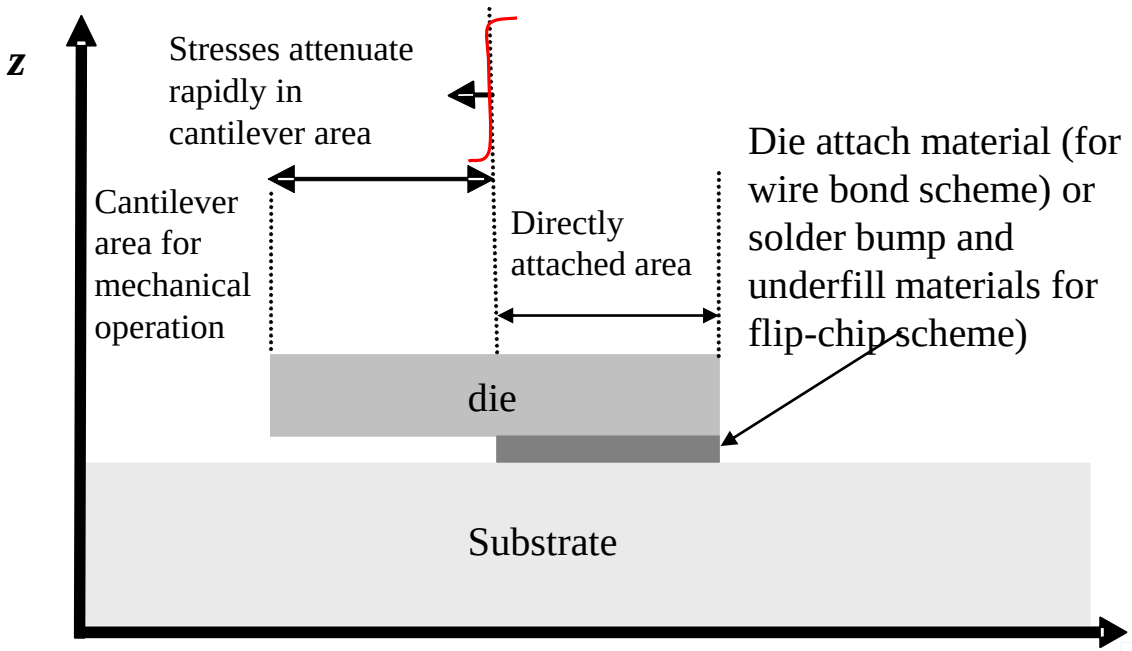


2.5 mm

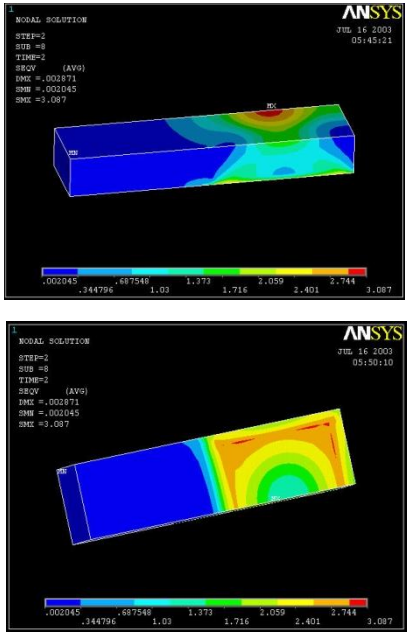
- Capacitive SiC pressure sensor with four polycrystalline SiC diaphragms electrically connected in parallel
- Measured at 100 kHz
- Packaging parasitic effects subtracted
- Parasitic conductance to be further reduced for packaging other sensors

Packaging System for SiC Capacitive Pressure Sensors

Low Stress Die-attach Structure for MEMS Packaging



Side view of lateral stress attenuation



Von Mises Stress contour plot of top and bottom of die

- Cantilever area for mechanical operation, cantilever area is almost stress free

High Temperature Passives

High Temperature Capacitors

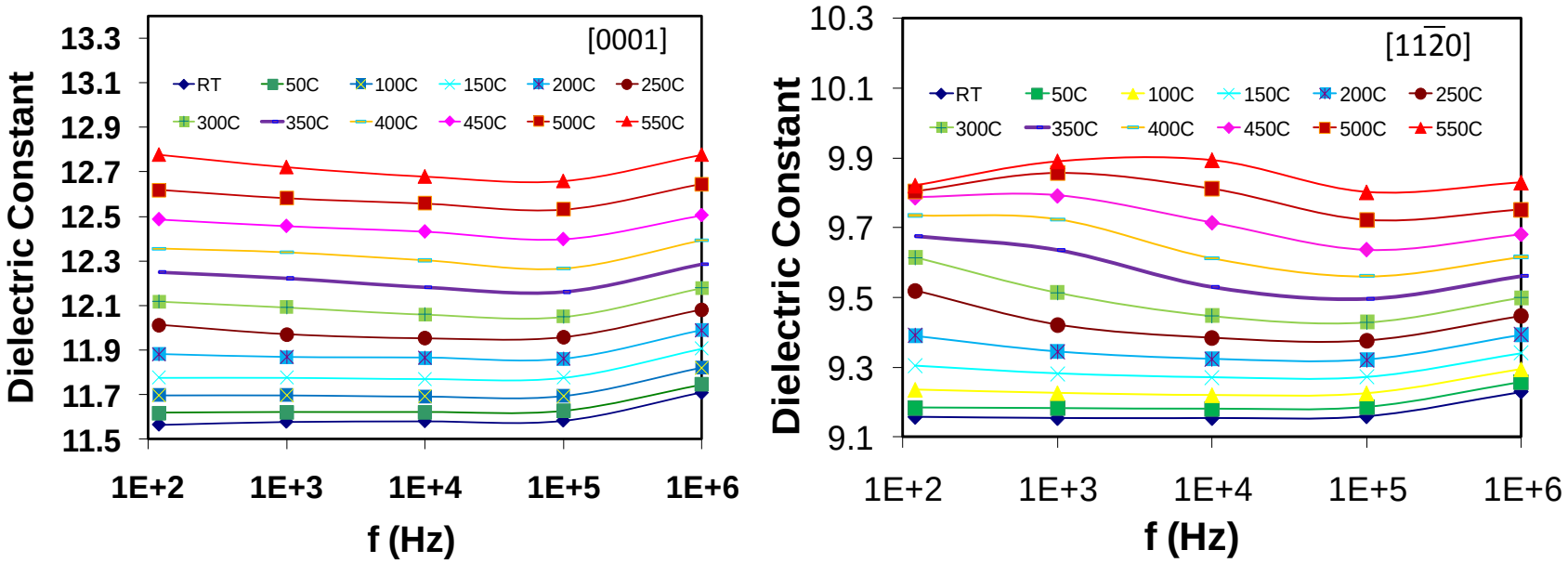
- T >175°C
- Dielectric constants change with temperature
- High dielectric loss at elevated temperature
- Specs are application dependent
- High temperature operable dielectrics
- Component level packaging and integration technologies needed

High Temperature Inductors

- Above limitary standard
- Material magnetic permeability constants change with temperature
- Higher loss at elevated temperature
- Specs are application dependent
- High temperature operable magnetic materials
- Component level packaging and integration technologies needed

High Temperature Dielectric Materials

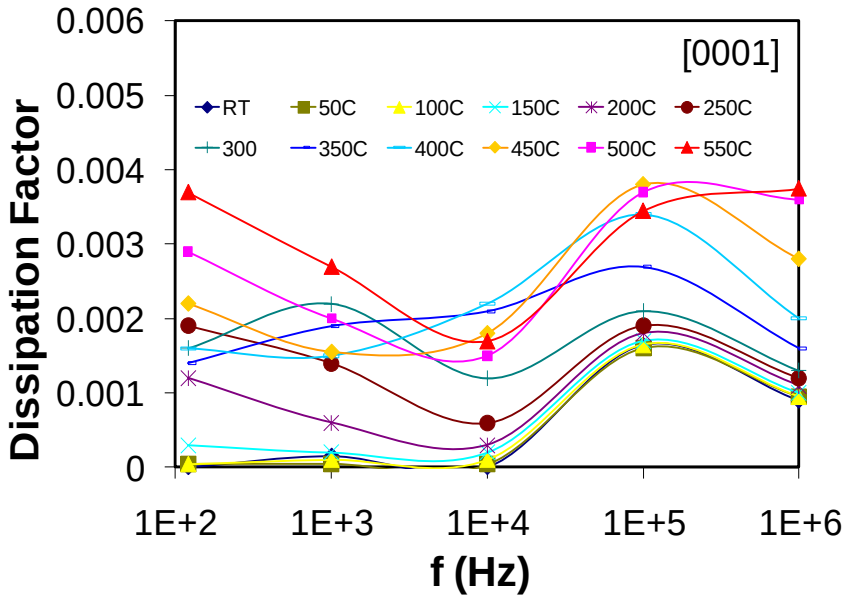
Dielectric Constant of C-face and A-face Sapphire Substrates

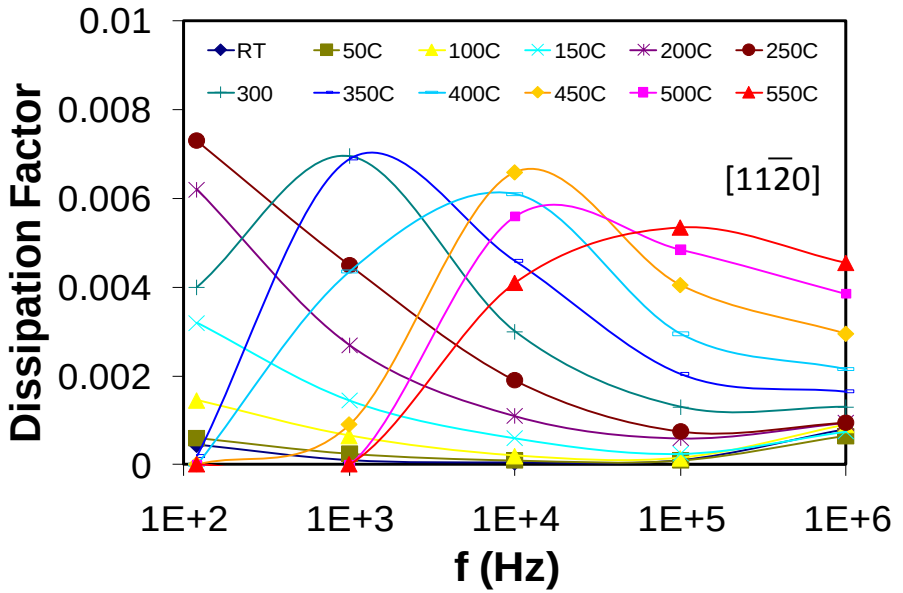


- Both C-face and A-face sapphire, dielectric constant increases monotonically with temperature
- 10.4% changes of C-face, and 7.5% changes of A-face of dielectric constant compared with 174% changes of 96% alumina in the frequency and temperature ranges
- Hard for fabrication

High Temperature Dielectric Materials

Dissipation Factors of C-face and A-face Sapphire Substrates





- The dissipation factor of C-face sapphire is less than 0.004 in the entire test temperature and frequency ranges
- The dissipation factor of A-face sapphire is less than 0.0075 in the entire test temperature and frequency ranges
- Orders of magnitudes improvement compared with ceramic alumina materials

Summary

Ceramic substrates and thick-film metallization based packaging systems demonstrated at 500°C

- Alumina and aluminum nitride packages and PCBs
- Packaged SiC JFET circuits successfully tested for over 10,000 hours at 500°C, over 100 thermal cycle tests between T_R and 500°C conducted
- Tested in *in situ* IIS orbit for 18 months as well as Shuttle flight conditions

Co-fired alumina 32-I/O high temperature package designed, fabricated, electrically characterized

- Tested with SiC integrated circuits at 500 °C, and 700°C for the first time
- DC and AC electrical parasitic parameters of neighboring I/Os of this package characterized between room temperature and 500 °C
- At 500 °C the DC resistance between neighboring I/Os is above 1 GΩ
- AC parasitic capacitance between neighboring I/Os at temperatures T≤ 500 °C in the frequency range from 120Hz and 1MHz is below 1.5pF, and parasitic AC resistance is over 20 MΩ

Commercial SOI digital and analog circuits tested above 225°C facilitated by high temperature packaging

- De-rated applications at T>225°C, below T range for SiC electronics

Summary

A spark-plug type sensor package for 500°C sensors

- Low parasitic effects
- Characterized and tested with a SiC sensor at temperatures up to 500°
- A low stress die-attach structure developed for high temperature MEMS
- This sensor package applies to high temperature and high differential pressure environments
- Limited by time – NASA VIPR II, III on-engine test work not discussed

High temperature passive components

- Needed for both SiC and SOI circuits, and both temperature ranges
- High temperature dielectric and magnetic materials needed
- Sapphire materials demonstrate very stable dielectric constant and low loss, but hard for fabrication
- Component packaging and integration technologies needed

4th "H" for microelectronics research - High temperature harsh environment microelectronics

Thank You Very Much for Your Attention!

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