A Thermal Runaway Failure Model for Low-Voltage BME Ceramic Capacitors with Defects

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Abstract – **Reliability of base metal electrode (BME) multilayer ceramic capacitors (MLCCs) that until recently were used mostly in commercial applications, have been improved substantially by using new materials and processes. Currently, the inception of intrinsic wear-out failures in high quality capacitors became much greater than the mission duration in most high-reliability applications. However, in capacitors with defects degradation processes might accelerate substantially and cause infant mortality failures. In this work, a physical model that relates the presence of defects to reduction of breakdown voltages and decreasing times to failure has been suggested. The effect of the defect size has been analyzed using a thermal runaway model of failures. Adequacy of highly accelerated life testing (HALT) to predict reliability at normal operating conditions and limitations of voltage acceleration are considered. The applicability of the model to BME capacitors with cracks is discussed and validated experimentally.**

Index Terms: **ceramic capacitors, reliability, simulation, thermal runaway, failures.**

I.   INTRODUCTION

Until recently, only precious metal (Ag/Pd alloy) electrode (PME) ceramic capacitors were used in military and aerospace applications. Reliability issues with base (Ni) metal electrode (BME) capacitors that are widely used in commercial applications are mostly due to specifics of their manufacturing. To avoid nickel oxidation, high-temperature procedures are carried out in a reducing atmosphere, which results in increased concentration of oxygen vacancies in the dielectric layers. These structural point defects act as electron donors resulting in formation of positively charged vacancies, V_O^{++}, that act as electron donors, increase conductivity of the dielectric, and reduce insulation resistance (IR) of capacitors. However, the most dangerous, reliability-related consequence of the presence of oxygen vacancies is related to their migration with time under applied voltage resulting in degradation of IR and failures with time of operation.

The mechanism of degradation and failures is attributed to accumulation of V_O^{++} at the grain boundaries and metal/ceramic interfaces resulting in decreasing energy barriers and increasing injection of electrons according to the Schottky mechanism [1, 2]. Most researchers agree that the rate of degradation is controlled by variations of the barrier height at the ceramic/metal interface with time [3-5].

According to this model, current density in the dielectric increases with time and has a tendency to stabilize at levels 2 to 3 orders of magnitude higher than the initial. This behavior was observed in various ceramic [3, 4, 6, 7] and tantalum [8] capacitors and was attributed to concentration polarization of V_O^{++} that are piling-up at the cathode and reduce the barrier height at the metal/dielectric interface from Φ_{B0} initially to a minimal value $\Phi_{B\ min}$ when distribution of oxygen vacancies is stabilized. Zafar and co-workers [4] suggested a stretched exponential dependence of Φ_B with time:

$$\Phi_B(t) = \Delta\Phi_B \times \left[1 - \exp\left(-\left(\frac{t}{\tau_V}\right)^\gamma\right)\right], \qquad (1a)$$

where $\Delta\Phi_B = \Phi_{B0} - \Phi_{B\ min}$, τ_V is the characteristic time and γ is the shape constant.

The characteristic time of the degradation process depends on temperature, T, and applied voltage, V, and can be expressed as [9, 10]:

$$\tau_V = \frac{0.78 \times d^2}{\mu_V \times V} \quad \text{where} \quad \mu_V = \mu_0 \times \exp\left(-\frac{E_V}{kT}\right), \quad (1b)$$

where μ_V is the drift mobility of V_O^{++}, μ_0 is a constant, d is the thickness of the dielectric, E_V (typically from 0.9 to 1.1 eV) is the activation energy of mobility, and k is the Boltzmann's constant.

Using these equations and Schottky model, wear-out processes in ceramic capacitors resulting in degradation of leakage currents can be simulated. The model predicts time to parametric failure caused by reduced IR considering capacitors with homogeneous, defect-free dielectrics. In practice, capacitors might have defects, and catastrophic or short circuit failures are of a greater reliability concern.

Over the years, substantial progress has been made in development of new manufacturing processes and materials so the useful life of capacitors has been increased substantially [11]. Currently, wear-out failures in BME capacitors at normal application conditions are extremely unlikely, which allows their usage in high reliability systems. Experience with precious metal electrode (PME) capacitors shows that failures during applications are mostly related to the presence of defects, in particular, cracks. Our previous studies have shown that the susceptibility of PME and BME capacitors with cracks

to failures in humid environments is different [12]. The objective of this work is to reveal specifics of degradation processes and probability of catastrophic failures in BME capacitors with defects during operation in dry environments such as life test or highly accelerated life test (HALT) conditions.

Studies have shown [13-15] that roughness and presence of voids in metal electrodes result in local field enhancement causing reduction of insulation resistance, which might affect performance of capacitors with thin dielectrics. Electric field in the dielectric is also increased by the presence of various macro defects resulting in thinning of dielectric layers. In this work, a model of failures in BME capacitors with defects has been suggested and thermal runaway processes simulated to assess the effect of external (temperature and voltage) and internal (dielectric thickness and size of defects) factors on the probability of catastrophic failures. Specifics of failures at high temperatures in the presence of cracks have been considered and the applicability of the model discussed.

II. A FAILURE MODEL FOR CAPACITORS WITH DEFECTS

Defects resulting in thinning of the dielectric increase local electric field, thus enhancing migration of V_O^{++} compared to the defect-free areas (see insert in Fig.1). The presence of similar defects has been shown to cause infant mortality (IM) failures in thin dielectric BME capacitors [14]. Note that voids in the dielectric can have the same effect as the thinning if mobile charged species are present on the internal surface of the void. In this case, redistribution of the species would reduce electric field inside the void and increase field in the surrounding areas of the dielectric.

Areas with thin dielectric have lower breakdown voltages (VBR) and can be revealed by analysis of distributions of VBR. Typically, intrinsic breakdown voltages in low-voltage (rated to 200 V and less) BME capacitors have tight distributions and are dozens of times greater than the rated voltage. The low-voltage tail of the distribution can be used to assess the proportion of capacitors with defects, and their severity. An examples of VBR distribution for 50 V BME capacitors that have ~ 20% of parts with defects is shown in Fig.1.a.

The ratio of VBR of a capacitor with defects (VBR_d) and the intrinsic breakdown voltage (VBR_i) indicate the enhancement of the electric field at the defect area. Considering that the empirical Prokopowicz-Vaskas equation for reliability voltage acceleration [16] depends on the ratio of electric fields at accelerated and normal conditions, we can calculate the expected time to failure for a capacitor with a given breakdown voltage:

$$TTF = TTF_0 \times \left(VBR_d \middle/ VBR_i \right)^n , \qquad (2)$$

where n is the voltage acceleration constant, TTF_0 is the intrinsic time to failure in a defect-free capacitor. For estimations, we can assume that during life test conditions (125°C, 100 V) $TTF_0 = 10,000$ hr. For PME capacitors $n \approx 3$,

and for BME capacitors this parameter is greater, $3 < n < 9$ [2, 17].

Calculated distributions of *TTF* for capacitors with different values of n are shown in Weibull coordinates in Fig.1b. Note that capacitors with intrinsic breakdown voltages had shape parameter $\beta > 20$, which indicates wear-out failures, whereas capacitors with defects had $\beta < 1$ indicating IM failures.

According to this model, the same degradation process that is responsible for intrinsic wear-out failures might result in IM failures for capacitors having defects. In this case, voltage and temperature reliability acceleration factors that are determined for wear-out failures might be used also to predict IM failures.
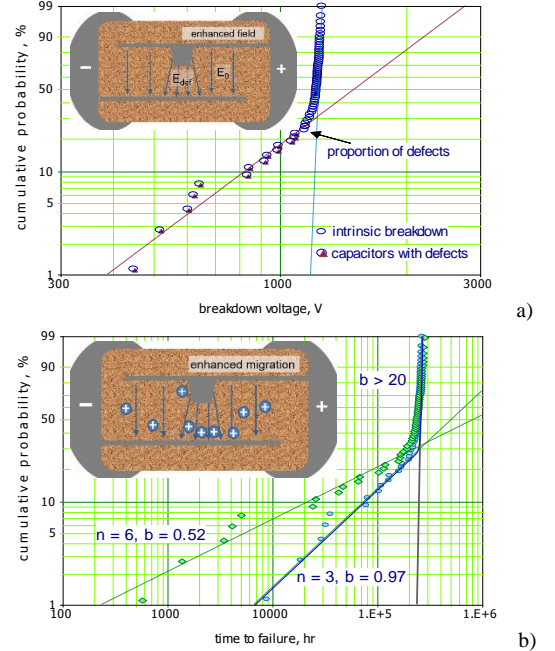

Figure 1. Distribution of breakdown voltages for 0.12 μF 50 V capacitors (a) and distributions of times to failure calculated per Eq.(1) at $n = 3$ and $n = 6$ (b). The values of β indicate slopes of the relevant Weibull distributions. Inserts show schematics of the defect-related breakdown (a) and failure mechanism (b).

III. THERMAL RUNAWAY MODEL

Enhanced electric field at the defect areas accelerates accumulation of oxygen vacancies at electrodes at the defect thus increasing current density with time of operation. This raises the local temperature of the defect resulting in formation of hot spots. At certain conditions the power generated by the current in the defect, P_{gen}, might be balanced by the power dissipated by thermal conduction, P_{dis}, resulting in stabilization of the leakage current and hot spot temperature. For a catastrophic failure to occur P_{gen} should remain greater than P_{dis} in the heating process.

Catastrophic failures caused by the thermal runaway happen when temperature at the defect site rises to a level exceeding melting temperatures of metals (1455 °C for Ni) and/or sintering temperature of ceramics (~1250 °C). For simplicity, and to get conservative estimations in the following analysis, we assume that catastrophic failures occur when temperature of the hot spot exceeds 1000 °C.

Let us consider a thinning-of-dielectric defect in a capacitor with a nominal thickness of the dielectric layer d and thickness of metal electrodes t (see Fig. 3a). Assuming that the defect has a cylindrical shape with a radius r and height $l = \alpha \times d$, the thickness of the dielectric at the defect site, $h = (1-\alpha) \times d$, where α is a relative height of the defect. The electric field at the defect $E_d = E_0/(1-\alpha)$, where E_0 is the field at defect free areas. Typically, the values of d for 50 V BME capacitors are in the range from 6 to 16 μm, and for 10 V capacitors it can be few micrometers only.

For a capacitor operating at a voltage V, the power generated at the defect site is $P_{gen} = I_d \times V$, where the current through the defect area can be determined as

$$I_d(T, E_d) = \pi \times r^2 \times J_d(T, E_d) \, , \qquad (3)$$

The power that is dissipated through thermal conductivity of ceramic and metal electrodes, P_{dis} is proportional to the temperature rise, $P_{dis} = (T-T_0)/R_\theta$, where R_θ is the thermal resistance of the defect, and T_0 is the environmental temperature. The difference between P_{gen} and P_{dis} increases temperature of the hot spot:

$$C \times \frac{dT}{dt} = \pi \times r^2 \times J_d(T, E) \times V - \frac{T-T_0}{R_\theta} \, , \qquad (4)$$

where $C = \pi \times r^2 \times d \times \rho \times c_p$ is the heat capacity of the defect, ρ = 5800 kg/m³ is the density, c_p = 420 J/kg_K is the specific heat capacity of the ceramic.

Leakage currents in capacitors.

The current density through a dielectric layer that is controlled by electron injection over a metal/dielectric barrier can be described using the Schottky/ Simmons model [18]:

$$J_S = AT^{3/2} \mu E \exp\left(-\frac{\Phi_B}{kT}\right) \exp\left(\frac{\beta_s E^{0.5}}{kT}\right), \qquad (5)$$

where A is a constant, μ is the mobility of electrons in the dielectric, E is the electric field in the dielectric, and β_s = 2.7×10^{-24} C× (m×V)$^{0.5}$ is the Schottky constant.

To validate the applicability of Eq.(5) for thermal runaway calculations, leakage currents in various types of 0.33 μF, 50 V capacitors were measured at different temperatures and voltages. An example of these measurements for a capacitor having dielectric thickness d = 12 μm and total surface area of electrodes 1.1 cm² are shown in Fig.2a. Results of the measurements have been approximated by Eq.(5) with an empirical adjustment of parameters A and μ. By assuming $A \times \mu$ = 0.00385 A×(V×K$^{3/2}$×m)$^{-1}$ Eq.(2) provides a good fit to the experimental data.

According to the Schottky/Simmons model, activation energy of conductivity is decreasing with applied field as $E^{0.5}$ at a constant rate β_s/kT = 0.034 eV×(μm/V)$^{0.5}$. Experimental data for different types of PME and BME capacitors (Fig. 2b) are in a reasonable agreement with the model and indicate values for the barrier heights, $\Phi_B \approx$ 0.75 eV for BME and $\approx$ 1.35 eV for PME capacitors. This difference explains substantially lower leakage currents, hence a lower probability of thermal runaway failures, in PME compared to BME capacitors.
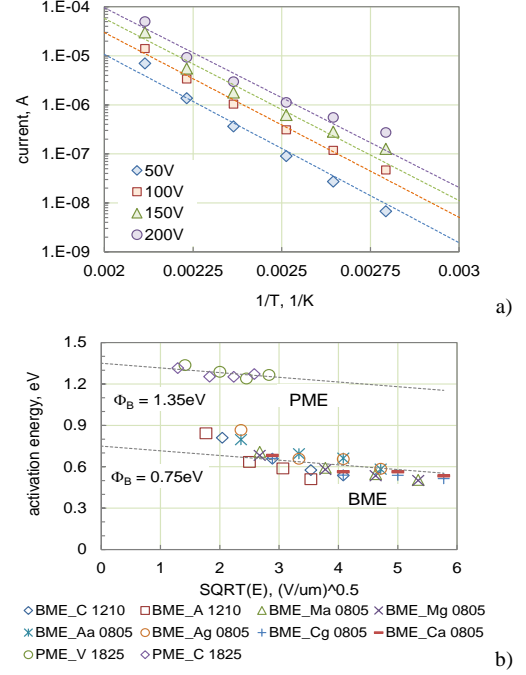

Figure 2. Temperature dependence of leakage currents in 0.33 μF 50 V BME ceramic capacitors at different voltages (a) and variations of activation energy with electric field for different types of 0.33 μF 50 V BME and PME capacitors. Marks indicate experimental data and dashed lines calculations per Eq.(5)

Combining Eq.(1) and Eq.(5), degradation of leakage currents with time can be simulated for a defect-free capacitor. In the presence of defects, processes in the defect areas should be simulated separately because current density in these areas might increase to much greater levels compared to defect-free areas. Depending on the power balance at the defect, degradation might either stabilize resulting in increased leakage currents that might cause parametric failures, or in a catastrophic failures due to thermal runaway. Analysis below determines conditions for catastrophic failures.

Thermal resistance of defects.

Let us consider a cylindrical shape of the defect shown in Fig.3a. The heat generated in this defect is released by thermal conductivity of ceramic from the top, bottom, and side surfaces of the cylinder, and by the thermal conductivity of metal along the electrodes (see Fig. 3b). The relevant thermal resistances $R1$, $R2$, and $R3$ can be calculated assuming that the temperature of the cylinder is constant, and temperature at a distance L from the defect remains stable and equal to T_0. At these conditions:

$$R_1 = \frac{1}{8 \times r \times \lambda_c}, \quad R_2 = \frac{\ln\left(L/r\right)}{4 \times \pi \times t \times \lambda_{Ni}}, \quad R_3 = \frac{\ln\left(L/r\right)}{2 \times \pi \times (1-\alpha) \times d \times \lambda_c}, \quad (6)$$

where λ_c = 2.7 W/(m×K) and λ_{Ni} = 90.9 W/(m×K) are thermal conductivities of the ceramic and nickel.

Note that $R1$ and $R2$ are combined resistances at both sides of the cylinder. Considering relatively small sizes of the defects, $R1$ was calculated as for a contact of a disc of radius r to a semi-infinite ceramic.

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For conservative estimations, we can assume that L is about the size of the chip, ~ 1 mm. As an example, Fig.3c shows thermal resistances calculated per Eq.(6), as well as the total resistance, $R_\theta = (1/R1+1/R2+1/R3)^{-1}$ as a function of the defect size, r, at $d = 12$ μm, $t = 1$ μm and different values of α. Note that R_θ has a relatively weak dependence on L and α, so some variations in L and defect's height would not change thermal resistance substantially. Also, because at small sizes of the defects heat dissipation occurs mostly via metal electrodes, and resistance $R3$ is relatively large, the effect of the height of the defect ($\alpha \times d$) on the total resistance is negligible.
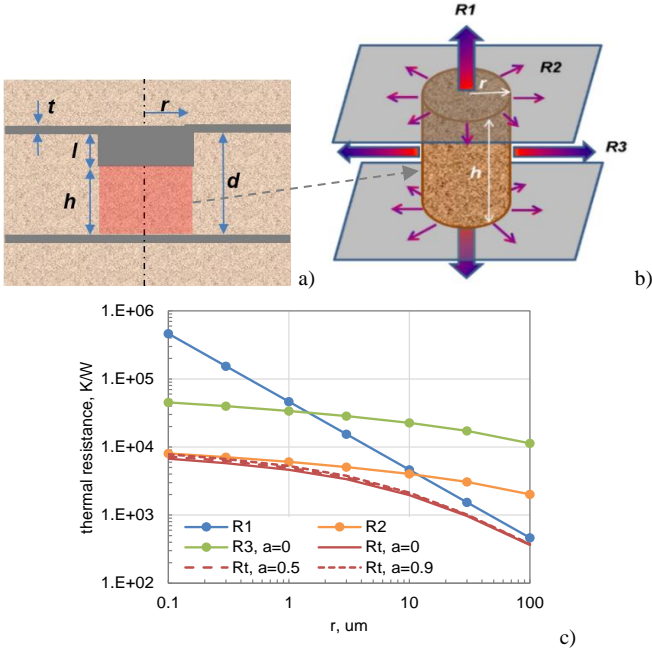

Figure 3. Schematic of a defect in the dielectric (a), heat release (b), and variation of the thermal resistances with the size of the defect for a BME capacitor with different values of α at $d = 12$ μm, $t = 1$ μm (c).

Variations of hot spot temperature with time.

Eq.(4) cannot be solved analytically, but allows for numerical solutions. Fig.4 shows examples of variations of the hot spot temperature with time during HALT calculated for different test conditions. The temperature increases rather fast, and the rate of heating corresponds to the characteristic time of the process that can be estimated as $\tau = R_\theta \times C$. At $d = 12$ μm and $r = 10$ μm $\tau \approx 11$ μsec and at $d = 3$ μm and $r = 3$ μm $\tau \approx 0.4$ μsec.

Simulations have been made for barrier heights decreasing as a result of degradation from $\Phi_B = 0.75$ eV initially to the level at which thermal runaway starts. It is seen that thermal runaway occurs at a certain critical level of Φ_{Bcr} and the difference between the stable conditions and conditions that result in catastrophic failures is less than 1 meV.

If Φ_{Bcr} is low, the concentration and mobility of oxygen vacancies might be not large enough to reduce Φ_B below the critical level. The probability of catastrophic failures can be characterized by Φ_{Bcr}: the greater Φ_{Bcr} the greater the probability of catastrophic failures. The value of Φ_{Bcr} depends on both, internal and external factors and will be analyzed in the following section.
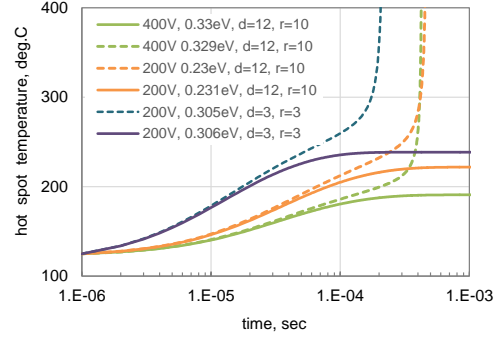

Figure 4. Variations of the hot spot temperature for cases when temperature is stabilizing (solid lines) and thermal runaway (dashed lines) for 50 V capacitors at 125 ºC. The legend shows the applied voltage, barrier height Φ_B, thickness of the dielectric d, and radius of the defect r in μm. In all cases, the relative height of the defect $\alpha = 0.5$.

IV. RESULTS OF SIMULATION AND DISCUSSION

Typically, degradation of leakage currents caused by migration of oxygen vacancies increases currents 2 to 3 orders of magnitude. For example, IR in barium strontium titanate (BST) capacitors during HALT at 280 ºC increased currents more than two orders of magnitude which was attributed to a decrease of Φ_B, from 0.63 eV to 0.46 eV [4].

According to Eq.(5), for leakage currents at 125 °C to increase by three orders of magnitude, the value of Φ_B should decrease from 0.75 eV to $\Phi_{B\ min}$ ~0.5 eV. Due to lateral diffusion from the periphery, concentration of V_O^{++} at the cathode at a defect can be greater than in defect-free areas of the dielectric thus allowing much greater increase of currents. For estimations, we can assume that the current density in the defect area increases 4 to 5 orders of magnitude. This decreases the minimal value of Φ_B at the defect to $\Phi_{B\ min}$ ~ 0.3 eV. Although the value of $\Phi_{B\ min}$ at defects is difficult to assess accurately, factors affecting the probability of catastrophic failures still can be analyzed considering that the lower Φ_{Bcr}, the less likely the probability of failure.

The hot spot temperatures for different internal and external conditions were determined using Eq.(4) and Eq.(5) at decreasing Φ_B with 5 meV increments until the hot spot temperature reaches the critical level of 1000 °C.

Variations of Φ_{Bcr} with the size of defect r for capacitors with different thickness of the dielectric $d = 12$, 6, and 3 μm tested at 125 °C and 200 V are shown in Fig.5. As expected, Φ_{Bcr}, hence the probability of failures, increases with the size of defects and is much greater in thin than in thick dielectric capacitors. At the same relative height of the defect $\alpha = 0.5$, catastrophic failures in capacitors with $d = 3$ μm might happen even at r~ 4 μm, whereas the size of defects should be more than 10 μm at $d = 6$ μm and more than 40 μm at $d = 12$ μm.

Thermal runaway failures do not occur even for defect sizes ~100 μm unless degradation of the barrier height to below 0.5 eV happens. Analysis of leakage currents shows that similar capacitors might even not fail parametrically. Obviously,

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capacitors that employ better quality dielectrics with a smaller concentration of oxygen vacancies can tolerate larger sizes of defects.

Degradation processes in capacitors depend on the electric field in the dielectric rather than on applied voltage. If the stress voltage would decrease proportionally to d (constant E and α conditions in Fig.5), the effect of dielectric thickness would be different and the situation would be reversed compared to testing at constant voltages. At constant E, capacitors with $r = 10$ and $\alpha = 0.5$ would have Φ_{Bcr} decreasing from 0.22 eV to 0.16 eV as d decreases from 12 μm to 3 μm. However, at V = const. for the same conditions Φ_{Bcr}, hence the probability of failures, would increase from 0.22 eV to 0.39 eV.
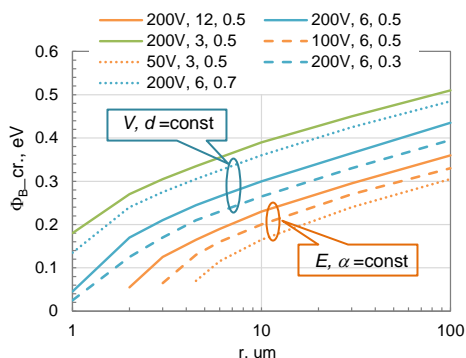

Figure 5. Effect of the defect size on the critical value of the barrier height for 50 V BME capacitors during life testing at 125 ºC. The legend indicates the test voltage, thickness of the dielectric d in μm and relative height α.

Because rated voltages of capacitors are not directly related to the dielectric thickness that might vary up to 3 times for capacitors rated to the same voltage, the probability of failures and reliability acceleration factors determined by the ratio of test and rated voltages cannot be used to compare results of HALT in parts with different thickness of the dielectric. For the same reason, voltage derating requirements for capacitors rated to the same voltage but having different thickness of the dielectric should be different.

Typically, HALT for ceramic capacitors is carried out at voltages up to 10 times the rated voltage and temperatures from 125 ºC to 200 ºC. Results of simulation of HALT at these conditions for 50 V capacitors with dielectric thickness $d = 6$ μm and defect height $l = 3$ μm ($\alpha = 0.5$) are shown in Fig.6. At a constant temperature, increasing test voltages raises Φ_{Bcr} substantially. For example, at $r = 30$ μm increasing voltage from 100 V to 500 V raises Φ_{Bcr} from 0.26 eV to 0.52 eV. Considering that for normal quality parts degradation is unlikely to decrease Φ_B to below ~ 0.5 eV, this means that testing capacitors at 125 ºC and 500 V would cause catastrophic failures that would never happen at lower voltages.

Increasing temperature from 100 ºC to 200 ºC during testing at 200 V results in relatively minor changes in Φ_{Bcr}. For example, for a defect with radius 10 μm, Φ_B increases from 0.29 eV at 100 ºC to 0.33 eV at 200 ºC. This means that within a typical range of voltage and temperature conditions during

HALT, increasing voltage is more likely to introduce new failure modes and cause failures in capacitors having small size defects that would not occur at voltages close to the operational. Acceleration of life testing by increasing temperature would assure more adequate conditions compared to acceleration by voltage. This is in agreement with data presented by Shiota et. al. [19], according to which acceleration at high voltages might result in errors of extrapolation to operating conditions, and acceleration by temperature is preferable to acceleration by voltage. Similar results were also reported by Randall et al. [2].
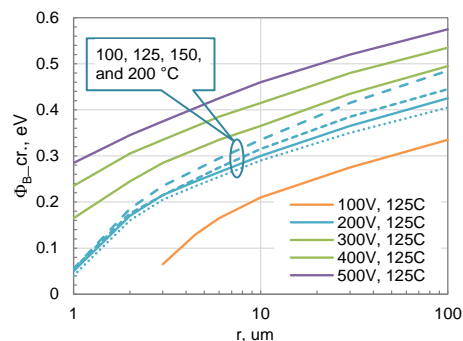

Figure 6. Effect of defect size on Φ_{Bcr} for BME capacitors with $d = 6$ μm and $\alpha = 0.5$ during HALT at different voltages and temperatures. Dashed lines correspond to simulations at 200 V and different temperatures from 100 ºC (bottom blue line) to 200 ºC (top blue line).

Note that PME capacitors have much lower leakage currents and much lower probability of thermal breakdown. Failures in these parts are likely due to the time dependent dielectric breakdown (TDDB) caused by generation of traps in the dielectric. According to the percolation model, breakdown occurs when concentration of defects reaches the critical level [20]. During breakdown, the energy stored in the part is released instantaneously resulting in adiabatic overheating and melting of a local area of the dielectric. For example, dielectric thickness for a typical 50 V PME capacitor is $d \approx 25$ μm. To heat up a sphere of ceramic of radius $r \sim d$ to 1000 ºC, energy of $\sim 1.5 \times 10^{-4}$ J is required. A 0.33 μF capacitor charged to 100 V would have energy about an order of magnitude greater, so instantaneous discharge of the part can cause catastrophic failure. Contrary to PME, degradation in BME capacitors occurs gradually and energy generated at the defect can be balanced by heat dissipation. This explains why "leaky" BME capacitors often degrade, but do not fail catastrophically, whereas PME capacitors with prevailing avalanche-like breakdown [21] might not degrade, but fail short circuit.

V. FAILURE MODEL FOR BME CAPACITORS WITH CRACKS

Analysis above is related to defects that can be presented as a local thinning of the dielectric. Another types of defects that are typical in ceramic capacitors are cracks and delaminations. To assess the effect of cracking on degradation in MLCCs during life testing, different types of 50 V BME capacitors (0.33 μF from manufacturers A and C and 1 μF from manufacturer A) were tested at 125 ºC and 100 V. Each type had two subgroups, one with virgin capacitors, and another

with capacitors having cracks introduced by Vickers indenter.

Results of testing are shown in Fig.7. Virgin 0.33 µF capacitors from two manufacturers remained stable during 100 hours of testing, whereas a certain level of degradation was observed in 1 µF capacitors after ~ 20 hours. Capacitors with cracks had low and stable currents up to a few hours, but after that leakage currents increased substantially, more than two orders of magnitude in some cases. All parts with cracks had a trend to current stabilization after dozens of hours of testing.
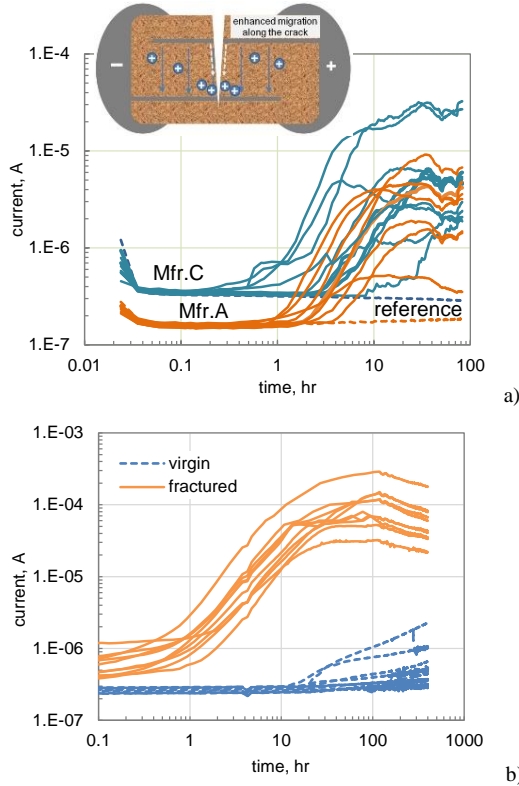

Figure 7. Results of testing at 125 °C, 100 V for 0.33 µF, 50 V (a) and 1 µF, 50 V (b) BME capacitors. Dashed lines correspond to virgin capacitors, and solid lines to capacitors with cracks introduced by Vickers indenter. An insert shows a schematic of degradation process in capacitors with cracks.

To explain this behavior, we can use the model of degradation developed above with some modifications. In the presence of fine cracks crossing electrodes, the electric field might not change substantially. However, ionic diffusion/migration along the surface of the crack occurs faster than in the bulk of the dielectric layer. This facilitates accumulation of V_O^{++} at local areas of metal electrodes near the crack, and accelerates degradation of leakage currents.

After reaching the ceramic/electrode interface, oxygen vacancies can diffuse along the interface thus charging areas close to the crack and reducing the barrier height at metal/ceramic interface. The degradation process can be simulated by reducing Φ_B at the electrode areas close to the crack as for the case with thinning of the dielectric. Similar to results discussed above for small size defects, relatively minor cracking with sizes of a few micrometers might increase leakage currents during HALT, but not cause catastrophic failures.

Due to the thermal nature of breakdown in low-voltage BME capacitors, degradation caused by migration of oxygen vacancies after HALT not only increases leakage currents, but should also reduce breakdown voltages. According to this mechanism, capacitors with defects should have reduced VBR after HALT to a much greater degree compared to the defect-free capacitors. To verify this prediction, breakdown voltages were measured using four groups of BME 0.33 µF, 50 V capacitors. The first group (60 pcs.) was measured using virgin, as received samples, the second (15 pcs.) after cracking introduced by Vickers indenter, the third (10 pcs.) virgin samples after HALT at 175 °C 200 V for 100 hr, and the forth (9 pcs.) using samples with cracks after HALT at 125 °C. Results of this testing are shown in Fig.8.
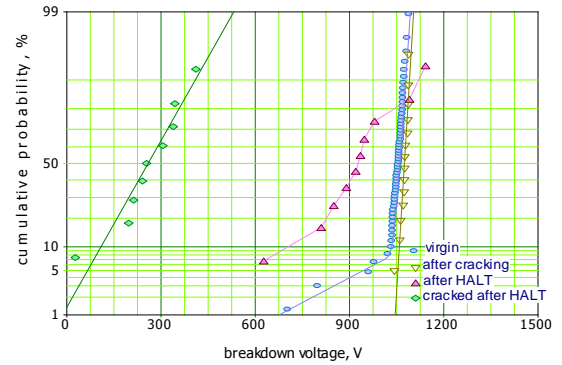

Figure 8. Distributions of breakdown voltages in 0.33 µF, 50 V BME capacitors measured on different groups of parts initially, after introducing cracks, and after HALT.

Distributions of VBR for virgin capacitors have a low-voltage tail indicating the presence of ~ 7% of capacitors with defects that might have been caused by thinning of metallization. However, the spread of the tail was not significant, and VBR remained greater than 50% of the intrinsic breakdown (~1050 V). Introduction of cracks did not affect the distribution of VBR initially, which is in agreement with our earlier study [22] and confirms that fine cracks do not increase electric field in the dielectric substantially. However, as expected, breakdown voltages after HALT reduced more than 3 times, from ~ 1050 V on average initially to ~ 300 V after testing. Some decrease in VBR (to ~ 900 V) as a result of HALT was observed even for virgin samples; however, these samples have been degraded by HALT at 200 V and much higher temperature (175 °C) than the cracked samples. Note, that only one out of 9 capacitors with cracks had VBR after HALT below the rated voltage, while the rest had acceptable electrical characteristics.

Current degradation presented in Fig.7 was simulated by using Eq.(1) and Eq.(4) for capacitors with $d = 6$ µm operating at 100 V and 125 °C. It was assumed that for virgin capacitors degradation resulted in decreasing Φ_B from 0.75 eV to 0.65 eV ($\Delta\Phi_B = 0.1$ eV). The characteristic time $\tau_V = 200$ hr, which corresponds to a mobility of oxygen vacancies of $\mu_V \sim 5\times10^{-15}$ cm²/Vs, and $\gamma = 0.7$. The cracking affected area was assumed to correspond to a cylinder with a radius $r = 25$ µm. Because

cracking does not increase electric field at the defect $\alpha = 0$. Due to accelerated migration along the crack the characteristic time is expected ~10 hr (μ_V ~10^{-13} cm^2/Vs). Extrapolation of data for temperature dependence of mobility of oxygen vacancies presented in [9] to 125 ºC results in μ_V ~3×10^{-14} cm^2/Vs, which is within the range of values accepted for this modeling.

At these conditions, calculations show that the critical value of the barrier height corresponds to $\Delta\Phi_{Bcr}$ = 0.54 eV. Simulations of current degradation have been made for $\Delta\Phi_B$ = 0.45 eV and 0.55 eV. In the first case, leakage currents are stabilizing after ~100 hr at a level of ~100 μA, whereas in the second case a catastrophic failure happens after ~50 hours of testing. Comparison of results in Fig. 7 and Fig.9 show that the modeling is in a reasonable agreement with experimental data. The fact that catastrophic failures were not observed in capacitors with cracks is most likely due to a required severe degradation of the barrier that is unlikely to happen for normal quality parts.
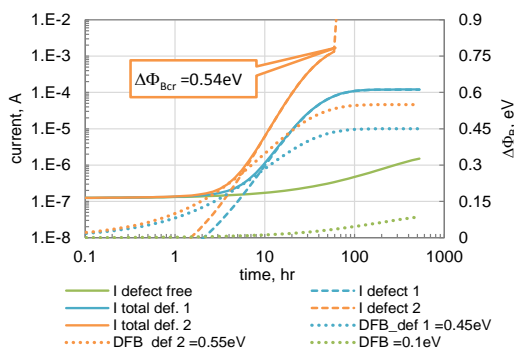

Figure 9. Degradation of leakage currents (solid lines) and barrier heights (dotted lines) simulated for a defect-free capacitor at $\Delta\Phi_B$ = 0.1 eV and τ_V = 200 hr and capacitors with defects (r = 10 μm, α = 0) at τ_V = 10 hr and $\Delta\Phi_B$ = 0.45 eV, case 1 – temperature stabilization, and $\Delta\Phi_B$ = 0.55 eV, case 2 – thermal runaway.

VI. Conclusion

1.   Defects in low-voltage BME capacitors can be revealed by analysis of distributions of breakdown voltages. A simple model based on Prokopowicz-Vaskas equation shows that degradation processes that cause wear-out failures can also result in IM failures in capacitors with defects.

2.   In the presence of defects, migration of oxygen vacancies towards the cathode is enhanced either by increased electric field at the defect area, as in case of thinning of the dielectric, or by increased mobility of oxygen vacancies, as in case of cracks. In either case, accumulation of positively charged vacancies at local areas results in increased leakage currents and formation of hot spots.

3.   A thermal runaway model for capacitors with defects has been suggested. According to the model, catastrophic failures occur when the barrier height decreases below a certain critical level Φ_{Bcr} that depends on external (temperature and voltage) and internal (size of defect, thickness of dielectric and metallization) factors. The greater Φ_{Bcr} the greater the

probability of catastrophic failures. For capacitors with dielectric thickness above 3 μm, having small, micrometer-size defects, Φ_{Bcr} is low so these defects are very unlikely to cause catastrophic failures.

4.   Because rated voltages are not related directly to the thickness of the dielectric, electric field in the dielectric, rather than applied voltage should be considered to analyze HALT results. Decreasing thickness of the dielectric might increase or decrease the probability of catastrophic failures depending on whether the testing is carried out at constant voltage or constant field conditions.

5.   In the range of typical HALT conditions (temperatures from 125 ºC to 200 ºC and voltages up to 10 times the rated voltage), voltage increases the probability of catastrophic failures to a greater degree compared to temperature. Small size defects that would not cause failures at normal operating conditions can result in short circuit failures during testing at increased voltages. The risk of overstressing during HALT by increasing voltages is greater than by increasing temperatures.

6.   Experiments with 50 V BME capacitors show that leakage currents in capacitors with cracks can increase during testing at 125 ºC and 100 V by more than two orders of magnitude, but stabilize or decrease with time after dozens of hours of testing, so no catastrophic failures happen. These parts after testing had also substantially reduced breakdown voltages compared to capacitors without cracks. Both results are in agreement with the suggested model that assumes accelerated transport of oxygen vacancies along the cracks.

7.   Low-voltage BME capacitors with defects are more likely to fail parametrically, whereas catastrophic failures are more probable for PME capacitors, which is attributed to different mechanisms of breakdown for PME (electronic) and BME (thermal) capacitors.

VIII. References

[1] W. Liu and C. A. Randall, "Thermally Stimulated Relaxation in Fe-Doped SrTiO3 Systems: II. Degradation of SrTiO3 Dielectrics," *Journal of the American Ceramic Society,* vol. 91, pp. 3251-3257, Oct 2008.

[2] C. A. Randall, R. Maier, W. Qu, K. Kobayashi, K. Morita, Y. Mizuno*, et al.*, "Improved reliability predictions in high permittivity dielectric oxide capacitors under high dc electric fields with oxygen vacancy induced electromigration," *Journal of Applied Physics,* vol. 113, pp. 1011-1016, 2013.

[3] T. Baiatu, R. Waser, and K. H. Hardtl, "DC electrical degradation of perovskite-type titanates. 3. A model of the mechanism," *Journal of the American Ceramic Society,* vol. 73, pp. 1663-1673, Jun 1990.

[4] S. Zafar, B. Hradsky, D. Gentile, P. Chu, R. E. Jones, and S. Gillespie, "Resistance degradation in barium strontium titanate thin films," *Journal of Applied Physics,* vol. 86, pp. 3890-3894, 1999.

[5] S. Takeoka, K. Morita, Y. Mizuno, and H. Kishi, "Thermally stimulated current (TSC) studies on resistance degradation of Ni-MLCC," *Ferroelectrics,* vol. 356, pp. 370-376, 2007.

[6] E. Bouyssou, R. Jérisian, N. Cézac, P. Leduc, G. Guégan, and C. Anceau, "Wafer level reliability and leakage current modeling of PZT capacitors," *Materials Science and Engineering: B,* vol. 118, pp. 28-33, 2005.

[7] S. Zhao, S. J. Zhang, W. Liu, N. J. Donnelly, Z. Xu, and C. A. Randall, "Time dependent dc resistance degradation in lead-based perovskites: 0.7 Pb(Mg1/3Nb2/3)O-3-0.3 PbTiO3," *Journal of Applied Physics,* vol. 105, Mar 1 2009.

[8] A. Teverovsky, "Degradation of leakage currents in solid tantalum capacitors under steady-state bias conditions," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 752-757.

[9] F. E. Kamel, P. Gonon, L. Ortega, F. Jomni, and B. Yangui, "Space charge limited transient currents and oxygen vacancy mobility in amorphous BaTiO3 thin films," *Journal of applied physics,* vol. 99, pp. 094107-1-5, 2006.

[10] S. Zafar, R. E. Jones, B. Jiang, B. White, P. Chu, D. Taylor, *et al.*, "Oxygen vacancy mobility determined from current measurements in thin Ba0.5Sr0.5TiO3 films," *Applied Physics Letters,* vol. 73, pp. 175-177, Jul 1998.

[11] H. Kishi, Y. Mizuno, and H. Chazono, "Base-metal electrode-multilayer ceramic capacitors: Past, present and future perspectives," *Japanese Journal of Applied Physics Part 1,* vol. 42, pp. 1-15, Jan 2003.

[12] A. Teverovsky and J. Herzberger, "Humidity Testing of PME and BME Ceramic Capacitors with Cracks," in *CARTS International*, Santa Clara, CA, 2014, pp. 15-29.

[13] M. M. Samantaray, A. Gurav, E. C. Dickey, and C. A. Randall, "Electrode Defects in Multilayer Capacitors Part I: Modeling the Effect of Electrode Roughness and Porosity on Electric Field Enhancement and Leakage Current," *Journal of the American Ceramic Society,* vol. 95, pp. 257-263, 2012.

[14] Y. Yamada, "Introduction of Small Size MLCC to Aero-Space Application and its technology, Murata," presented at the ESA 1st International Symposium 'Space Passive Component Days', Noordwijk, The Netherlands, 2013.

[15] M. Nakano, A. Saito, and N. Wada, "E–J Characteristics in Multilayer Ceramic Capacitors with the Thin Dielectric Layers," *Key Engineering Materials* vol. 421-422, pp. 277-280, 2009.

[16] T. I. Prokopowicz and A. R. Vaskas, "Research and development, intrinsic reliability, subminiature ceramic capacitors," ECOM, Alexandria, VA, USA 1969.

[17] J. L. Paulsen and E. K. Reed, "Highly accelerated lifetesting of base-metal-electrode ceramic chip capacitors," *Microelectronics Reliability,* vol. 42, pp. 815-820, Jun 2002.

[18] J. G. Simmons, "Richardson-Schottky effect in solids," *Physical Review Letters,* vol. 15, pp. 967-968, 1965.

[19] A. Shiota, T. Oguni, T. Nakamura, M. Matsuda, H. Wada, and H. Sano, "Lifetime Evaluation under Operating Condition for MLCC by Highly Accelerated Life Test," in *Capacitor And Resistor Technology Symposium (CARTS)* Huston, TX, 2013, pp. 207-216.

[20] I. Stolichnov, A. Tagantsev, N. Setter, S. Okhonin, P. Fazan, J. S. Cross, *et al.*, "Constant-current study of dielectric breakdown of Pb(Zr,Ti)O-3 ferroelectric film capacitors," *Integrated Ferroelectrics,* vol. 32, pp. 737-746, 2001.

[21] B. Rawal and H. Chan, "Conduction and failure mechanisms in barium titanate based ceramics under highly accelerated conditions"," ed: AVX Technical information.

[22] A. Teverovsky, "Breakdown voltages in ceramic capacitors with cracks," *IEEE Transactions on Dielectrics and Electrical Insulation,* vol. 19, pp. 1448-1455, 2012.