Experimentally Observed Electrical Durability of 4H-SiC JFET ICs Operating from 500 °C to 700 °C

Philip G. Neudeck[1], David J. Spry[1], Liangyu Chen[2], Dorothy Lukco[3], Carl W. Chang[3] and Glenn M. Beheim[1]

[1]NASA Glenn Research Center, [2]OAI/NASA GRC, [3]Vantage Partners LLC

Abstract. Prolonged 500 °C to 700 °C electrical testing data from 4H-SiC junction field effect transistor (JFET) integrated circuits (ICs) are combined with post-testing microscopic studies in order to gain more comprehensive understanding of the durability limits of the present version of NASA Glenn's extreme temperature microelectronics technology. The results of this study support the hypothesis that T ≥ 500 °C durability-limiting IC failure initiates with thermal-stress-related crack formation where dielectric passivation layers overcoat micron-scale vertical features including patterned metal traces.

Previously, we reported multi-level interconnect 4H-SiC JFET ICs operating for 1000's of hours at 500 °C [1,2] and briefly to 700 °C [2,3].

Figure with caption from [1]

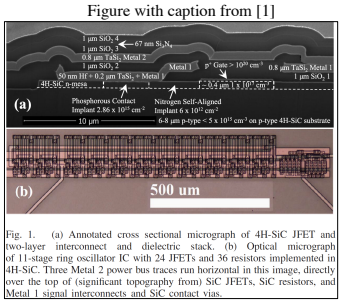
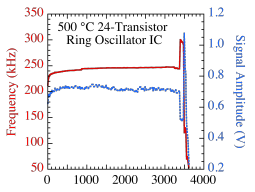
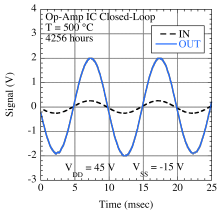
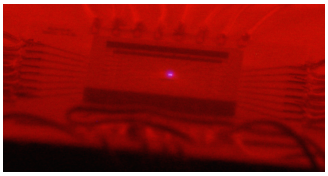


Fig. 1. (a) Annotated cross sectional micrograph of 4H-SiC JFET and two-layer interconnect and dielectric stack. (b) Optical micrograph of 11-stage ring oscillator IC with 24 JFETs and 36 resistors implemented in 4H-SiC. Three Metal 2 power bus traces run horizontal in this image, directly over the top of (significant topography from) SiC JFETs, SiC resistors, and Metal 1 signal interconnects and SiC contact vias.

500 °C durable ring oscillators and op-amps.
Up to 24 transistor digital and analog demonstration ICs.



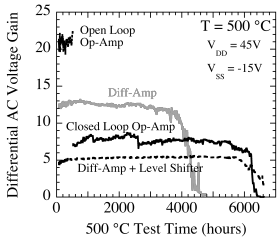


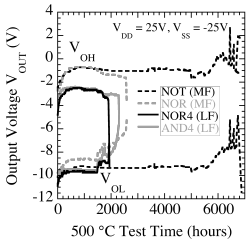


600 °C to 700 °C for accelerated stress testing of 500 °C ICs.

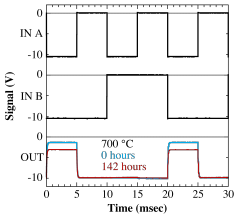
Below we present additional data from packaged integrated circuit oven-testing at 500 °C and 700 °C in room-air atmosphere.

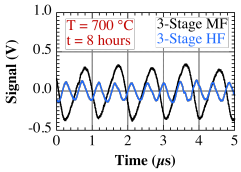
500 °C: All circuits now tested to failure, which occurs prior to 7000 hours.





700 °C: NOR logic gate (left) and ring oscillators (right) [3].





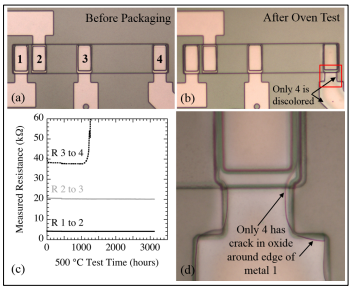
4H-SiC JFET logic ICs intrinsically function at 700 °C.

Most IC failures are consistent with large internal resistance increase (i.e., "open circuit") mode of failure.

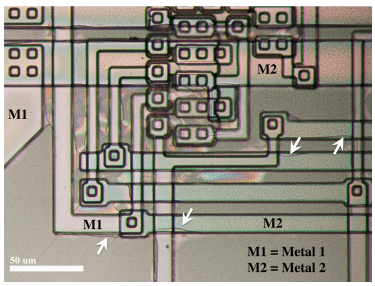
Microscopic studies of multiple failed ICs evidence a common mechanism of IC failure (first proposed in [2], further supported below):

(1) Thermal-stress causes cracks to form in the dielectric, often above topology induced by edges of underlying metal interconnect features.
(2) Cracks enable atmospheric oxygen to reach and locally oxidize (optically discoloring) underying $TaSi_2$ metal inteconnect.
(3) As local $TaSi_2$ oxidation proceeds, interconnect local resistance increases leading to circuit degradation and failure.

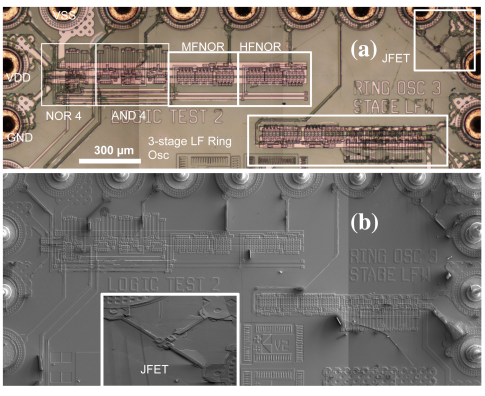
500 °C TLM study from [2].
Only the contact with a dielectric crack (#4) failed.



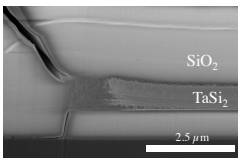
500 °C failed NOR 4 logic gate.
White arrows denote some of the dielectric cracks.



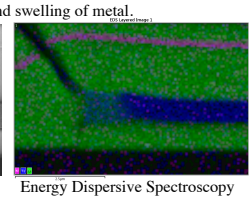
191.5 hours at 700 °C
Far more extensive damage, including oxidized interconnect swelling.



Cross-sectional study of dielectric crack running along edge of $TaSi_2$ interconnect confirms oxidation and swelling of metal.



SEM cross-section showing crack and swelling along edge of $TaSi_2$ trace after 700 °C.



Energy Dispersive Spectroscopy elemental map confirming oxygen in swollen region of metal trace.

Conclusions:

(1) Durability of present-generation 4H-SiC JFET IC at 500 °C is between 1500 hours to 7000 hours.

(2) Crack formation/propagation in dielectric film limits T ≥ 500 °C IC operating lifetime.

References:

[1] D. J. Spry, et al., IEEE Electron Device Lett. 37 (2016) 625-629.
[2] D. J. Spry et al., IMAPS Int. High Temp. Electronics Conf. 2016, pp. 249-256.
[3] D. Spry, et al., SPIE Proc. 9836 (2016) https//dx.doi.org/10.1117/12.2232926.

Acknowledgements: K. Moses, J. Gonzalez, A. Avishai, M. Mrdenovich, A. Miller, M. Krasowski, N. Prokop, R. Okojie, G. Hunter, R. Buttler, L. Matus, R. Meredith.
Work sponsored by NASA under Transformative Tools and Technologies (TTT).