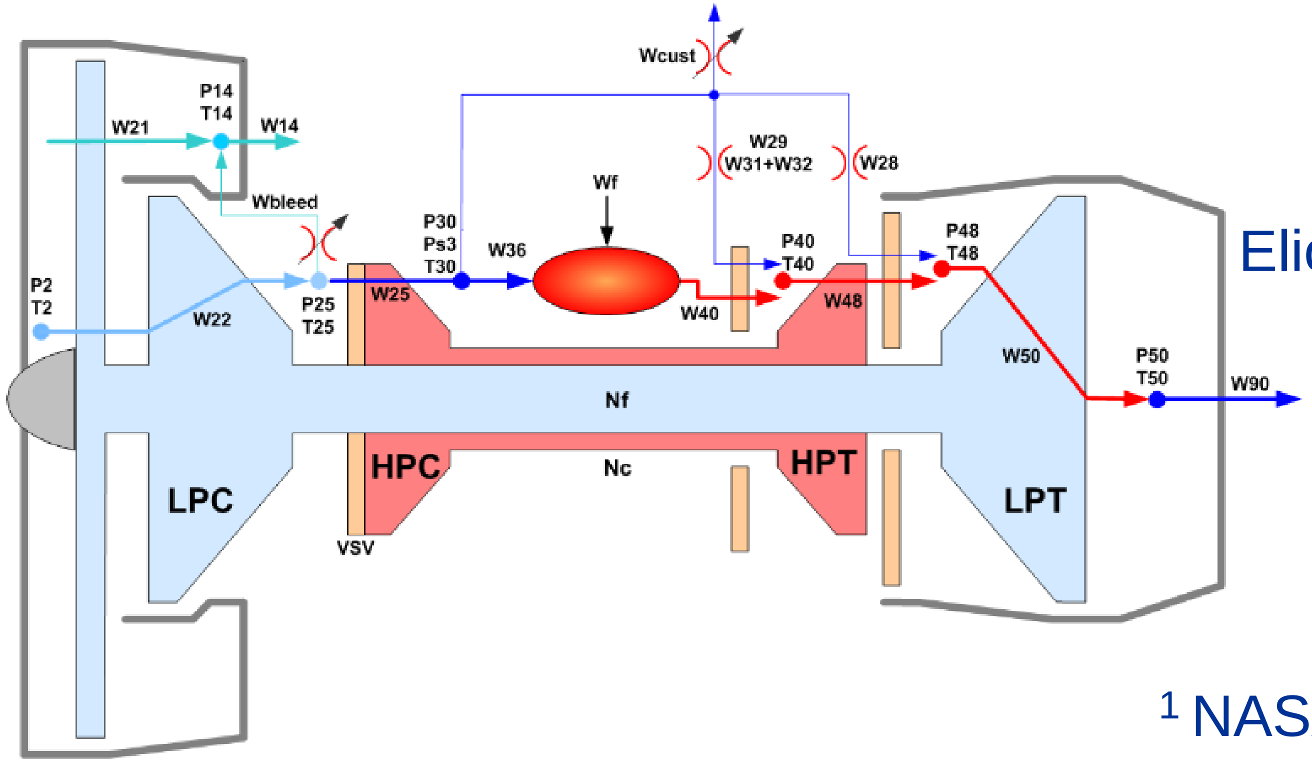
Design and Benchmarking of a Network-In-the-Loop Simulation for Use in a Hardware-In-the-Loop System



Eliot Aretskin-Hariton [1], George Thomas [2]
Dennis Culley [1], Jonathan Kratz [1]

SciTech 2017

[1] NASA Glenn Research Center, Cleveland, OH
[2] N & R Engineering, Parma Hts., OH

Overview

- Background
- Motivation and goals
- Controller Models
- Test Results
- Conclusions

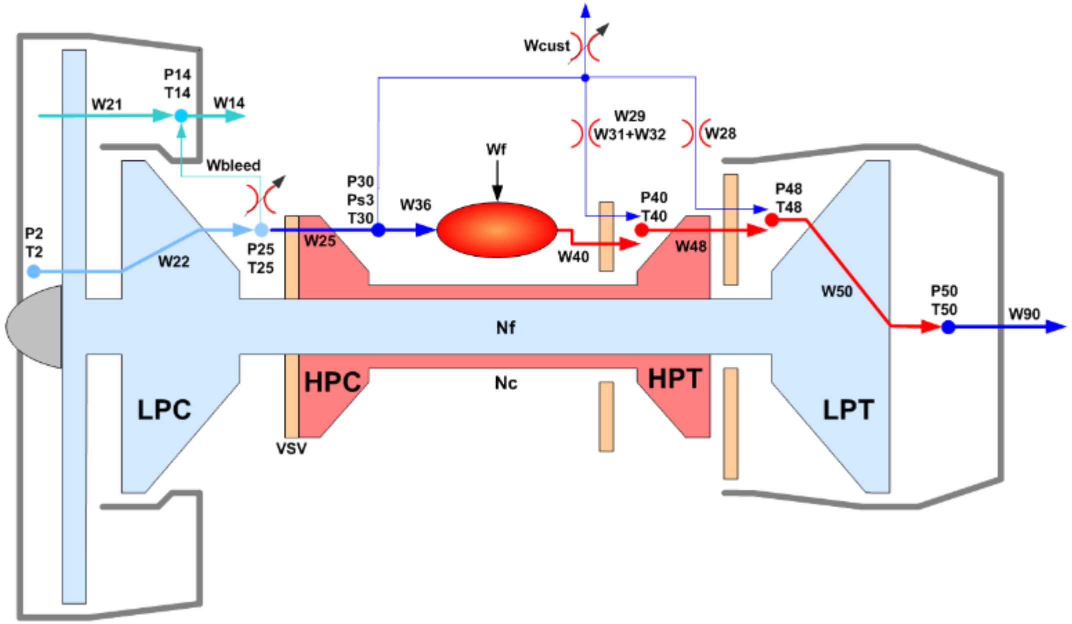
Background
Aircraft Engine Control Architecture

- Centralized control – analog data network to transfer information to/from sensors, analog to digital conversion inside central controller, some signals to the engine have less content

- Distributed Control – digital data network, analog to digital conversion at sensor source, control logic can executed outside of the central controller (e.g. fuel flow meter),

Motivation and Goals

- Develop C-MAPSS40k engine model to better represent a Hardware-In-The-Loop (HIL) system
- Conversion of C-MAPSS40k to a distributed model to enable exploration of distributed engine control
- Allows for the exploration of advanced engine control systems
  - Controls to compensate for information loss
  - Model based controls
  - Requirements exploration

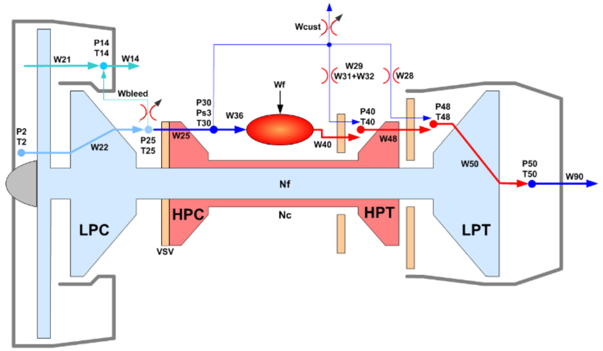


Controller Models

- Baseline: C-MAPSS40k out of the box, 1 computer

Baseline C-MAPSS40k

Engine Model
Control System
User Interface



Several configurations were compared to the original C-MAPSS40k:

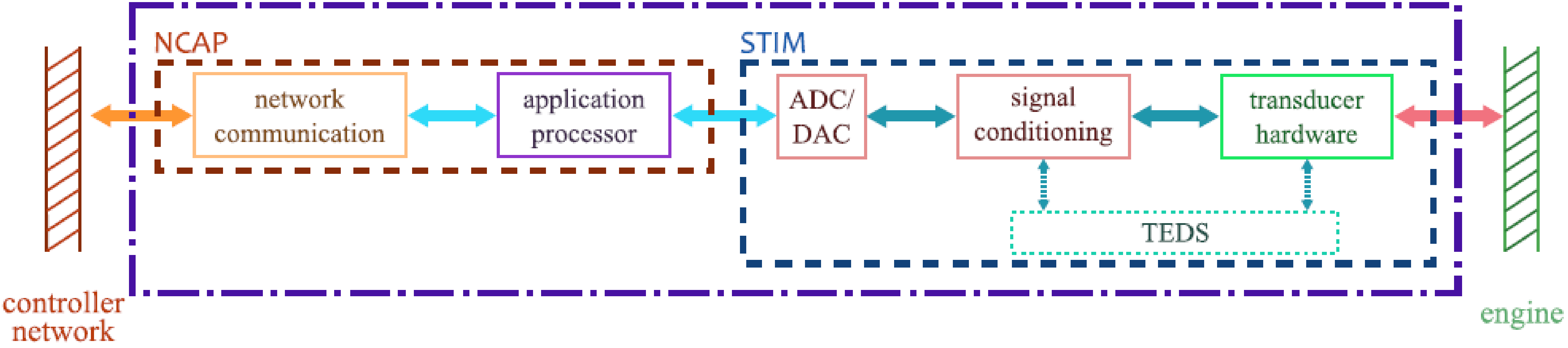
Processor-in-the-Loop (PIL) – SciTech 2016

Ideal Network-in-the-Loop (Ideal NIL) – JPC 2016

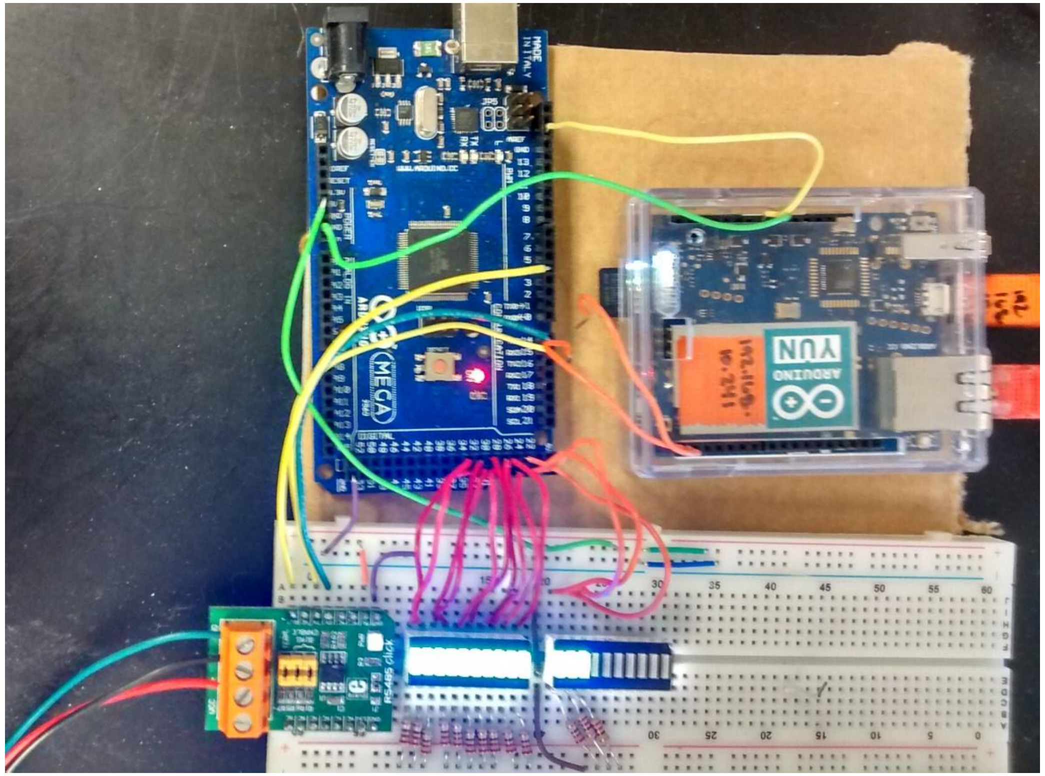
Network-in-the-Loop (NIL) – SciTech 2017

Smart Transducer Model (SXD)

- Network Capable Application Processor (NCAP)
  - Network communication
  - Application interface to STIM
- Smart Transducer Interface Module (STIM)
  - Analog to Digital and Digital to Analog converter
  - Signal conditioning
  - Interface to transducer

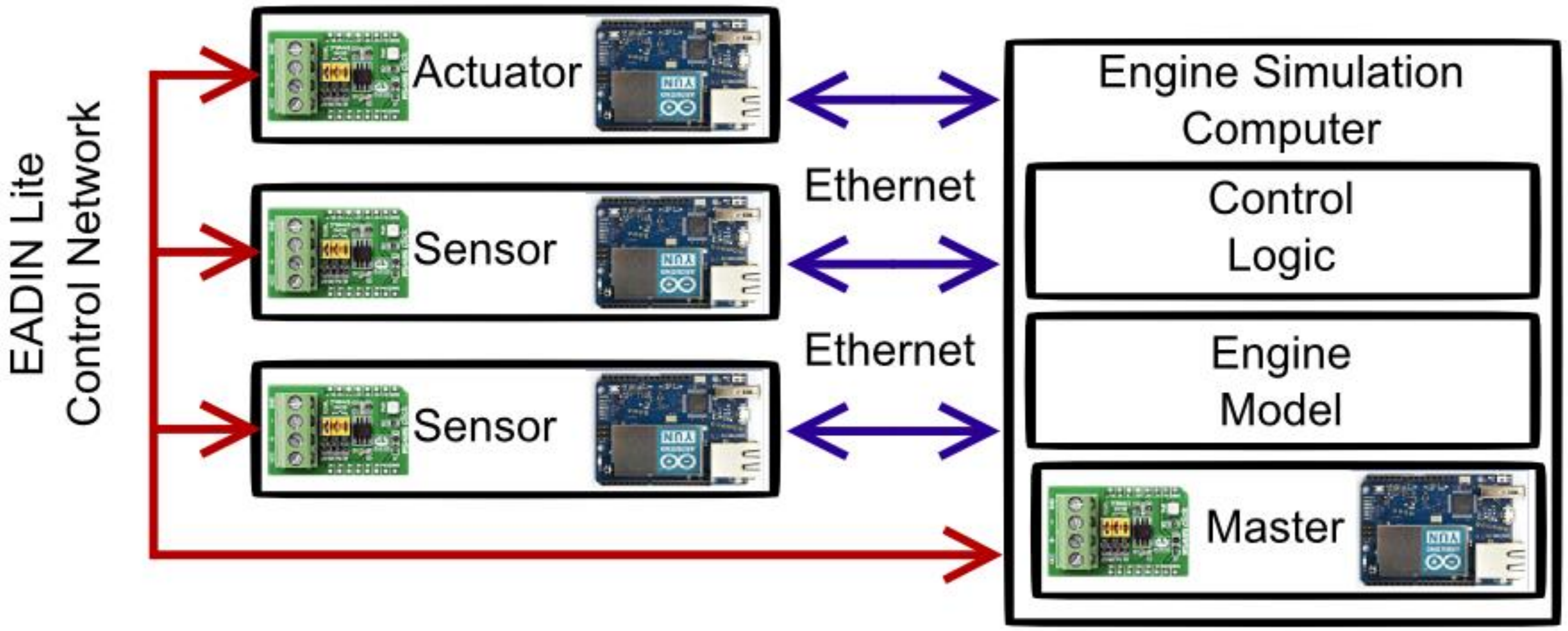


SXD As Implemented in Test Bed



Network-in-the-Loop (NIL) Control Network

- System that allows information to flow between the control logic and the engine simulation
- Traditional engine systems are analog (no latency, star topology)
- New engines are digital (latency, sample delay, many topologies)



EADIN Lite Control Network Details

- Major and Minor Frames

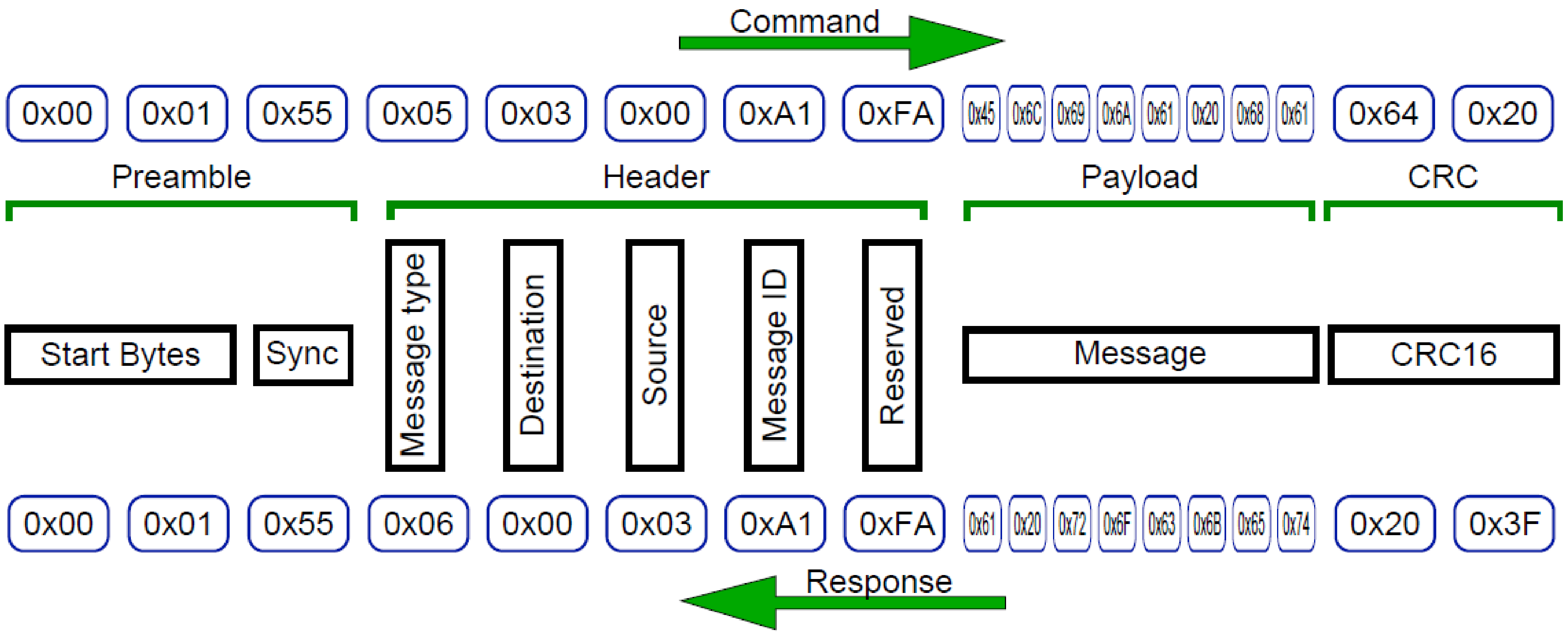
Major Frame	Sampled sensors:
Minor Frame 1	Nc, Nf, T2
Minor Frame 2	Nc, Nf, T50
Major Frame	
Minor Frame 1	Nc, Nf, T2
Minor Frame 2	Nc, Nf, T50

- Frame Interval
- Major frame has 50 minor frames

Node Type	Wf, VSV, VBV, P2, P25, Ps3, P50, Nc, Nf	T2, T25, T30, T50
Sample Interval	10 minor frames	25 minor frames

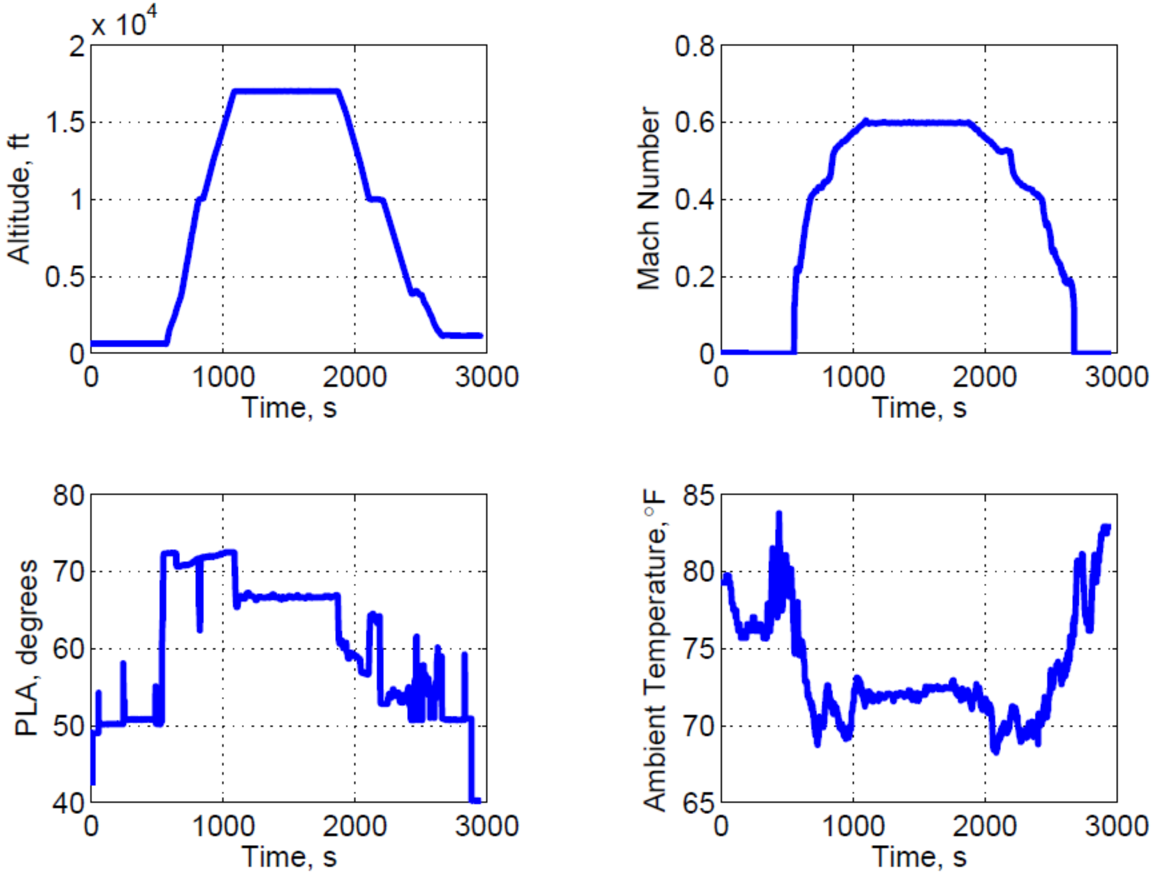
EADIN Lite Control Network Details

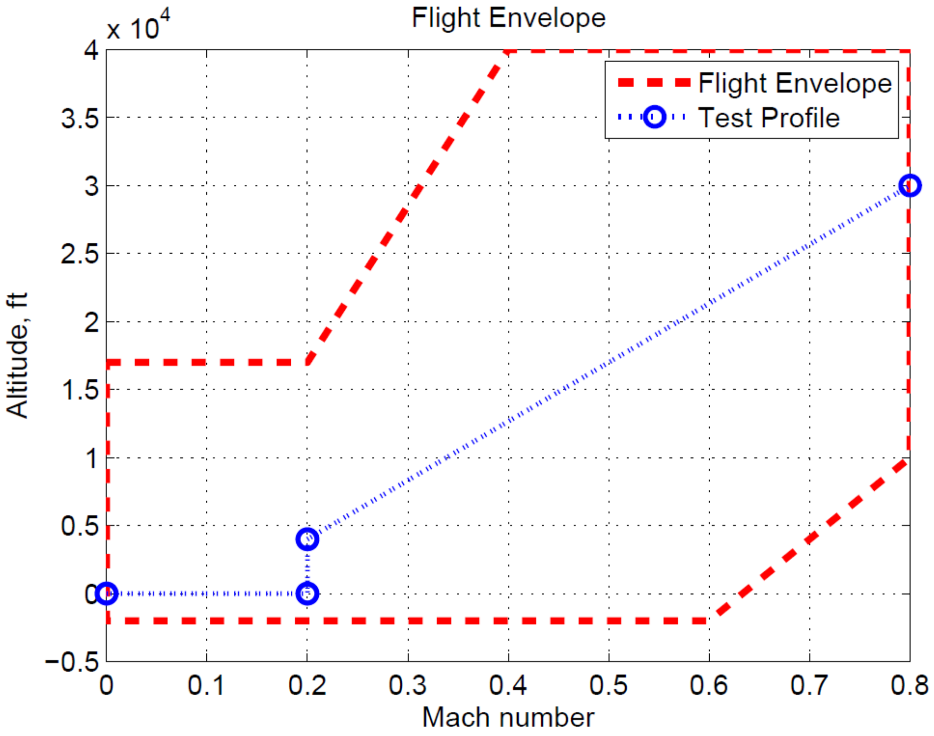
- Master / Slave protocol
- Protocol based on Distributed Engine Control Working Group draft spec.
- Example packet shown below:



Test Setup

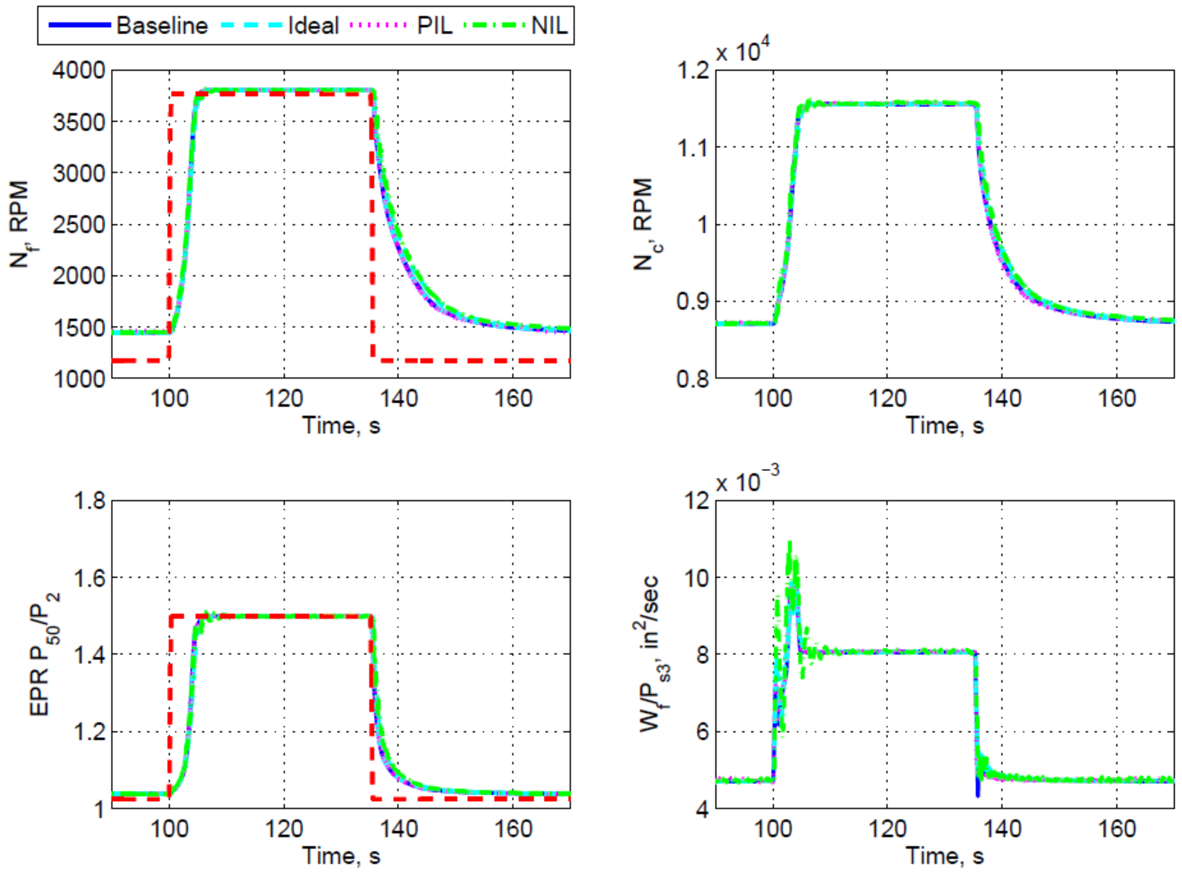
- Real flight profile used to evaluate fuel efficiency
- Burst and chop at various points in the flight envelope to study transients





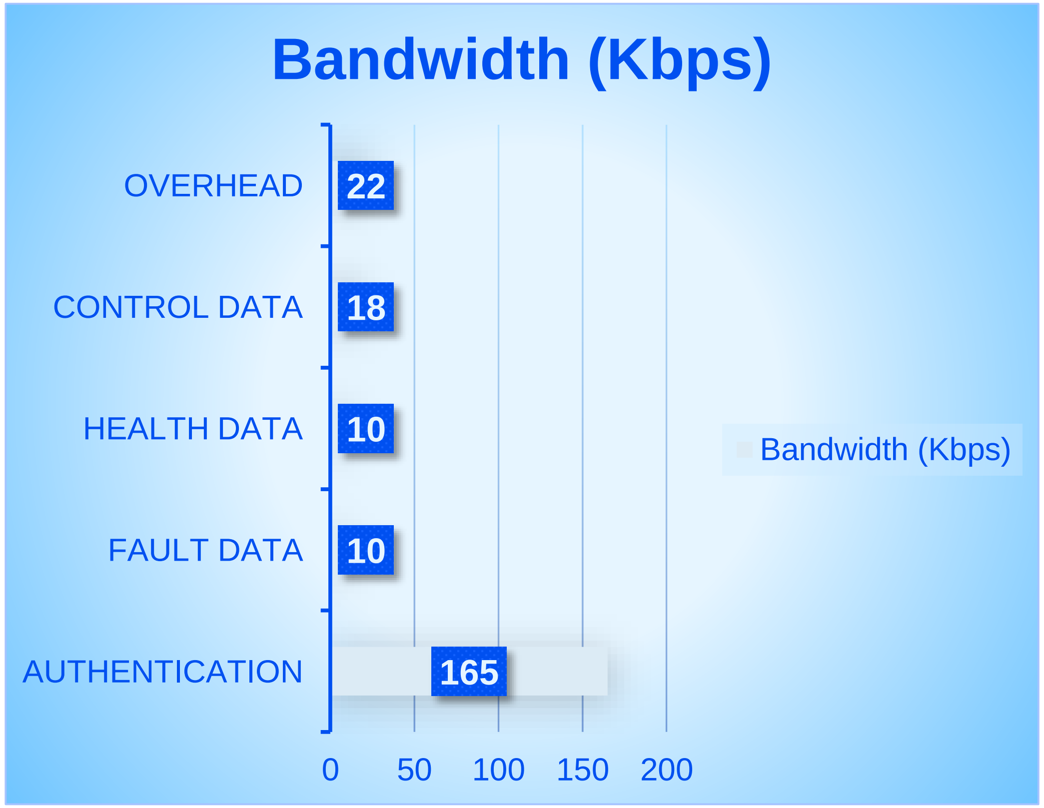
Test Results

- Thrust Specific Fuel Consumption had changed negligibly
- No operability margins violated
- Fuel Flow (Wf) actuator ringing
- NIL system has communication delays, other systems assume instantaneous messaging
- C-MAPSS40k controller was not redesigned to compensate for network delays, SXD quantization, and signal conditioning
- No filtering was applied to the communication network sensor data to take care of aliasing to compensate for reduced sample rate



Network Sizing

- Successful tests indicate potential network speeds of 120Kbps to 450Kbps depending on security requirements
- Additional requirements may create additional loads on the network
- Health Monitoring Data
- Fault Reporting Data
- Authentication
- More Sensors / Actuators



Conclusions

- A real-time network was integrated into C-MAPSS40k engine model
- Impacts of the real-time network on control system performance were studied
- Network bandwidth requirements were estimated
- Results indicate that control logic should be redesigned to optimize networked systems

Questions?

Eliot Aretskin-Hariton

earetski@mail.nasa.gov

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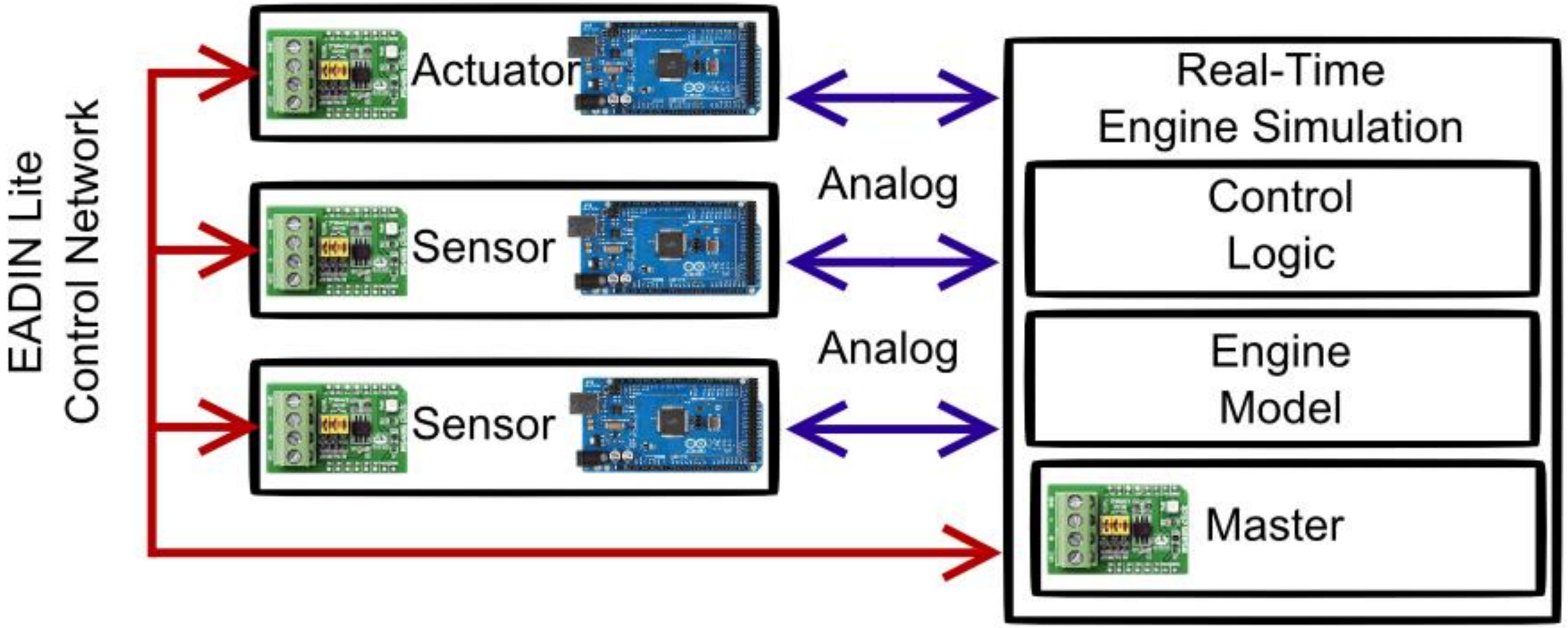
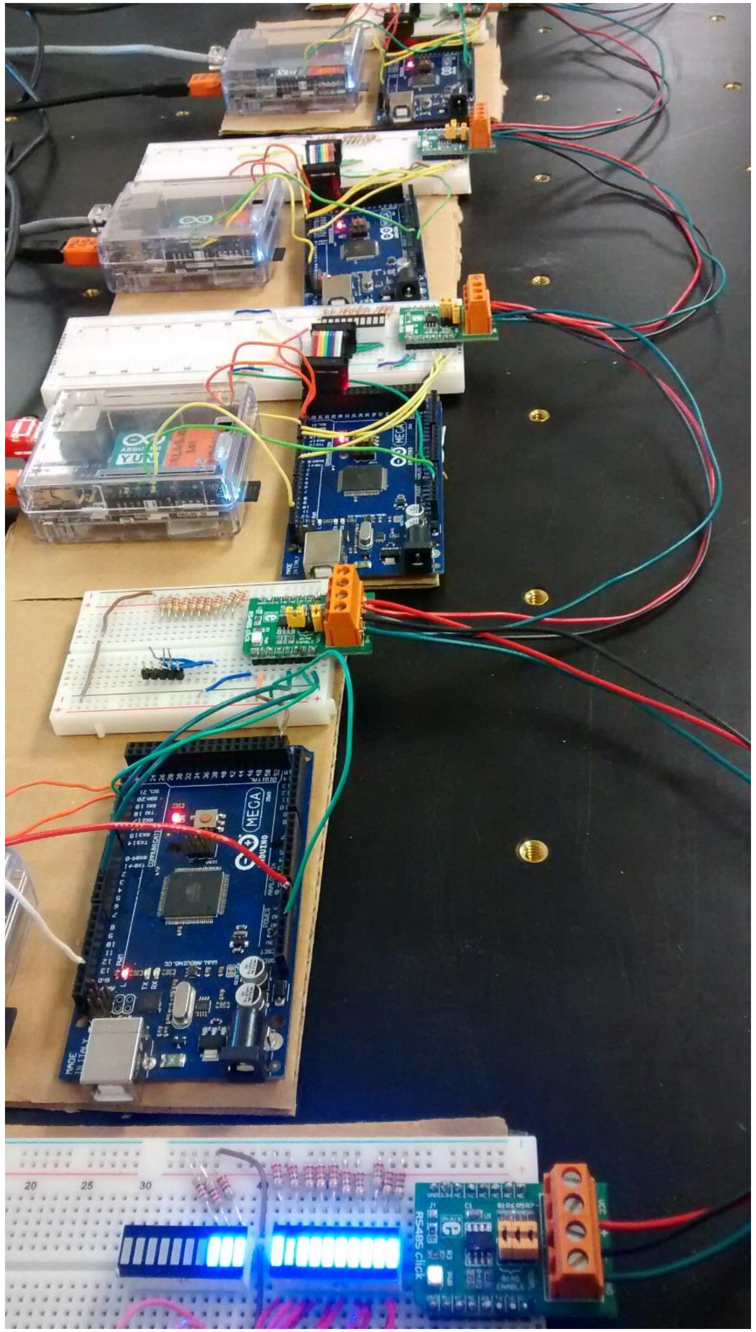
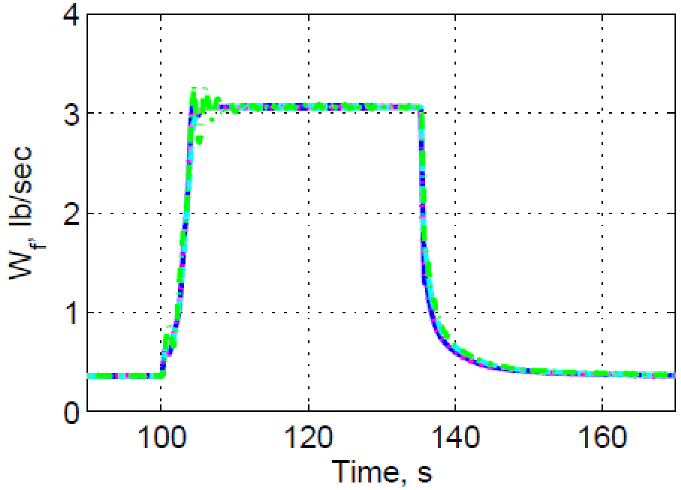
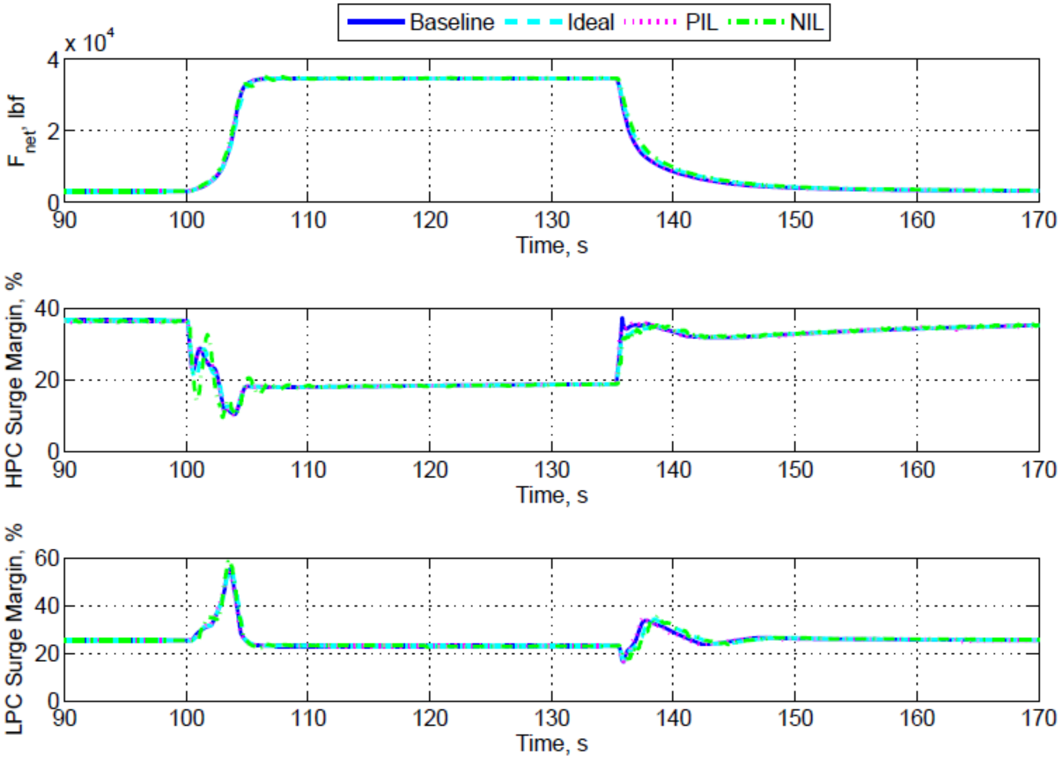
Future Work
Network-in-the-Loop with Analog I/O



Backup




W_f, lb/sec
Time, s
0
1
2
3
4
100
120
140
160


Baseline
Ideal
PIL
NIL
x 10^4
F_{net}, lbf
HPC Surge Margin, %
LPC Surge Margin, %
Time, s
90
100
110
120
130
140
150
160
170