Wideband Reconfigurable Harmonically Tuned GaN SSPA for Cognitive Radios

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Abstract—**The paper presents the architecture of a wideband reconfigurable harmonically-tuned Gallium Nitride (GaN) Solid State Power Amplifier (SSPA) for cognitive radios. When interfaced with the physical layer of a cognitive communication system, this amplifier topology offers broadband high efficiency through the use of multiple tuned input/output matching networks. This feature enables the cognitive radio to reconfigure the operating frequency without sacrificing efficiency. This paper additionally presents as a proof-of-concept the design, fabrication, and test results for a GaN inverse Class-F type amplifier operating at X-band (8.4 GHz) that achieves a maximum output power of 5.14-W, Power Added Efficiency (PAE) of 38.6%, and Drain Efficiency (DE) of 48.9% under continuous wave (CW) operation.**

Keywords—GaN; SSPA; Cognitive; Reconfigurable; X-Band; Satellite Communications; inverse Class-F

I. INTRODUCTION

Cognitive radio is an intelligent wireless communication system that exploits internal parameter tuning capability and knowledge of the external environment to enhance machine learning; and establish reliable communications through the efficient utilization of the radio spectrum [1], [2], and [3]. Internal parameters include as examples transmit-power, carrier-frequency, and modulation waveform; and external environment includes as examples radio interference levels, spectrum availability, and channel capacity.

Cognitive radios are expected to perform all of the above functions across two or more decades of frequency spectrum in order for them to coexist with licensed legacy systems operating at fixed frequency, power level, and bandwidth. Such a lofty goal involves tackling significant design challenges in the implementation of cognitive radios, particularly in the power amplifier section of the transmitter. The overall efficiency of the cognitive radio on board a satellite is essentially determined by the efficiency of the high-power amplifier. Harmonically-tuned power amplifiers such as, the Class-F and inverse Class-F amplifiers are often preferred because of their high PAE [4] and [5]. High PAE results in lower DC power consumption, improves device reliability, and smaller heat sink for excess waste heat removal. However, the input/output matching networks in these amplifiers contain resonant elements for precise control of the second and third harmonics [6]. Consequently, the matching networks are inherently narrow band, which places a huge constraint on the desired decade bandwidth discussed earlier.

In this paper, we present a novel architecture for a harmonically tuned high efficiency, high power, SSPA that can be dynamically reconfigured for frequency and output power in cognitive radios. This is accomplished by designing the SSPA around an unmatched transistor and reconfiguring the center frequency and bandwidth of operation by selecting and switching appropriate input/output matching networks. The bank of input/output matching networks are designed such that the SSPA operates at optimum efficiency over each discrete frequency range, which are contiguous within the S-band (2.2 to 2.4 GHz), X-band (8.0 to 8.5 GHz), and Ka-band (25.5 to 27.0 GHz) frequencies designated for NASA's Near Earth Network satellite communications.

Next as a proof of concept, we present the design, modeled/simulated parameters, and the measured performance of a harmonically tuned high efficiency, high power, inverse Class-F amplifier operating over a narrow frequency band centered at 8.4 GHz (X-band) for reconfigurable cognitive radios. A 6-W Cree CGHV1F006S packaged unmatched GaN High Electron Mobility Transistor (HEMT) is used as the active device to demonstrate the proposed design.

II. ARCHITECTURE OF A WIDEBAND RECONFIGURABLE HARMONICALLY-TUNED HIGH EFFICIENCY/HIGH POWER SSPA FOR A COGNITIVE RADIO:

The architecture of a wideband frequency and output power reconfigurable harmonically-tuned SSPA for a cognitive radio is schematically presented in Fig. 1. In this arrangement, each input matching network (IMN) is paired with a corresponding output matching network (OMN) so as to provide optimum impedance at the input port and the output port of the transistor, respectively; and is implemented across each discrete frequency range, which are contiguous within the designated frequency bands. The optimum impedances presented to the transistor results in a harmonically-tuned amplifier circuit that operates at peak efficiency over a wide band of frequencies. The bandwidth
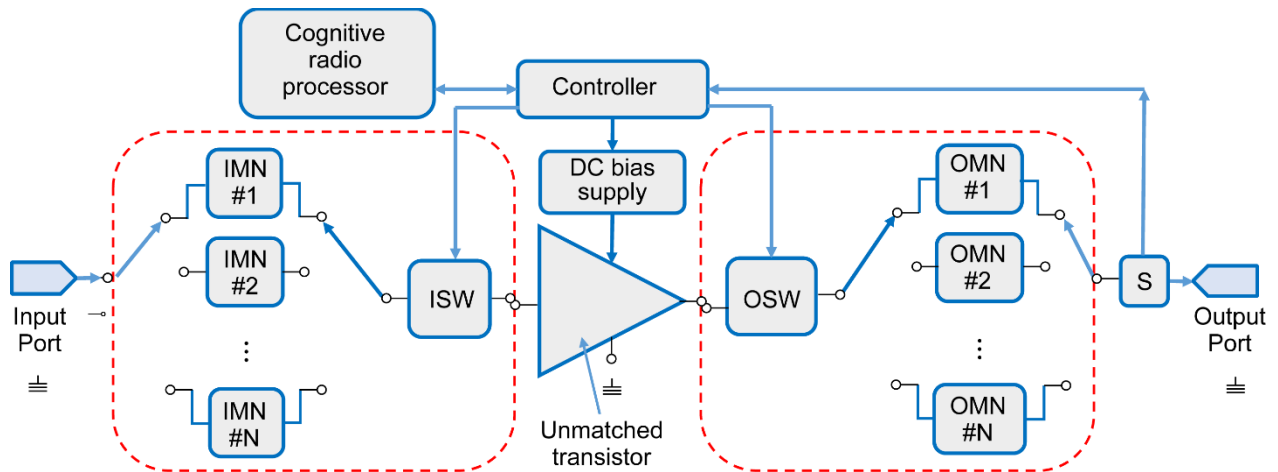
Fig. 1. Circuit level architecture of a wideband reconfigurable, harmonically-tuned high efficiency, high power SSPA.

of the individual matching networks determines the total number of matching networks that are required for contiguous coverage of the entire designated frequency range. The matching networks are coupled to the input port and to the output port of the transistor by an input switch (ISW) and an output switch (OSW), respectively. A controller commands these switches as well as sequentially turns ON the DC bias supply to the gate and drain terminals of the transistor. Frequency reconfiguration is enabled by dynamically selecting the appropriate pair of matching networks. Transmit-power control or power reconfiguration is enabled by selecting the appropriate DC bias parameters to the transistor. To ensure safety and reliability, sensors (S) at the output of the amplifier monitors both the output RF power coupled to the antenna and also the package or case temperature. This information is fed back to the controller, which can turn OFF the DC bias supply in the event of an emergency. The controller receives command from, as well as provides the status information to, the cognitive radio processor.

The transistor in the above architecture is application specific and could either be a Si LDMOS or a GaAs pHEMT or a GaN HEMT. In addition, the switch ISW at the input operates at low RF power levels and consequently could be MEMS based, while the switch at the output operates at high power and hence could be PIN diode based. Furthermore, the physical dimensions of input/output matching network stubs could be significant at S-band frequencies and one way to circumvent this problem is to fabricate them on a high permittivity substrate material such as silicon. Moreover, for volume production, the circuit elements within the area indicated by a dotted red rectangle in Fig. 1 could be manufactured as a single low cost silicon chip.

III. INVERSE CLASS-F AMPLIFIER

A. Harmonically-Tuned Amplifiers

The Class-F presentation of an open at the third harmonic and short at the second to the transistor's drain terminal to achieve high efficiency when operating at saturation is inverted in the case of the inverse Class-F. Many works have shown achieved PAE > 80%, for both types of amplifiers in the 1 to 2 GHz range, but both efficiency and output power drops as the frequency increases [7] and [8].

B. Design of Inverse Class-F Amplifier

The Cree transistor chosen for this development is capable of operating up to 18 GHz. The design center frequency for the inverse Class-F amplifier is 8.4 GHz. Consequently, the second and third harmonics are at 16.8 and 25.2 GHz, respectively. Due to the limitations of the transistor f_T, only the second harmonic is considered in this design. The target output power (P_{out}) is 36 dBm or higher and PAE is 35% or higher.

The transistor amplifier is modeled as a two-port network with input and output matching networks as shown in Fig. 2. In this figure, Γ_S is the reflection coefficient seen looking towards the generator from the output port of the input matching network and Γ_L is the reflection coefficient seen looking towards the load from the input port of the output matching network. Γ_{opt-in} is the optimum reflection coefficient seen looking from the gate terminal of the transistor when the drain terminal is terminated in a matching network. Similarly, $\Gamma_{opt-out}$ is the optium reflection coefficient seen from the drain terminal when the gate terminal is terminated in an matching network. The matching networks are designed such that the transistor sees optimum impedances at the gate and drain terminals at the fundamental and higher harmonic frequencies for maximum P_{out} and PAE. To accomplish this task, design and simulation software tools such as Keysight® Technologies' Advanced Design System (ADS), which includes Momentum 3D planar EM simulator is used. In addition, built in passive device libraries and models provided by CREE are used in the simulations.

Through drain characteristics, load pull, harmonic balance, and S-parameter simulations, proper DC biasing and optimal terminating impedances were established. To present the optimal impedances to the gate and drain terminals, input/output
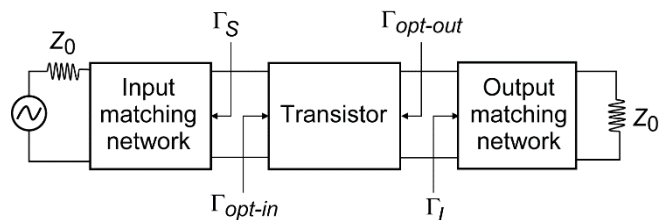

Fig. 2. Schematic of the inverse Class-F amplifier design.

matching networks were designed using quarter-wave transmission lines, radial stubs, surface mount devices (SMD), open stubs, and shunt components. In addition, to ensure stability by suppressing oscillations a low frequency stability circuit at the input and a parallel resistor-inductor (RL) circuit in the gate DC bias line were provided [9].

C. Amplifier Circuit Fabrication

The amplifier circuit was fabricated on a 20 mil, half ounce Rogers® RO3003™ substrate with permittivity ε_r = 3.0. Photolithography was used to etch the circuit pattern and an LPKF U3 laser was used to drill via holes and cut the board outlines. Figure 3 shows the final fabricated amplifier with soldered surface mount devices, and with coaxial input/output connectors for characterization. The assembled amplifier circuit board is attached to a forced air cooled aluminum heat sink.
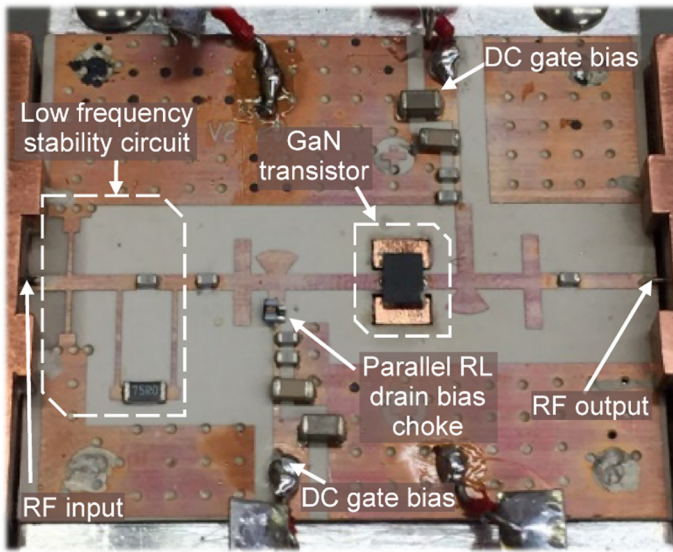

Fig. 3. Fabricated X-band inverse Class-F GaN amplifier.

D. Transistor Thermal Management

Thermal management is a crucial factor in design of high power amplifiers for space applications. Any microwave integrated circuit operating at a temperature greater than 110 °C or junction temperature above 125 °C is prohibited by the EEE-INST-002 quality standard [10]. For stable operation as a continuous wave amplifier, it was determined important to include efficient heat management techniques in the design to lower the junction temperature of the transistor and thereby improve the amplifier stability. Figure 4(a) shows a small milled copper tab that was attached to the belly of the transistor package, contacting all four ground terminals using thermally conductive epoxy. The transistor and copper tab were then inserted into a cutout in the substrate as shown in Fig. 4(b). The contact between the copper tab and the aluminum heat sink below was established using conductive thermal adhesive and grease. Copper's thermal conductivity is second to CVD diamond [11] and performed well in spreading the waste heat
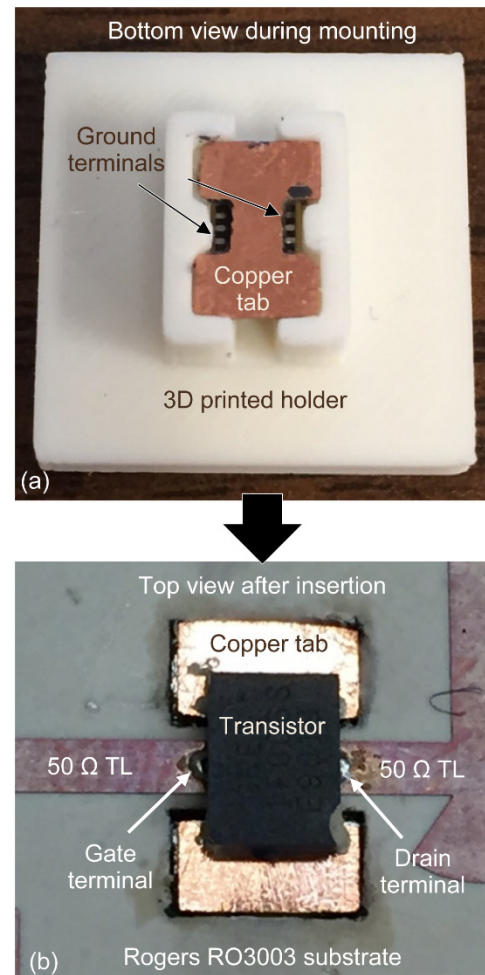

Fig. 4. (a) Copper tab and transistor mounting process using 3D printed holder; (b) Insertion of packaged transistor into Rogers 3003 board.

away from the transistor's package, which was validated by observing the thermal profile through a thermal imager as explained in Section IV. The copper heat sink resulted in a drain current close to the manufacturer's specification and also improved the overall RF performance of the amplifier.

E. Tuning the Amplifier Post Fabrication

Due to discrepancies between simulated and measured input and output impedance, tuning the amplifier post fabrication was deemed necessary to improve overall RF performance. The tuning was accomplished by adding floating copper pads along transmission lines (TL) as shown in Fig. 5. These tabs provide the necessary circuit elements to improve the input and output impedance match and bring the measured and simulated Γ_{opt-in} and $\Gamma_{opt-out}$ in close agreement. In Figs. 6 and 7 the measured and simulated Γ_{opt-in} and measured and simulated $\Gamma_{opt-out}$, with copper pad tuning, are shown to be in good agreement at both the fundamental (8.4 GHz) and second harmonic (16.8 GHz) frequencies.
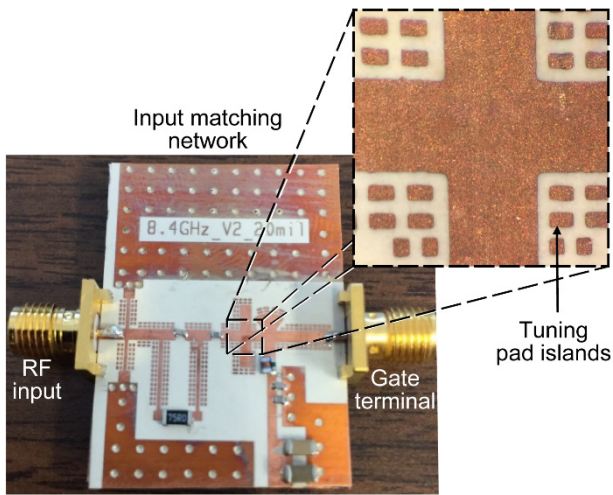
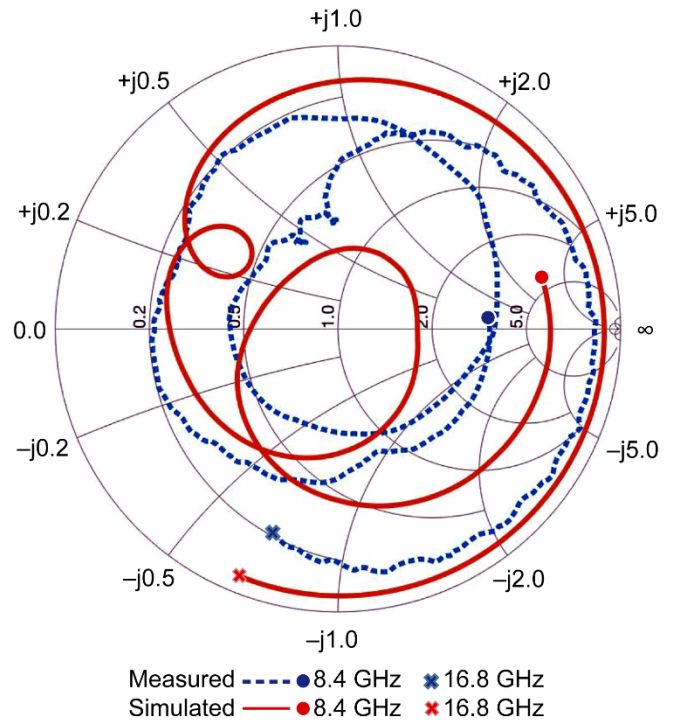Fig. 5.   Isolated input matching network with tuning pads.

Measured ----●8.4 GHz ✖16.8 GHz
Simulated ——●8.4 GHz ✖16.8 GHz

Fig. 6.   Simulated and Measured ($\Gamma_{opt\text{-}in}$) parameters of input matching network after copper pad tuning from 8.4 to 16.8 GHz.
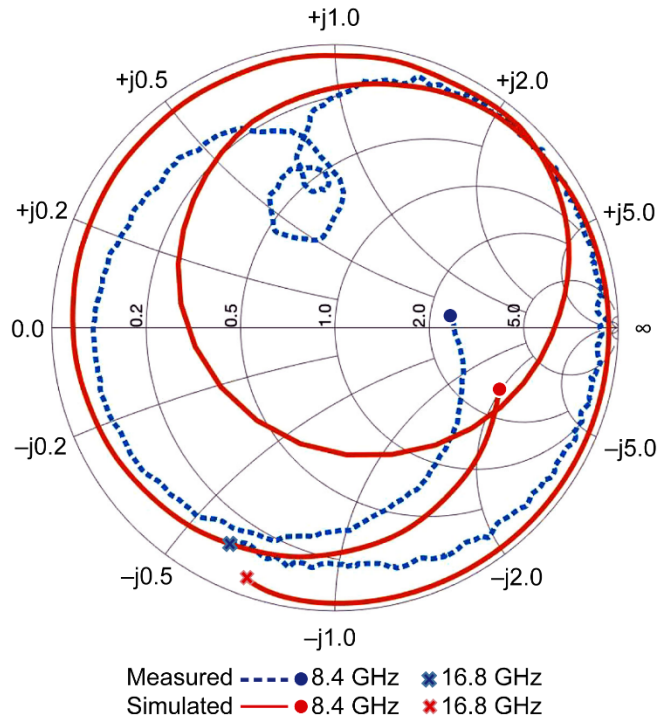

Measured ----●8.4 GHz ✖16.8 GHz
Simulated ——●8.4 GHz ✖16.8 GHz

Fig. 7.   Simulated and Measured ($\Gamma_{opt\text{-}out}$) parameters of output matching network after copper pad tuning from 8.4 to 16.8 GHz.

IV. INVERSE CLASS-F AMPLIFIER CHARACTERIZATION

A. Maximum Output Power and PAE

Measured output power (P_{out}) and PAE as a function input drive power (P_{in}) is presented in Fig. 8. The measured gain and VSWR as a function of P_{in} is presented in Fig. 9. The maximum output power at saturation (P_{sat}) is 5.14 W at 8.45 GHz and the corresponding gain is 6.6 dB, PAE is 35.4% and drain efficiency (DE) is 45.1%. The maximum PAE improves to 38.6% at 8.34 GHz and when V_{DS} = 35 V and V_{GS} = −3.2 V. The corresponding P_{out} is 4.36 W, gain is 6.76 dB, and DE is 48.9%.
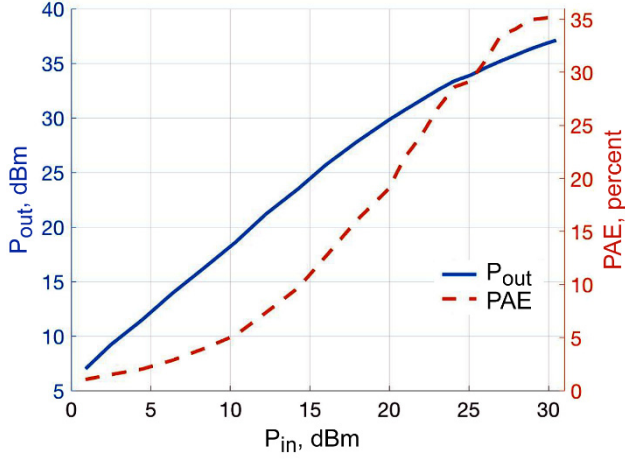

Fig. 8. Measured P_{out} and PAE vs. P_{in} for inverse Class-F GaN amplifier, V_{DS} = 40 V, V_{GS} = −3.2 V and frequency = 8.45 GHz.
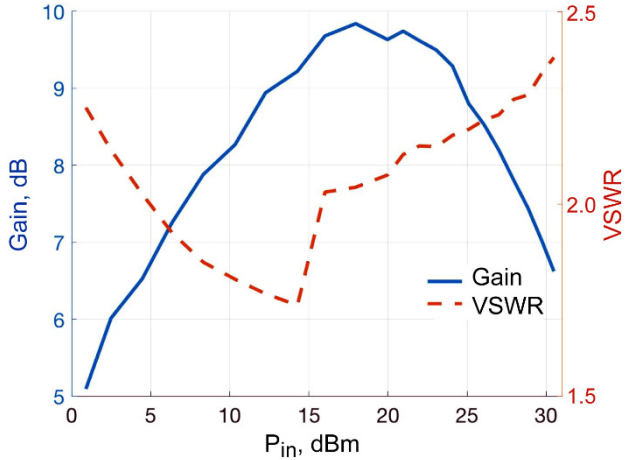

Fig. 9. Measured Gain and VSWR vs. P_{in} for inverse Class-F GaN amplifier, V_{DS} = 40 V, V_{GS} = −3.2 V, and frequency = 8.45 GHz.

B. Thermal Profile

Thermal profile of the inverse Class-F GaN amplifier was evaluated during CW operation for different settings of the input frequency, P_{in}, and V_{DS}. In each case the P_{out}, gain, PAE and the package or case temperature of the transistor was recorded. The temperature was determined using a Flir® Exx series infrared camera. The results are summarized in Table I. Figure 10 presents the thermal profile of the amplifier under the above-mentioned conditions as observed by the infrared camera.

The data in Table I indicates that when the frequency, P_{in}, and V_{DS} are 8.36 GHz, 29.9 dBm, and 32 V, respectively, the package or case temperature is 95 °C. The estimated DC power dissipated by the transistor under these conditions is ≈ 7 W. The transistor manufacturer's data sheet indicates that for a package or case temperature of 95 °C, the maximum allowable power dissipation can be as high as 9 W [12]. Thus, the inverse Class-F GaN amplifier under the above operating conditions has a thermal safety margin of ≈ 22%.

TABLE I. TRANSISTOR PACKAGE OR CASE TEMPERATURE PROFILES FOR VARIOUS FREQUENCY, INPUT POWER, AND DRAIN BIAS; V_{GS} = −3.2 V, I_{DS} RANGES 0.22 TO 0.27 A.

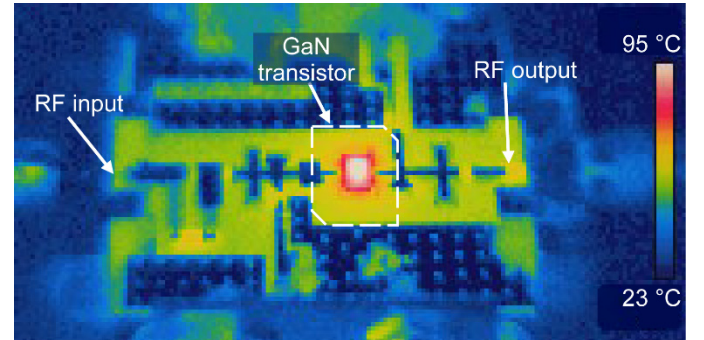| Freq. (GHz)	P_{in} (dBm)	V_{DS} (V)	Gain (dB)	PAE (%)	Temp (°C)	P_{out} (W)
8.45	29.1	32	6.7	37.4	86	3.8
8.45	29.9	32	6.1	34.7	93	3.9
8.36	29.9	32	6.3	37.3	95	4.2
8.32	28.4	32	6.8	34.2	106	3.3
8.32	28.0	35	7.5	34.7	118	3.5
8.45	29.1	35	6.4	31.2	122	3.5
8.45	27.2	40	7.9	30.8	125	3.2
8.32	28.9	35	6.8	32.3	128	3.7
8.32	27.9	40	7.7	32.2	140	3.7
8.32	28.8	40	7.5	33.8	143	4.3
8.45	29.9	40	6.9	36.2	148	4.9

Fig. 10. Thermal profile of inverse Class-F GaN amplifier as observed by the infrared camera, Frequency = 8.36 GHz, P_{in} = 29.9 dBm, V_{DS} = 32 V, and V_{GS} = −3.2 V.

C. Amplifier Bandwidth

The measured PAE and P$_{out}$ as a function of the frequency is presented in Fig. 11. The design requirements for the inverse Class-F GaN amplifier is P$_{out}$ > 36 dBm and PAE > 35%. The data in Fig. 11, indicates that the above requirements can only be met over a very narrow frequency range extending from 8.315 to 8.385 GHz. Hence, the inverse Class-F GaN amplifier has relatively a narrow bandwidth on the order of 70 MHz at X-band. The measured gain and VSWR as a function of the frequency is presented in Fig. 12. As predicted from simulations, when the VSWR is minimum, the P$_{out}$ and PAE are maximum.
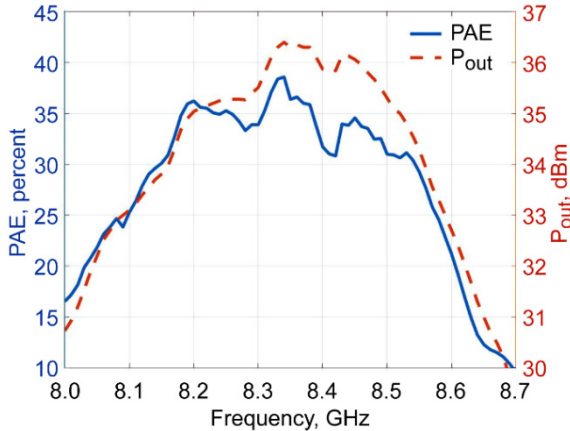

Fig. 11. Measured PAE and P$_{out}$ vs. Frequency for inverse Class-F GaN amplifier; V$_{DS}$ = 40 V, V$_{GS}$ = −3.2 V; P$_{in}$ ranges 21.5 to 30.35 dBm, VSWR ranges 2.4 to 33.
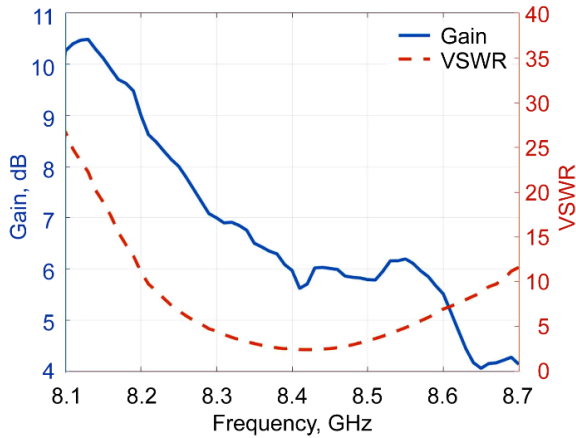

Fig. 12. Measured Gain and VSWR vs. Frequency for inverse Class-F GaN amplifier; V$_{DS}$ = 40 V, V$_{GS}$ = −3.2 V; P$_{in}$ ranges 21.5 to 30.35 dBm.

V. DISCUSSIONS AND CONCLUSIONS

The architecture for a wideband reconfigurable harmonically-tuned GaN SSPA for cognitive radios is presented. The SSPA topology offers broadband high efficiency performance through the use of multiple tuned input/output matching networks, which enables the cognitive radio to reconfigure the operating frequency without sacrificing efficiency. Additionally, as a proof-of-concept the design, fabrication and characterization of a GaN inverse Class-F type amplifier operating at X-band (8.4 GHz) is presented. The amplifier achieves P$_{SAT}$ of 5.14W, PAE of 38.6%, and DE of 48.9% in continuous wave (CW) operation. The amplifier has a narrow bandwidth, which is on the order of 70 MHz at X-band.

VI. FUTURE WORK

Future work will focus on the design of multiple tuned input/output matching networks on a chip to enhance the bandwidth. In addition, RF power combining techniques to achieve higher output power and demonstrate transmit power reconfiguration. The power combining will include the development of a balanced amplifier that can doubles output power and also a spatial power combiner based on a planar NxN element array of patch antennas. The details on the patch antennas can be found in a companion paper at the CCAA Workshop entitled, "Reconfigurable Wideband Circularly Polarized Stacked Square Patch Antenna for Cognitive Radios."

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