

Advanced Stirling Convertor Control Unit Testing at NASA Glenn Research Center in the Radioisotope Power Systems System Integration Laboratory

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Future NASA missions could include long duration flyby, orbital, lander, or rover applications where generating power from sunlight may be limited. Radioisotope Power Systems (RPS) provide a dependable power source for missions where inadequate sunlight or operational requirements make other power systems impractical. Over the past 16 years, NASA Glenn Research Center (GRC) has been supporting the development of RPSs. The Advanced Stirling Radioisotope Generator (ASRG) utilized a pair of Advanced Stirling Convertors (ASC). While flight development of the ASRG has been cancelled, much of the technology and hardware continued development and testing to guide future activities. Specifically, a controller for the convertor(s) is an integral part of a Stirling-based RPS. For the ASRG design, the controller maintains stable operation of the convertors, regulates the alternating current (AC) produced by the linear alternator of the convertor, provides a specified direct current (DC) output voltage for the spacecraft, synchronizes the piston motion of the two convertors to minimize vibration as well as manage and maintain operation with a stable piston amplitude and hot end temperature. It not only provides power to the spacecraft but also must regulate convertor operation to avoid damage to internal components and maintain safe thermal conditions after fueling. Lockheed Martin Coherent Technologies (LMCT) has designed, developed and tested an Engineering Development Unit Advanced Stirling Convertor Control Unit (EDU ACU) to support this effort. GRC used the ACU EDU as part of its non-nuclear representation of a RPS which also consists of a pair of Dual Advanced Stirling Convertor Simulator (DASCS), and associated support equipment to perform a test in the Radioisotope Power Systems System Integration Laboratory (RSIL). The RSIL was designed and built with flexibility to evaluate hardware utilizing RPS technology. The RSIL provides insight into the electrical interactions between as many as 3 radioisotope power generators, associated control strategies, and typical electric system loads. The first phase of testing included a DASCS which was developed by Johns Hopkins University/Applied Physics Laboratory and simulates the operation and electrical behavior of a pair of ASC's in real time via a combination of hardware and software. Testing included the following spacecraft electrical energy storage configurations: capacitive, battery, and supercapacitor. Testing of the DASCS and ACU in each energy storage configuration included simulation of a typical mission profile, and transient voltage and current data during load turn-on/turn-off. Testing for these devices also included the initiation of several system faults such as short circuits, electrical bus over-voltage, under-voltage and

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a ‘dead bus’ recovery to restore normal power operations. The goal of this testing was to verify operation of the ACU(s) when connected to a spacecraft electrical bus. The results of these tests are presented here.

Nomenclature

<i>ACU</i>	= advanced Stirling convertor control unit
<i>A/D</i>	= analog to digital
<i>APS</i>	= ASC piston sensor
<i>ASC</i>	= advanced Stirling convertor
<i>ASRG</i>	= advanced Stirling radioisotope generator
<i>D/A</i>	= digital to analog
<i>DASCS</i>	= dual advanced Stirling convertor simulator
<i>DAQ</i>	= data acquisition system
<i>DSP</i>	= digital signal processor
<i>EDU</i>	= engineering development unit
<i>EM</i>	= engineering model
<i>GRC</i>	= Glenn Research Center
<i>FCDA</i>	= facility control and data acquisition
<i>FPGA</i>	= field programmable gate array
<i>IGBT</i>	= insulated gate bipolar transistor
<i>JHU/APL</i>	= the Johns Hopkins University/Applied Physics Laboratory
<i>LMCT</i>	= Lockheed Martin/Coherent Technologies
<i>PDCU</i>	= power distribution control unit
<i>PMAD</i>	= power management and distribution system
<i>PWM</i>	= pulse width modulation
<i>RMS</i>	= root mean square
<i>RPS</i>	= radioisotope power system
<i>RSIL</i>	= radioisotope power system systems integration laboratory
<i>SRU</i>	= shunt regulator unit
<i>SSPC</i>	= solid state power controller

I. Introduction

The Radioisotope Power Systems (RPS) program has worked to develop the Advanced Stirling Radioisotope Generator (ASRG) technology for applications in future space missions. Related technologies include Advanced Stirling Convertors (ASC), an Advanced Stirling Convertor Control Unit (ACU), and Dual Advanced Stirling Convertor Simulator (DASCS). The ASC’s were developed by Sunpower, the ASRG and ACU was developed by Lockheed Martin, and the DASCS was developed by the Johns Hopkins University/Applied Physics Laboratory (JHU/APL). As part of the RPS program, a decision was made to also develop a Radioisotope Power Systems System Integration Laboratory (RSIL) to help verify and validate RPS components to advance the ASC/ACU Technology Readiness Level (TRL). RSIL is capable of simulating an end-to-end power system to provide insight into the electrical interactions of up to 3 representative RPS sources operating in parallel, the associated control schemes, and typical electrical loads.

Initial testing in RSIL validated the operation and interaction of two ASCs, two DASCS units, and a Dual Convertor Controller (DCC) engineering model (EM) as reported in [Ref 1]. This paper presents the second test series consisting of two ACUs and two DASCS units for verification of correct ACU operation.

II. Testing Components

A. ACU/EDU

The ACU controls the ASC’s piston amplitude and synchronizes them at their operating frequency by means of an AC voltage input to the ASC alternator coil winding. Figure 1 shows a high level block diagram and the ACU interfaces to the ASCs and host spacecraft. The ASC piston sensor (APS) shown in Figure 1 allows the ACU to measure the piston amplitude and is only used when operating with ASC’s. Figure 2 is one level deeper and shows the ACU controller card block diagram with associated functions to perform ACU operations. The ACU has three controller cards, two cards (designated card 1 and card 2 in Figure 1) to actively control two ASCs contained in the

ASRG housing and the third card is in hot standby, providing a single-fault tolerant, N+1 redundancy architecture. The controller cards in the ACU also provide independent power factor correction and voltage control to each ASC to allow for fine tuning when variations are seen in the ASCs. The ACU converts single-phase AC power into DC and sources DC current to the spacecraft by following its bus voltage between 22 and 34 Vdc. Above 34 Vdc, the converted DC power is shunted to the ASRG external shunt; below 22 Vdc, current is provided to the spacecraft to assist in the bus voltage recovery.

Operational telemetry and command/control between the spacecraft and ASRG are performed via the redundant MIL-STD 1553B serial bus residing in controller cards 1 and 3. The ACU fault handling and transfer of ASC control from an active card to the spare is autonomous, utilizing several fault monitors that are either self-determined or majority voted to activate the failover switch.

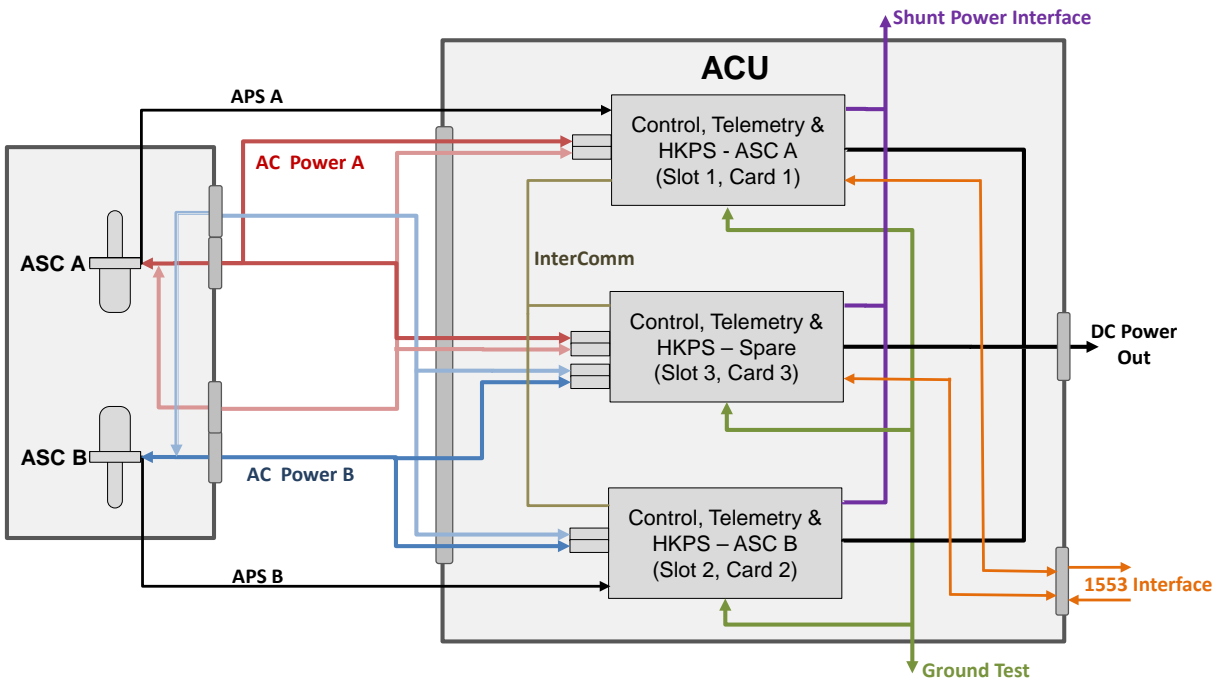


Figure 1. ACU high Level block diagram.

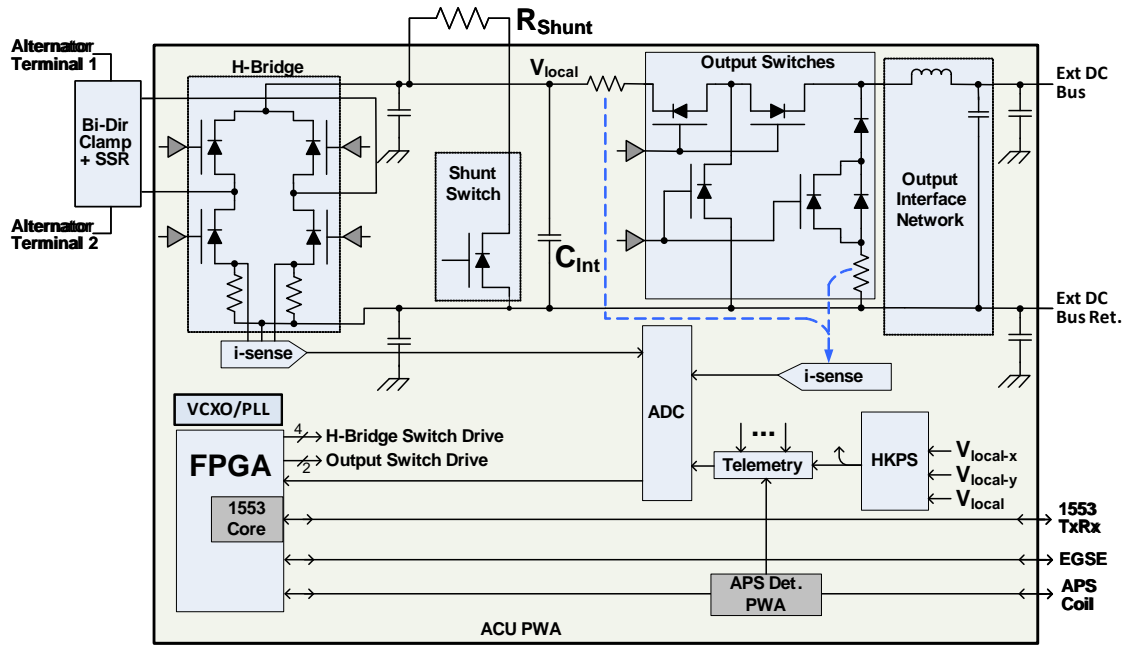
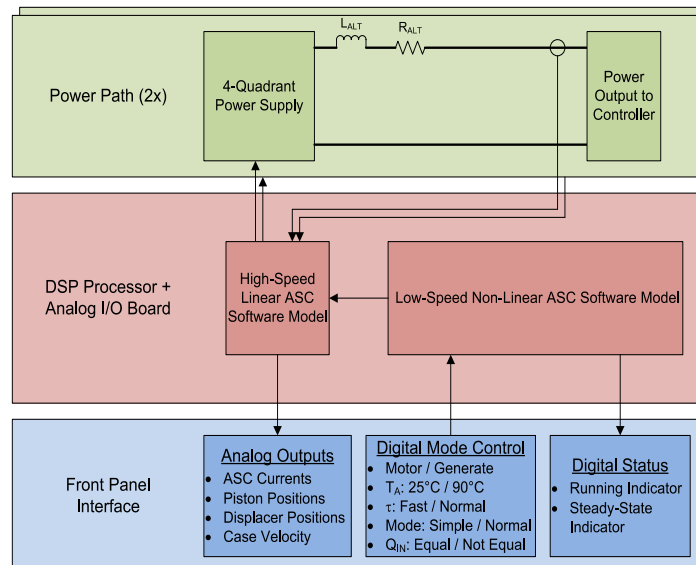


Figure 2. ACU controller card block diagram.

B. DASCS

A DASCS was developed using custom-designed circuits, commercial equipment, and a linearized ASC model [Ref 2] implemented in software on an off-the-shelf digital signal processor (DSP) development board. A block diagram including user interface capabilities of the DASCS is shown in Figure 3 while a photograph of the DASCS is shown in Figure 4.



Alternator inductance and resistance are modeled with physical components with electrical properties similar to the actual alternator in series with a back emf voltage source. A commercial current sensor is filtered and then digitized by an analog to digital converter (A/D) in the DSP development system. The DSP is programmed to use the input current to calculate and produce an output voltage through a digital to analog converter (D/A), also part of the DSP, proportional to the ideal converter back emf voltage based on the ASC model equations. The back emf voltage passes through an electrical isolator and is then used to control the output of a 400W commercial power supply. The power supply output is the equivalent of the back emf output of the converter alternator. The DASCs output is calculated from ASC model equations and includes converter mechanism dynamics beyond the alternator electrical inductance and resistance. The DASCs can be reprogrammed to mimic other types of Stirling converters by changing the linear model implemented in the DSP and the physical alternator inductance and resistance components.

Previous engine simulator designs used an AC source, resistor, and inductor and only modeled electrical performance with no consideration of converter mechanical behavior. Designers frequently found that their controllers did not function the same with an ASC as with their engine simulator. The impact of controller problems like AC input current sampling noise or spacecraft bus voltage changes on mechanical parameters like piston amplitude could only be investigated using time-consuming testing with a real ASC. In addition, damage to the ASC might occur during such evaluations.

The DASCs was used to test the DCC prior to operating with an actual ASC. The DASCs helped solve numerous nonlinearity and noise-related problems in sensing the alternator current. Overcoming those issues reduced output power fluctuations at the load, resulting in smaller peak-to-peak variations in piston amplitude and improved operating efficiency. The effectiveness of the DASCs was shown when the ASC was successfully controlled, at full power, on the first attempt by the DCC controllers. If DCC testing was only performed with an ASC, the success of the controller design and its 2-year design and development time to full-power ASC demonstration would not have been possible. The same behavior observed while testing with the ASC was also seen while testing with the DASCs including piston amplitude noise, controller efficiency, and sensitivity to load changes. The DASCs also provides an easy-to-use environment for debugging and testing fault detection and recovery of the DCC without risk of damage to a real ASC.

C. Support Hardware

The ACU support rack, shown in Figure 5, contains hardware for starting the ACU and DASCs and providing load support when the ACU output is not connected to the RSIL loads. The test support rack consists of a startup power supply, an ACU control panel, an electronic load, a DC bus capacitance control panel, a Yokogawa WT3000

Figure 3. DASCs block diagram with user interface.

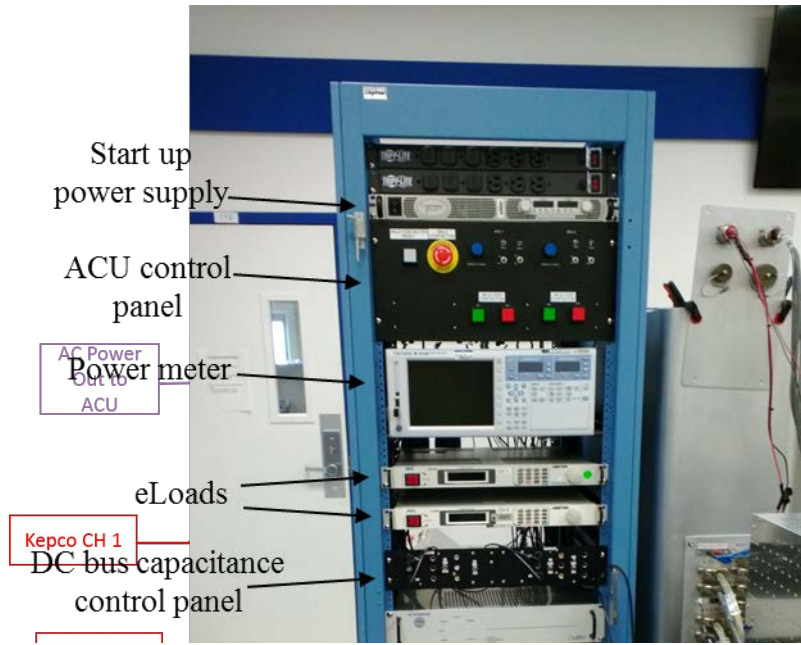
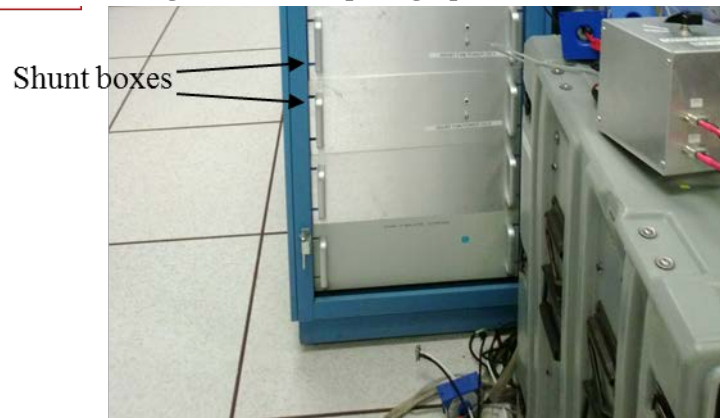


Figure 4. DASCs photograph.



power meter, and two external shunt boxes. The test support rack allows for startup and operation of two ACUs and two DASCs. The startup power supply provides power to the ACU electronics during the startup process before the DASCs output power reaches full power. The startup power supply has programmable current and voltage limits which are set to protect the ACU in the event of problems during the startup procedure. Relays on the ACU control panel are used to connect the startup power supply to the ACUs. In the current configuration, only one ACU is connected to the startup power supply at a time. When the DASCs reaches full power, the ACU control panel relays are used to disconnect the ACU from the startup power supply and the ACU electronics draw power directly from the DASCs output. The ACU control panel is also used to control the DASCs reset state and to control relays which connect the ACU outputs to the RSIL.

The electronic load is an electronic load used to dissipate power during system startup. During the startup process, the ACU output cable is connected to the electronic load. After the ACU and DASCs are operational and running at full power, the ACU output cable is manually disconnected from the electronic load and connected to the RSIL. The electronic load is capable of dissipating full ACU power. The ACU relies on a DC electronic load to sink power in an output voltage range between 22.0 and 34.0 V_{dc} which is determined by the end user. The ACU will track to this voltage, providing power as a constant-power source, and will sense a bus overvoltage condition. The ACU will provide constant power as long as the end user is in the required voltage range, but it will internally shunt power and disconnect itself from the bus if the voltage range is exceeded. Shunt resistors sized for maximum output power of the convertors are mounted in the test rack for this purpose. The bus is connected to a capacitor bank for transient energy storage that allows a range of 10,000 to 100,000 μ F.

The power meter is used to monitor and record the operating characteristics of the DASCs and the electronic load. The power meter is configured to measure AC voltage and current and analyze data during the tests. The main characteristics displayed on the power meter include the power factor, DASCs root mean square (RMS) voltage, DASCs RMS current, and DASCs output power for each DASCs channel. A total of 8 data channels for all four DASCs channels is recorded during system operation.

The DC bus capacitance control panel is used to control the charge and discharge operations of the bus capacitance. The two external shunt boxes are connected to the ACU external shunt cable. The external shunt boxes are designed to shunt all DASCs power as needed.

A capacitor bank along with a 4-pole double-throw (4PDT) switch is connected between the DASCs and the ACU. The two channel capacitor bank connects a large capacitance during the simple mode DASCs startup before it is connected to the ACU. The 4PDT switch is used to connect the DASCs output between the capacitor bank and the ACU input. This configuration allows stable DASCs operation as the DASCs is brought out of reset and then connected to the ACU.

Figure 5. ACU support rack.

The data system utilizes National Instruments' LabVIEW-based data acquisition (DAQ) hardware and software to acquire data and monitor the test. It displays and records data on a computer, collects and saves data in various time frames, and calculates parameters with received data. The ACUs are connected to the DAQ over redundant MIL-STD-1553 channels. ACU telemetry is received by the DAQ and displayed on the ACU LabVIEW command and telemetry station. The ACU LabVIEW command and telemetry station allows test operators to command the ACU operating setpoints, set ACU monitor and protection setpoints, and monitor system operations. Separate displays are provided for each ACU. The user may specify upper and lower bounds for parameters monitored by the DAQ system. Flags are set on the ACU displays in the event that error conditions are encountered. The ACU hardware is designed to protect itself and the source from faults and is not dependent on the DAQ for fault protection. Data collection allows for detailed analysis of DASCs operation. To achieve this, LabVIEW collects and displays several parameters, including

- Alternator RMS voltage, RMS current, and power
- DASCs operating frequency
- Power factor
- DASCs voltage, current and power
- A complete data record of all ACU telemetry is recorded on the DAQ. ACU telemetry is scanned at a 2-second rate.

The LabVIEW system provides an interface for commanding the ACU. These commands include:

- Changing the voltage applied to the convertor , V_{sat}
- Convertor operating frequency
- Disconnect from the spacecraft
- Connect to the spacecraft

III. RSIL

RSIL the RSIL is comprised of five major components designed to simulate a prototypical spacecraft which may be powered by a RPS feeding a set of electrical loads. The major components shown in Figure 6 are: up to 3 RPS power sources, a power management and distribution system (PMAD), an energy storage system (i.e. bus capacitor, battery or super capacitor), electrical load simulators, and a flight control computer simulation. This integrated electrical system tests RPS generators as part of an end-to-end spacecraft system rather than as stand-alone power generators. RSIL's spacecraft simulation capabilities encompass:

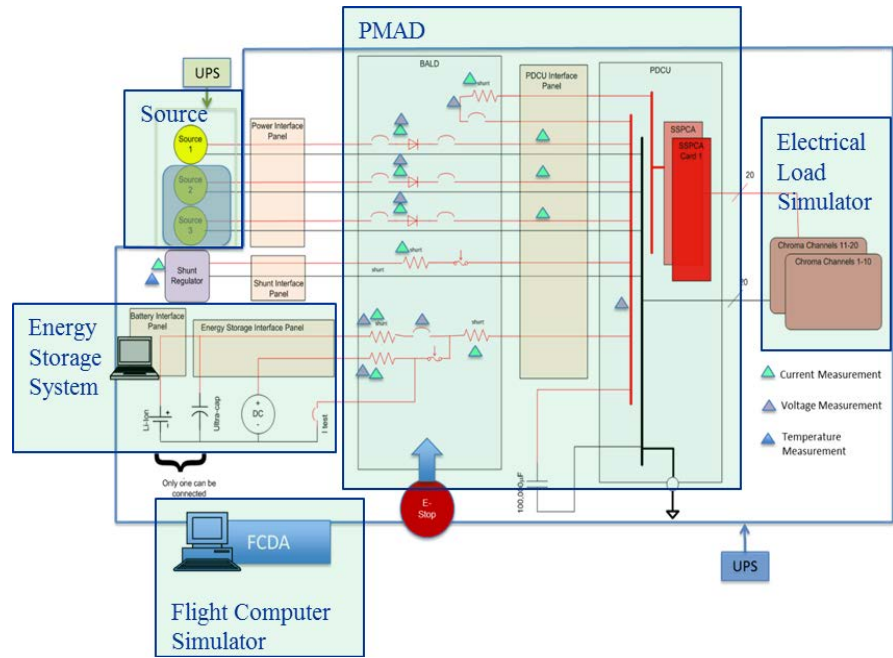


Figure 6. RSIL system architecture.

- Generators: 1, 2, or 3 200W RPS generators.
- Energy Storage: 100,000 µF bus capacitor, 165F supercapacitor, or 24A-hr Li+ battery
- Electrical Loads: 20 channels at 100W each.
- Main Bus:
 - Regulation: ± 0.05 volts with power shunt engaged.
 - Control Range: 22 to 38 volts (26 to 33 with Li+ battery)
- Battery Charging: Adjustable rate limit 2 to 25 amp.

The power management and distribution subsystem consists of an interface unit, power distribution and control unit (PDCU) utilizing solid-state power controllers (SSPCs) for load switching, and a shunt regulator unit (SRU) to shunt excess power not used by the loads and to regulate charging of the energy storage device. The electronic load bank consists of 20 independent channels configurable as either constant resistance, constant current, constant power or constant voltage. An overall LabVIEW-based facility control and data acquisition system (FCDA) manages the data storage and display. The RSIL can be configured in 3 ways: 1) stand-alone bus capacitor, 2) bus capacitor with a battery unit, and 3) bus capacitor with a supercapacitor. Since the ASC's are constant power sources, the energy storage unit is used to provide power at times when the load demand exceeds the source capabilities.

In addition to these components, the RSIL incorporates a relay based electrical safety system in the event of system failures. The control panel, which monitors various system signals, and associated alarm panel is shown in Figure 7. The safety system includes 2 levels of safety: alarms and shutdowns, with the emergency shutdown logic shown in Figure 8.

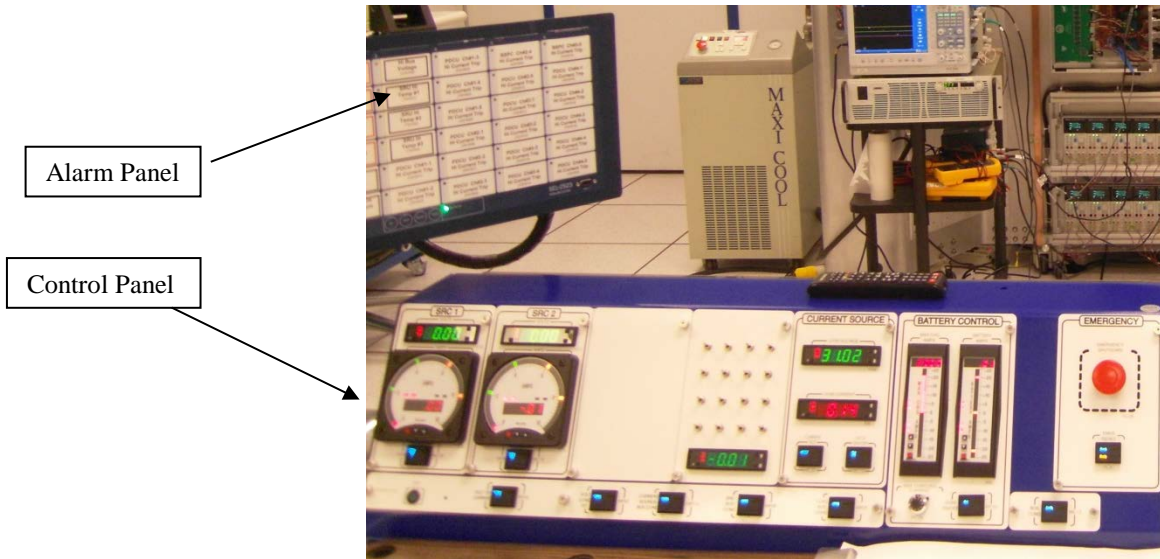


Figure 7. Control and alarm panels.

Electric power distribution system parameters (voltages, currents, and temperatures), are continuously monitored for out-of-tolerance operation. In the event of an unsafe parameter reading, the monitoring system provides audible and visual alarms. The RSIL operator is responsible for correcting the out-of-tolerance condition or halting the test sequence to determine the cause of the excursion.

Electrical power parameters that are out-of-limit trigger an automatic emergency shutdown procedure, again with associated audible and visual alarms. A shutdown can also be initiated by the RSIL operator. The emergency shutdown procedure for RSIL is:

1. Remove all energy sources from the spacecraft simulator via mechanical contactor.
2. Disconnect all loads from the RPS via a mechanical contactor.
3. Notify RPS test director of the event.

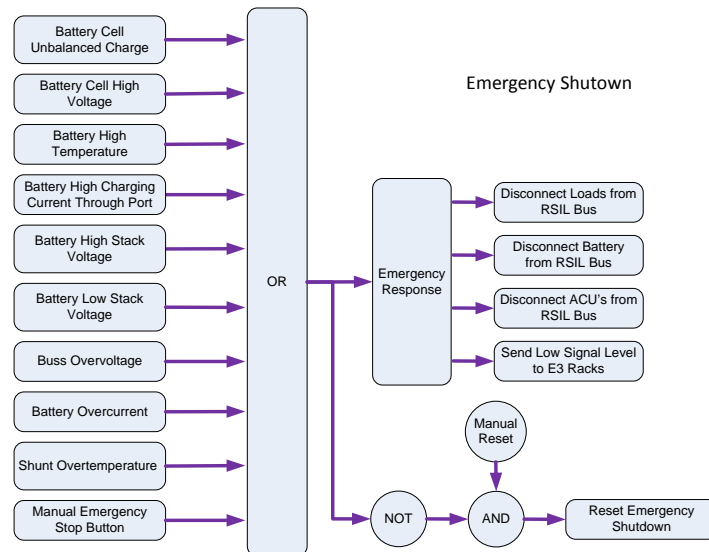


Figure 8. Emergency shutdown diagram.

IV. Testing

Testing with the ACU in RSIL was performed in both single input and dual input configurations. Single input testing consisted of one ACU, one DASCS connected on one RSIL input channel. The results of the two single input

channel tests are not presented in this paper for brevity. The ACU operated as predicted with the ACU maintaining control of DASCS, and RSIL managing the power bus via energy storage and dissipative loads. Each of the two input channels were tested separately before operating with two RSIL inputs.

The dual input testing consisted of two ACUs and two DASCS's as parallel inputs to the RSIL. Two ACUs were built by LMCT and are referred to as EDU 4.0 and EDU 4.1. A photograph of the test setup is shown in Figure 9 and a block diagram of the setup is shown in Figure 10.

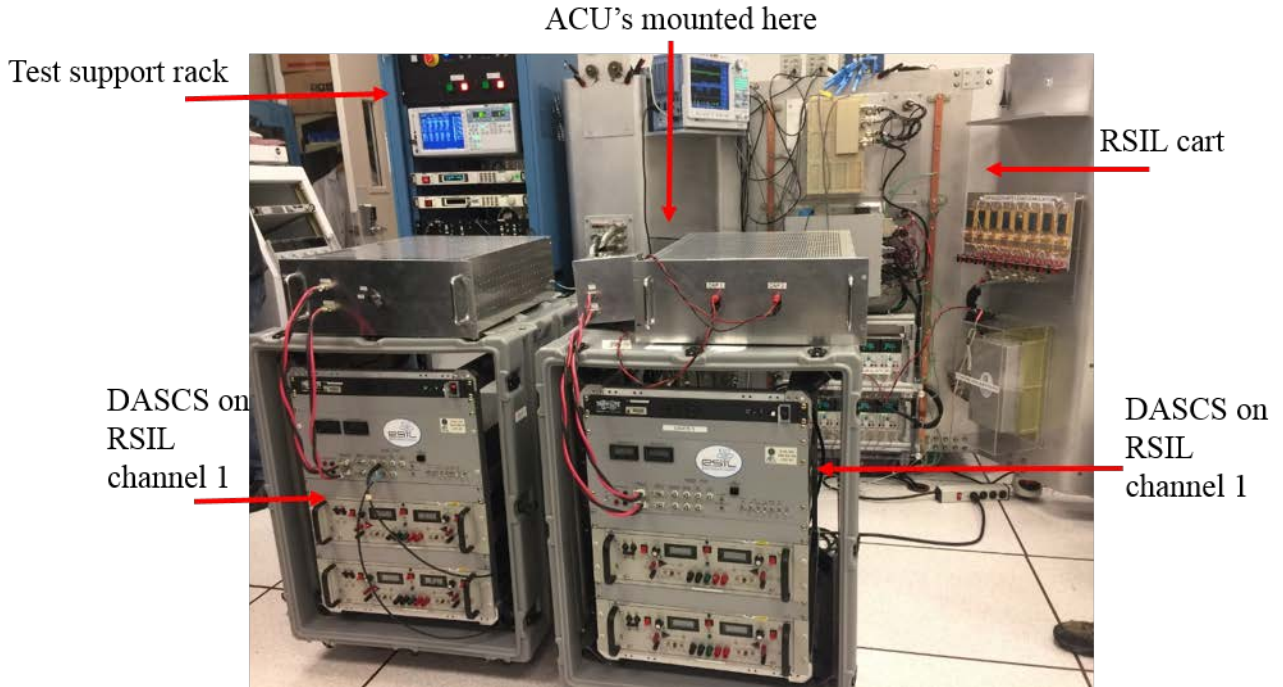


Figure 9. RSIL and RPS setup.

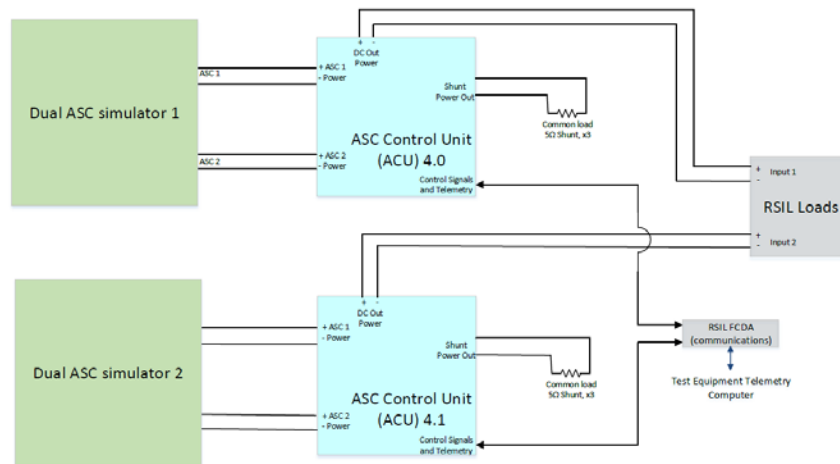


Figure 10. Block diagram of dual input channel test setup.

The tests listed in Table 1 were performed both for the single and dual input channel tests. All of the dual input channel test results are not presented in this paper for brevity but only those highlighted in yellow will be presented. The four main tests included load step change, load profile, voltage limit, and short circuit.

- 1) The load step change test verified the RSIL's ability to respond to a change in the load demand. It also verified that the ACU and ASC were not impacted by this load change. Step changes in electrical load were executed using the Chroma programmable loads using the following settings:

- Constant power load
 - Constant resistance load
- 2) A load profile, based on data from several representative missions, tested the RPS and RSIL ability to maintain operation during load demands above and below the power provided by the RPS. The load profile used during the tests is shown in Figure 11. This profile was executed at bus voltages of 26, 28 and 32 V and spacecraft loads consisting of constant power, constant resistance and a combination of constant power and constant resistance. When the RSIL required more power than the RPS could accommodate, the energy storage device (supercapacitor or battery) supplied the additional power. When the RSIL demanded less power than what the source provided, the shunt regulator unit dissipated the excess power.

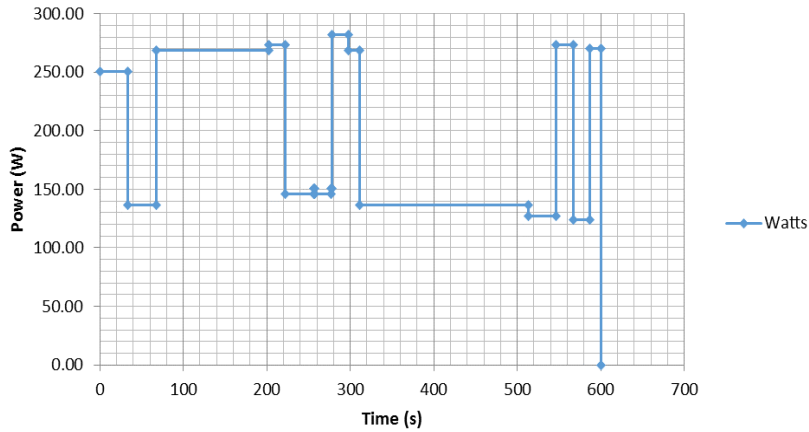


Figure 11. RSIL dual input channel load profile.

- 3) The voltage limit tests verified the ACU's ability to go into a constant current mode when below the acceptable DC bus voltage level of 22 V. Above the acceptable DC bus voltage range of 34 V, the ACU disconnects and shunts the power in its external shunt resistors.
- 4) The short circuit test verified the RSIL's ability to respond to a short on one of the loads. For the short circuit test, a switch-operated Insulated Gate, Bipolar Transistor (IGBT) was connected across the inputs to a Chroma load with the IGBT's emitter connected to the power return. When the IGBT's gate was energized, the device shorted the high side of the Chroma's input to the return power connection. Shorting events were induced manually by the RSIL operator. The IGBT used was a Fuji Electric 1MBI400-060 unit with ratings of 400 amps, 600 volts.

Table 1. RSIL tests.

Energy Storage	Test
Capacitor	
	Constant Power Load Step Change
	Constant Resistance Load Step Change
	Short Circuit on Constant Power Load
	Short Circuit on Constant Resistance Load
	Constant Power Load Profile at 26, 28, & 32 V
	Constant Resistance Load profile at 26, 28, & 32 V
	Constant Power and Constant Resistance Load Profile at 26, 28, & 32 V
	Upper Voltage limit
	Lower Voltage Limit Constant Power Load
	Lower Voltage Limit Constant Resistance Load

Supercapacitor	
	Constant Power Load Step Change
	Constant Resistance Load Step Change
	Short Circuit on Constant Power Load
	Short Circuit on Constant Resistance Load
	Constant Power Load Profile at 26, 28, & 32 V
	Constant Resistance Load profile at 26, 28, & 32 V
	Constant Power and Constant Resistance Load Profile at 26, 28, & 32 V
	Upper Voltage limit
	Lower Voltage Limit Constant Power Load
	Lower Voltage Limit Constant Resistance Load
Battery	
	Constant Power Load Step Change
	Constant Resistance Load Step Change
	Short Circuit on Constant Power Load
	Short Circuit on Constant Resistance Load
	Constant Power Load Profile at 26, 28, & 32 V
	Constant Resistance Load profile at 26, 28, & 32 V
	Constant Power and Constant Resistance Load Profile at 26, 28, & 32 V

Table 2 lists the power levels on each channel. The power provided to RSIL is approximately 20 W less than that provided by the DASCS due to line loss and housekeeping power required by the ACU. Prior to connecting to RSIL, the DASCS's are brought to full power operation with the ACU dissipating power in external shunt resistors (as described in section II.D). When steady state operation of the DASCS's is achieved, a command is sent to the ACU to connect to RSIL.

Table 2. RSIL bus voltage and current for dual input channel supercapacitor bus testing.

Input Channel	EDU	DASCS Power	RSIL Power (W)
1	4.0	149	132
2	4.1	150	132

A. Capacitor bus

The test results presented for the capacitor bus energy storage configuration include upper voltage and under voltage limit testing. For the upper voltage limit test, the bus voltage was raised above 34 V to verify the ACU's ability to disconnect from the bus when out of range from its designed bus voltage range. The results of this test are shown in Figure 12 to Figure 15. The ACU successfully disconnected and then returned to nominal operation when the bus voltage was back in range.

Figure 12 and 13 show that as the bus voltage increased to 34.5 V, the ACU began shunting DASCS power in the external shunt resistors. Figure 16 and Figure 17 shows that each DASCS continues to supply power through the upper voltage event.

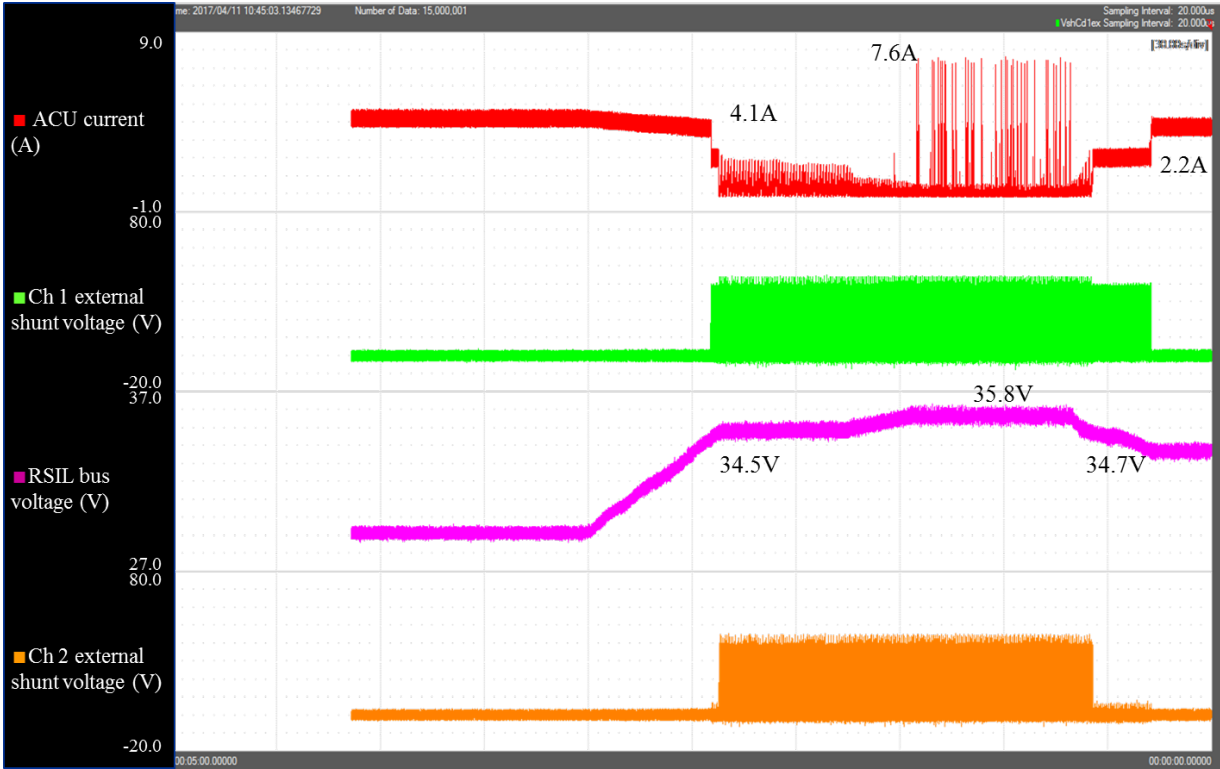


Figure 12. Bus capacitor upper voltage limit and recovery test current performance data channel 1.

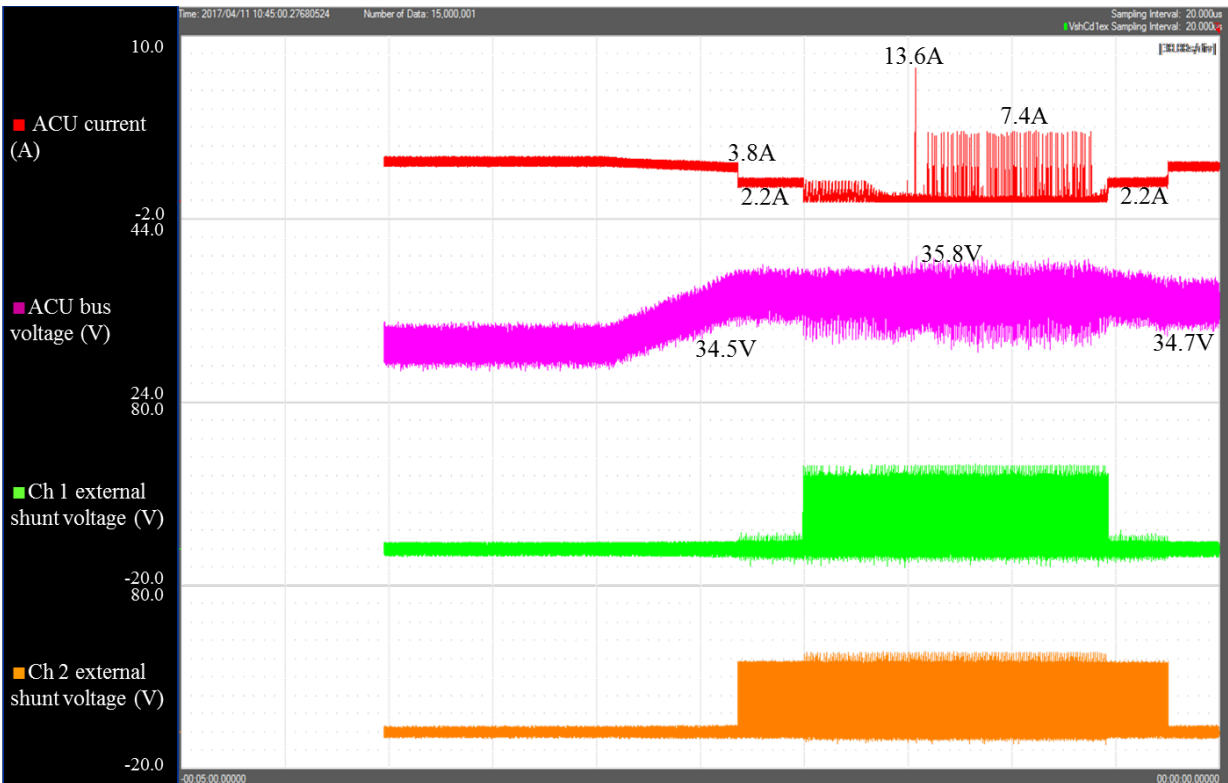


Figure 13. Bus capacitor upper voltage limit and recovery test current performance data channel 2.

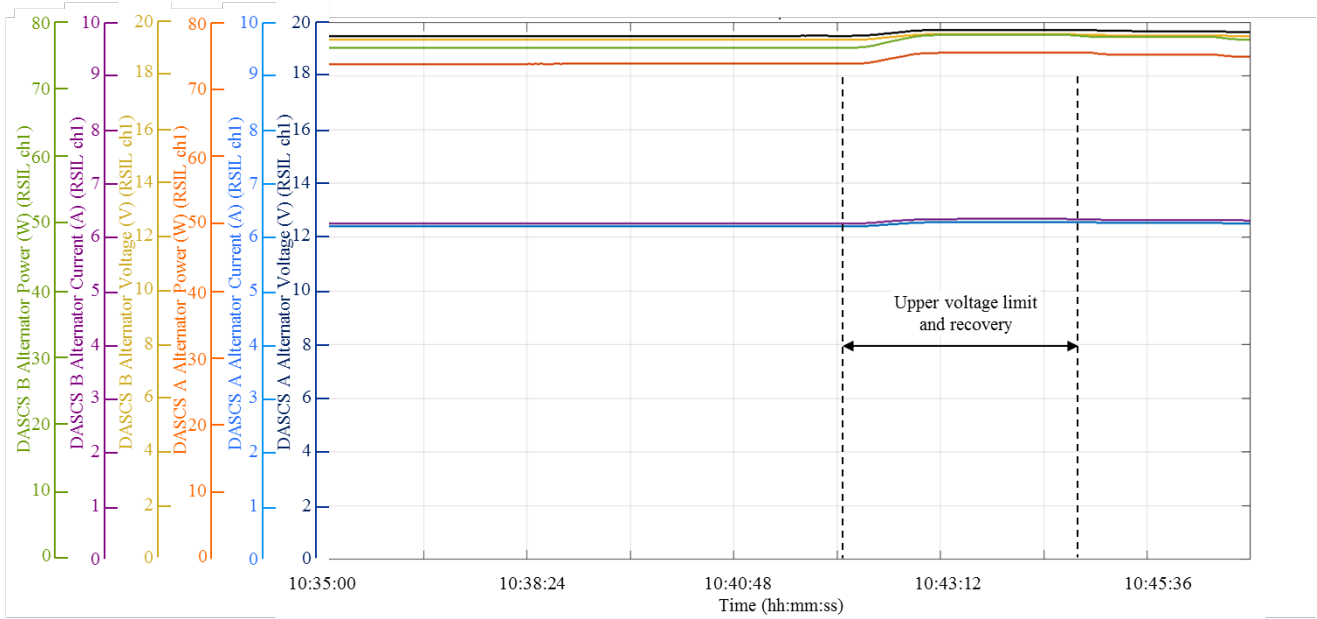


Figure 14. Bus capacitor upper voltage limit and recovery channel 1 test DASCS performance data.

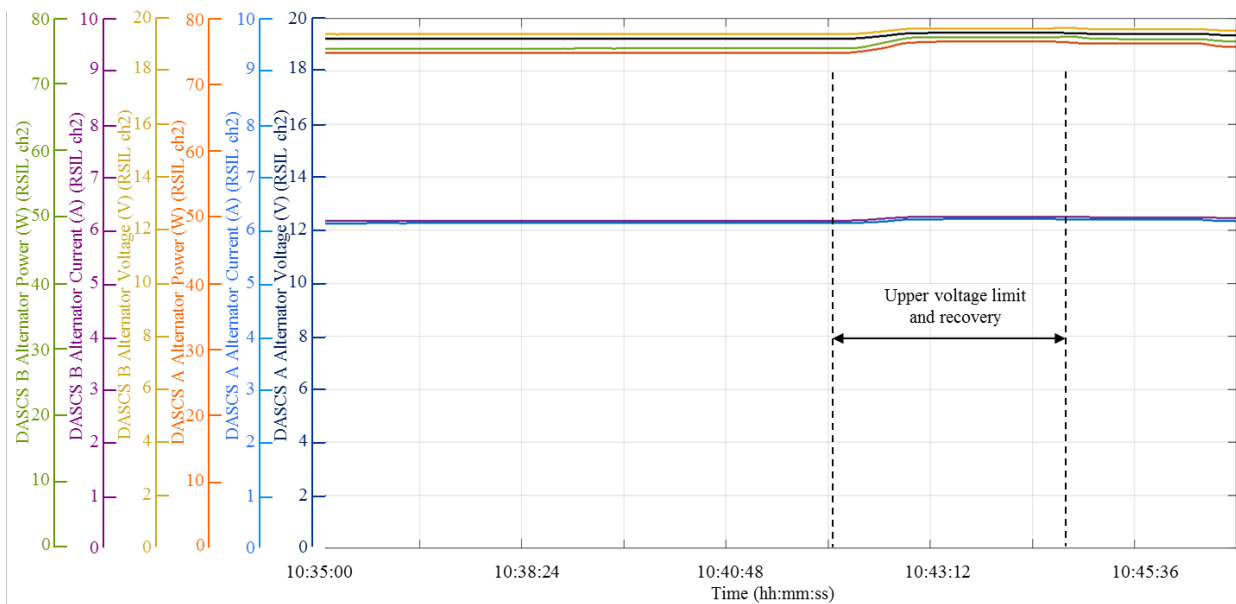


Figure 15. Bus capacitor upper voltage limit and recovery channel 2 test DASCS performance data.

For the lower voltage limit test, the bus voltage was decreased below 22 V to verify the ACU’s ability to enter a dead bus recovery mode and supply a constant current of approximately 4.6 A in an attempt to raise the bus voltage back to a normal level. When the bus voltage returns to its nominal operation, the ACU exits dead bus recovery mode and all power is provided to the spacecraft. The results of this test are shown in Figure 16 to Figure 19. The ACU successfully entered dead bus recovery mode and exited when the bus voltage was back in range.

Figure 18 and Figure 19 shows the oscilloscope traces as each ACU recovers from dead bus mode in a constant power configuration. The plots show that the ACU current is in constant current mode at 4.7 A as the RSIL bus voltage is increased. When the RSIL bus voltage reaches approximately 20.6 V, the ACU comes out of dead bus mode and the ACU current increases to 6.3 A. As the bus voltage drops, the ACU goes into a constant current mode as shown on the oscilloscope plots with the ACU current dropping to 4.7 A. With the RSIL loads in a constant power configuration, the bus voltage dropping, and the ACU entering a constant current mode, the RSIL loads begin drawing additional current. The constant power loads cause a quick dip in the bus voltage resulting in a 33 A spike in the load

current. This additional current is supplied by the quick discharge of the bus capacitor. It is seen from the oscilloscope plots that the system quickly recovers from this transient and the ACU maintains control of the DASCs. Figure 16 and Figure 17 shows that each DASCs continues to supply power through the low voltage event. When the ACU goes into dead bus recovery, the ASC output power increases by approximately 2 W and then returns to its nominal power level when exiting dead bus recovery. LMCT believes that this slight variation in ASC output power is caused by the lack of AC voltage feedback in the ACU. Without the AC voltage feedback, the ACU is not able to precisely track the ASC output power as the bus voltage drops. As seen in the data plots, this is a temporary condition and the ACU quickly recovers and brings the output power back to the normal level. LMCT recommended adding AC voltage feedback to the ACU in any future developments. During the single input channel testing, it was learned that the dead bus recovery mode was not functioning properly and was repaired prior to the dual input channel testing. This is discussed in Section V in detail.

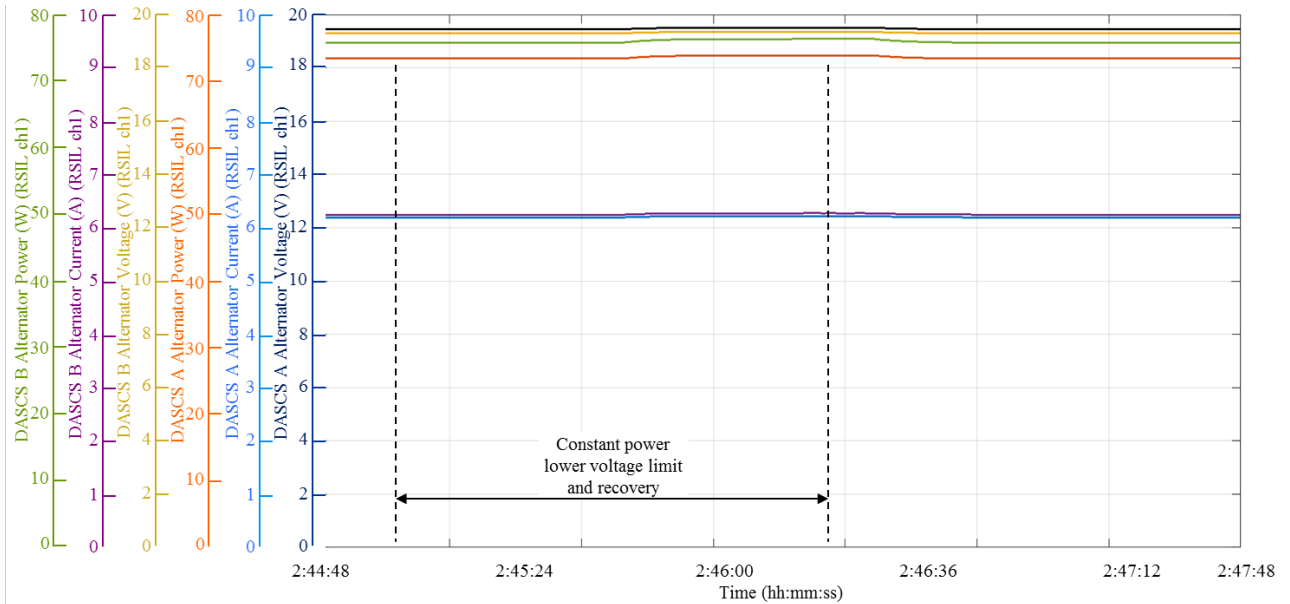


Figure 16. Bus capacitor lower voltage limit and recovery test DASCs channel 1 performance data.

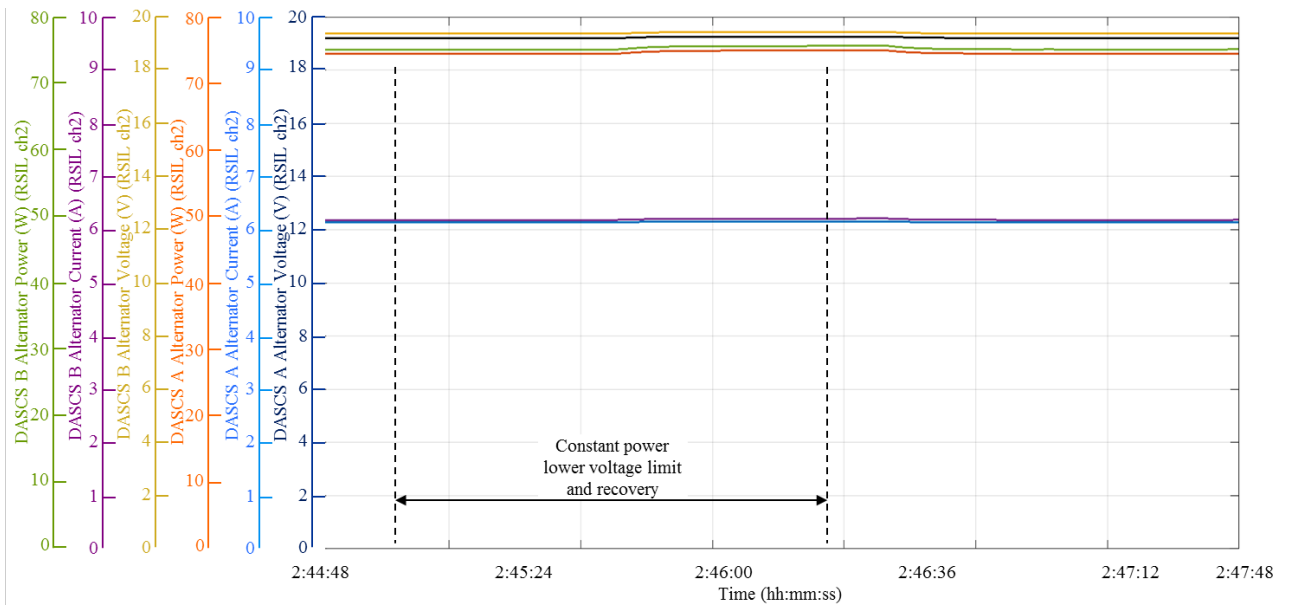


Figure 17. Bus capacitor lower voltage limit and recovery test DASCs channel 2 performance data.

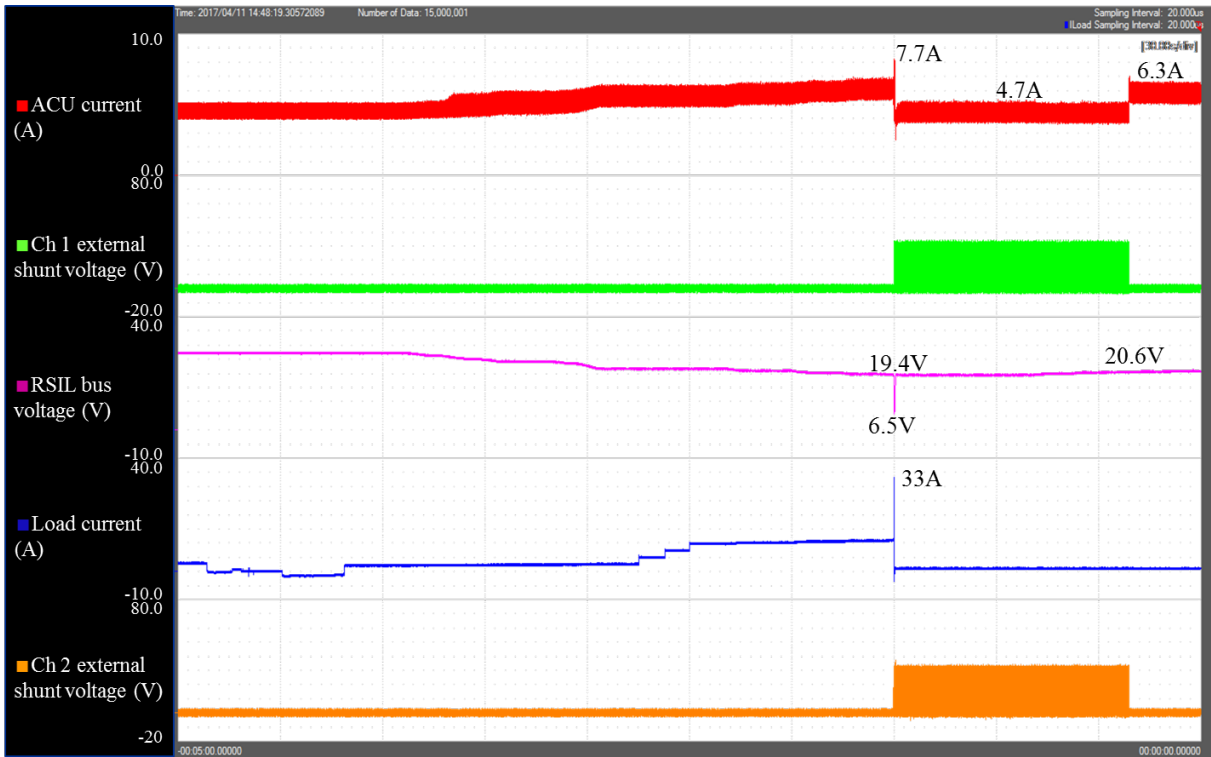


Figure 18. Bus capacitor lower voltage limit and recovery test current performance data channel 1.

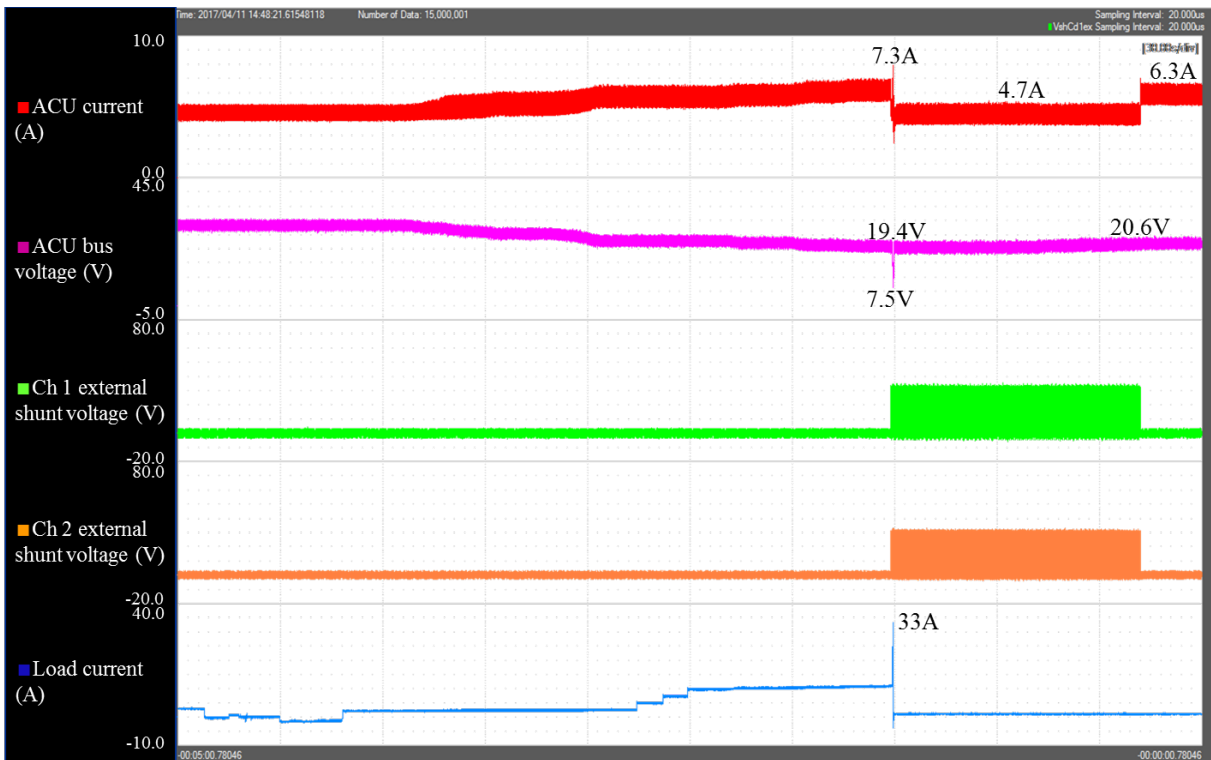


Figure 19. Bus capacitor lower voltage limit and recovery test current performance data channel 2.

B. Supercapacitor bus

The load profile test, performed over a period of ten minutes, was performed at bus voltages of 26, 28 and 32 V to illustrate system operation over a typical 28 V spacecraft bus operating range. The results of the load profile tests are shown in Figure 20 to Figure 22 showing RSIL shunt and energy storage device (supercapacitor) either dissipating or supply additional power as the spacecraft load demand changes. The DASCs output power, as shown in Figure 21 and Figure 22, changes with the bus voltage due to the lack of AC voltage tracking as discussed in Section IV A. The RPS and RSIL operated in the manner expected with the ACU maintaining control of the DASCs and RSIL providing extra power as required by the load via energy storage and dissipating power via the shunt regulator.

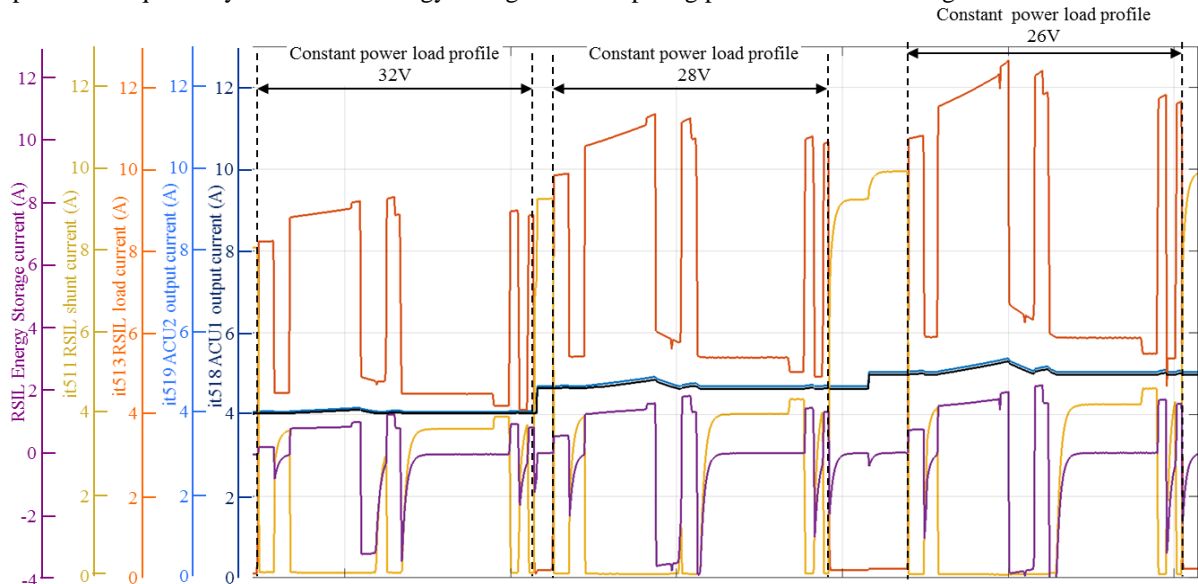


Figure 20. Supercapacitor load profile test current performance data.

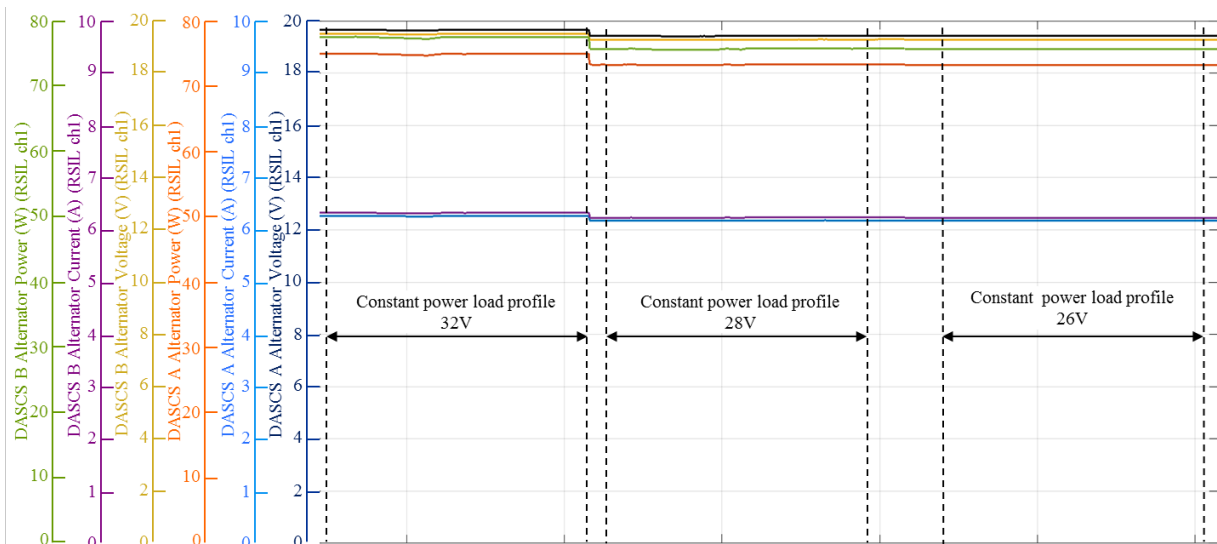


Figure 21. Supercapacitor load profile test DASCs channel 1 performance data.

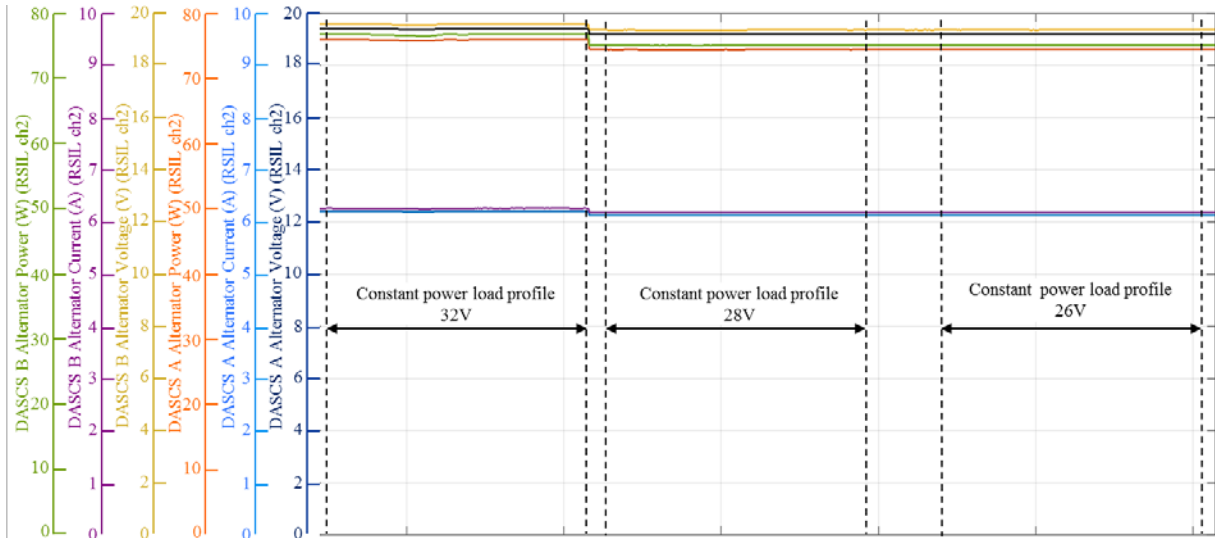


Figure 22. Supercapacitor load profile test DASCs channel 2 performance data.

C. Battery bus

The test results presented for the battery energy storage configuration include spacecraft load step and spacecraft load short testing. These tests were performed at a nominal bus voltage of 28 V. For the load step test, a positive 150 W step load change, seen in Figure 23 and Figure 24, was initiated and then the load was removed. Figure 25 and Figure 26 show the DASCs response during the spacecraft load step test. No disturbances were observed at the sources for either of the tests.

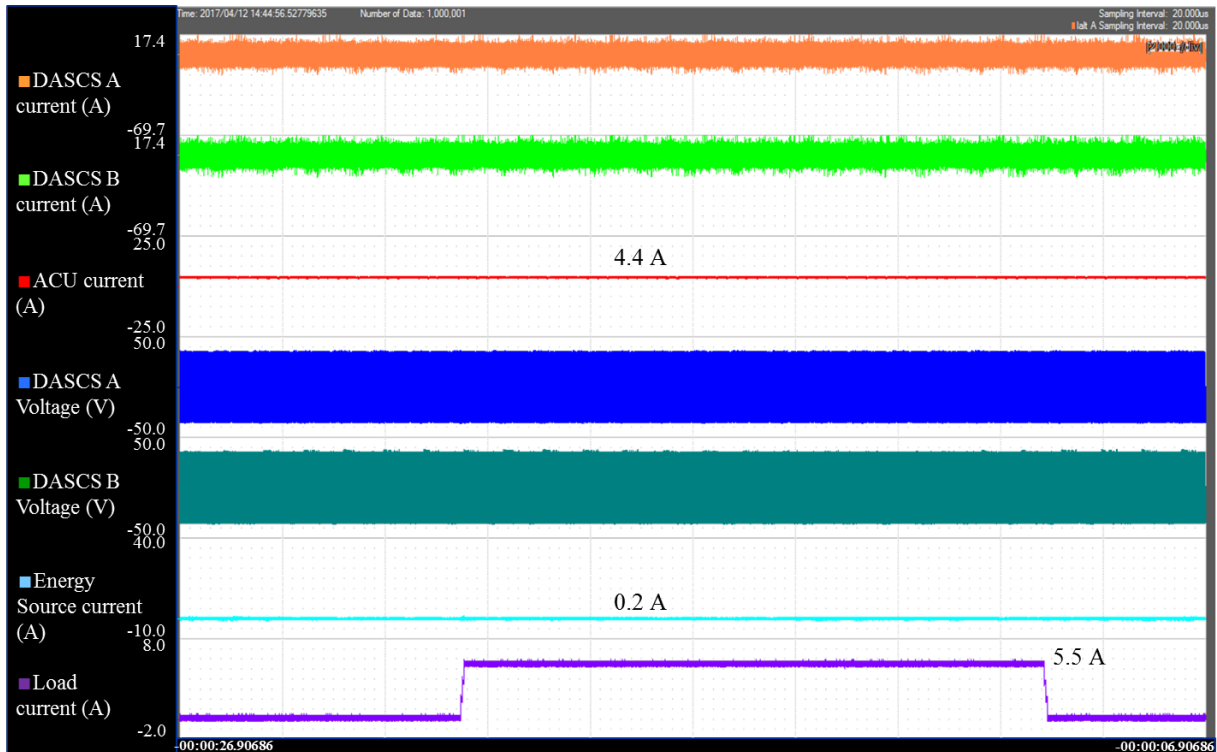


Figure 23. Battery step load change test channel 1 performance data.

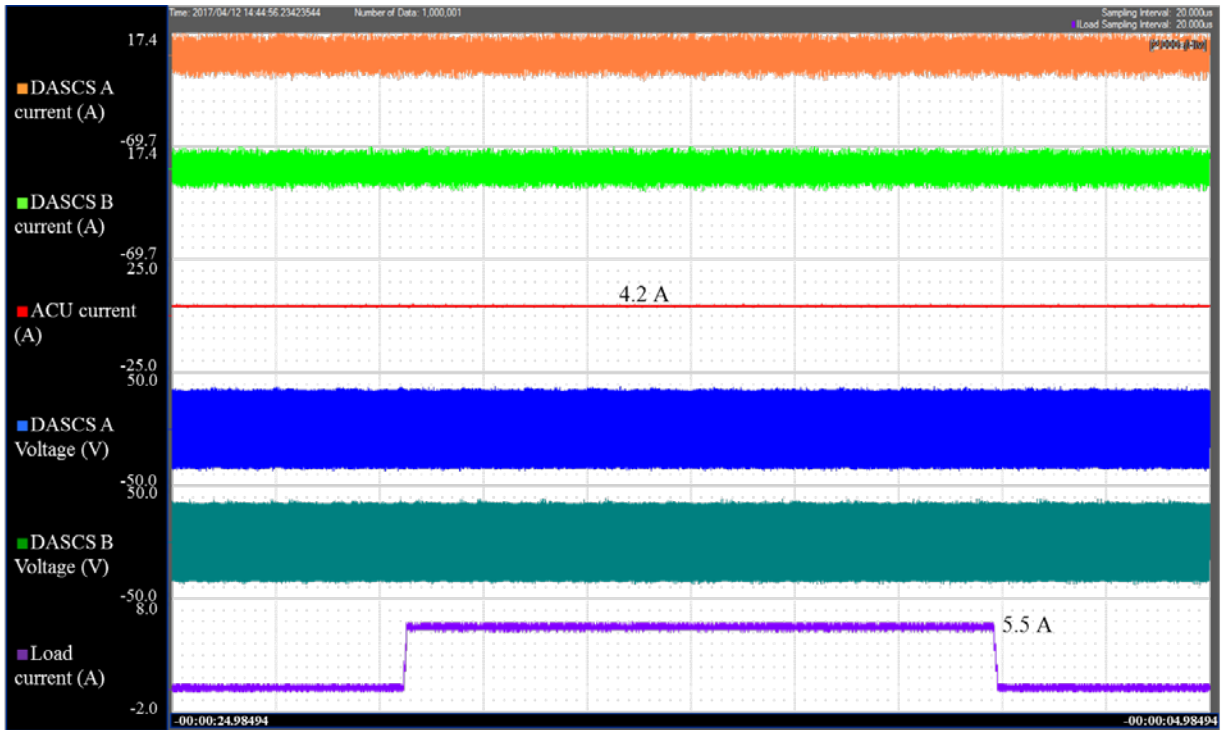


Figure 24. Battery step load change test channel 2 performance data.

For the short circuit test, one load channel was set to 90 W and then shorted. The oscilloscope was set to trigger when the short was initiated. Figure 25 and Figure 26 shows that the DASCs operation was not impacted by the short and that the load and energy source current increased to 82 A and 62 A respectively. No disturbances or abnormalities were seen at the source and all systems operated as expected.

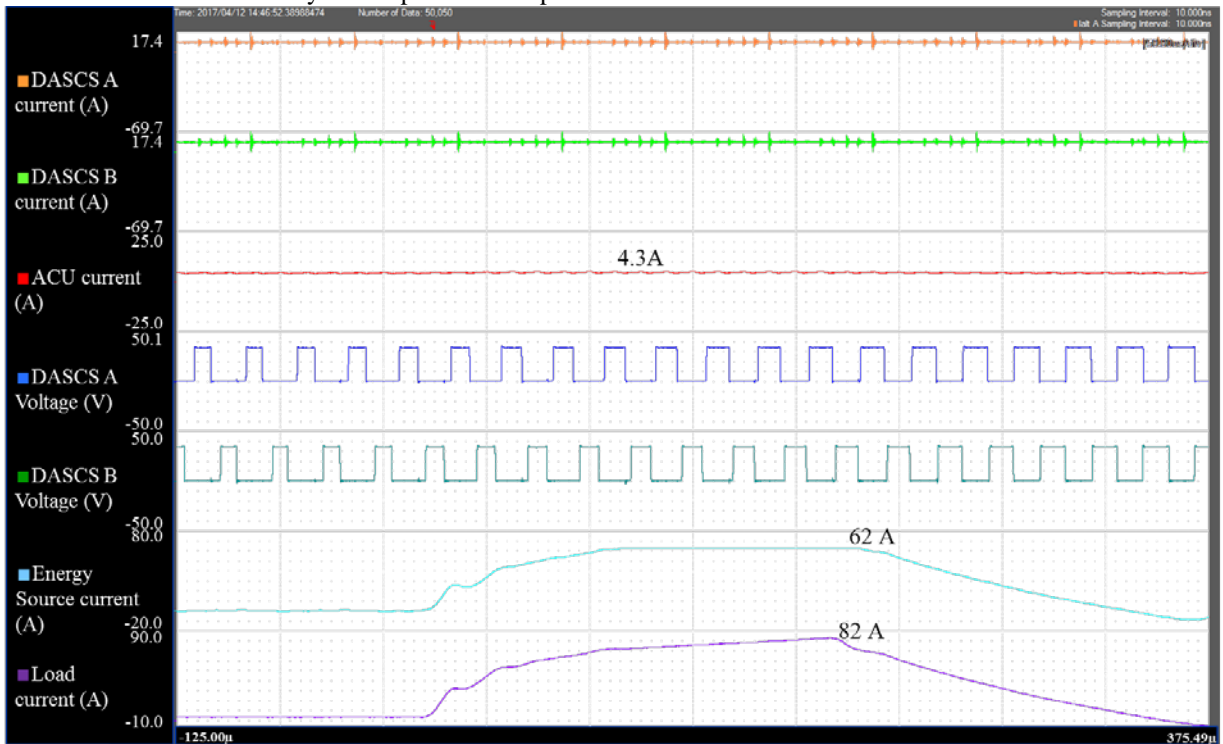


Figure 25. Battery load short test channel 1 performance data.

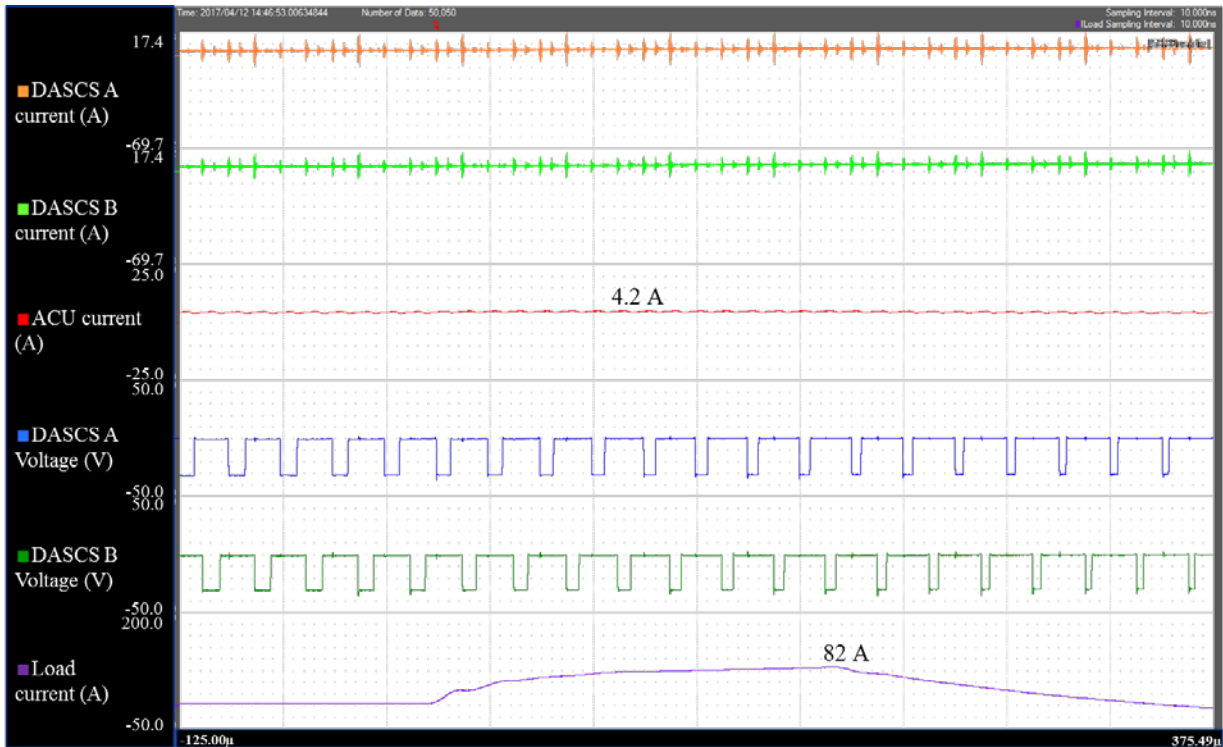


Figure 26. Battery load short test channel 2 performance data.

V. Lessons Learned

Two issues were identified with the dead bus recovery mode of the ACU during single input channel testing. First, a large current spike was sometimes produced on the DC output of the ACU when going into dead bus recovery mode. In addition to the large current spike, it was later learned that the power out of the ASC must be greater than 68.4 W for the ACU to recover from dead bus recovery mode.

A. Current Spike Lesson Learned

Two events need to happen to turn off the DC output. The Pulse Width Modulated (PWM) signal driving the output switches needs to cease switching and a one-shot shutdown signal needs to be sent. This one-shot signal energizes a clamp that shorts the gate-source voltage of the high side MOSFETs thereby shutting off the DC output. Testing with RSIL showed that during specific operating conditions, the FPGA did not produce the necessary one-shot clamp signal. When this happened, the MOSFET gate-source voltage was not being clamped and the current would run unconstrained out of the ACU to the simulated RSIL spacecraft bus. Often the unconstrained current would peak around 80 Amps as it would only be limited by the small resistance of the DC output circuit.

Figure 27 shows the high level circuit diagram of the DC output daughter card circuit that was added to the ACU to fix the current spike issue. In this circuit, a copy of the current sense is routed to a comparator. The other input to the comparator is a set point above normal operation that represents a current level at which the comparator should react and shutdown the DC output. The set point chosen was well above the normal operating point so that noise would not cause false trips but also low enough that the output inductor would not saturate and would therefore control the output current level rise. Once the comparator is tripped, it triggers a one shot circuit to the clamp and at the same time disables the PWM signal. These two signals are paired with AND and OR logic devices so that these signals coming from the FPGA can route straight through this board during normal operation.

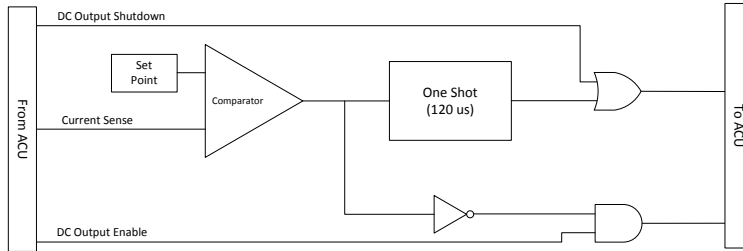


Figure 27. DC output daughter card circuit.

After this circuit was installed onto the controller cards, normal operation of the ACU was checked first to ensure that there were no new issues introduced by the daughter cards. The second part of the testing was to recreate the conditions in which the overcurrent spike was first observed and ensure the newly installed boards corrected the anomaly. The rework was completed in two phases to reduce risk.

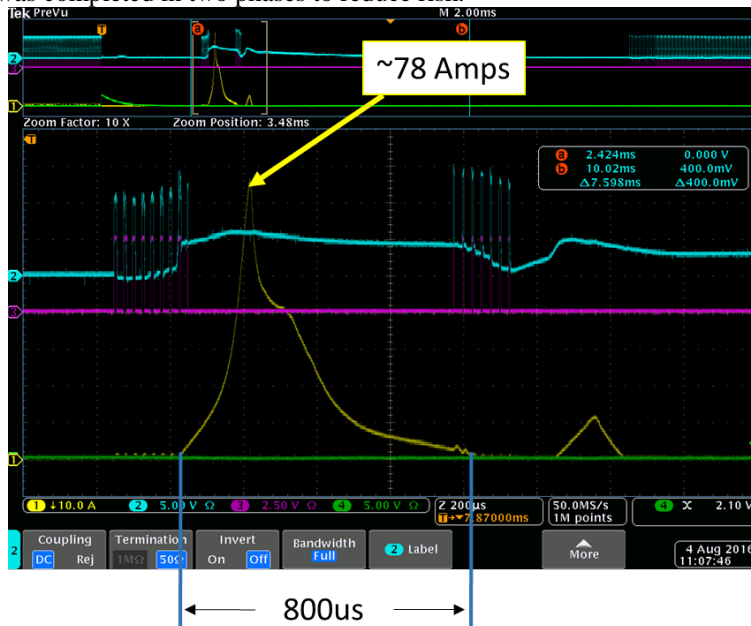


Figure 28. DC output current anomaly before fix.

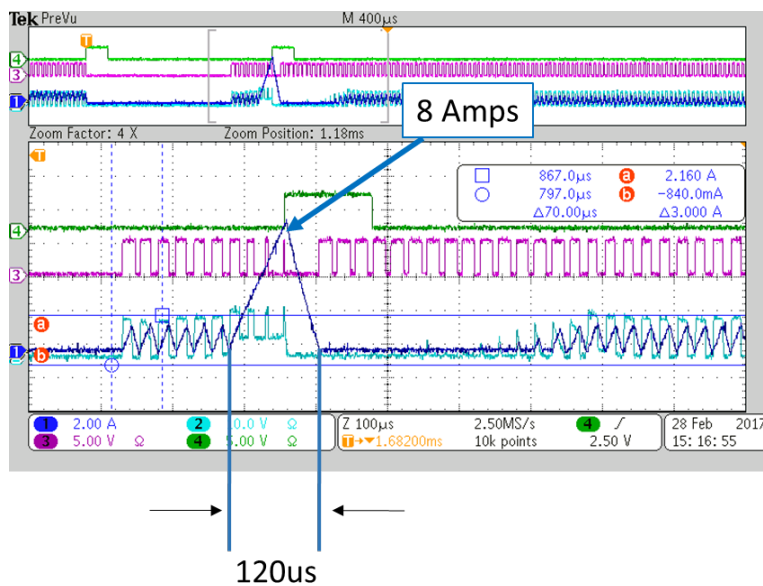


Figure 29. DC output after daughter card implementation.

B. Dead Bus Recovery Power

The second lesson learned was that low levels of AC input power from the DASCs, would not allow the spacecraft bus to be driven from dead bus mode to normal bus mode. The problem was found to be a requirements issue. While in dead bus mode, the original requirement stated that the ACU shall provide a constant level of output current (1.75 A) until the spacecraft bus goes above 22 V and the ACU returns to normal operation which is to provide constant power. In order to ensure that the requirement is met over the ACU lifetime, the constant current set point was hardcoded into the FPGA to be 2.25 A. In dead bus mode, the ACU also uses about 20 W of input power below which it will not output any DC power in order to ensure survival. This means that with the present implementation, to recover from dead bus, the minimum AC input must be: 21.5 V (max dead bus voltage) x 2.25 A (dead bus current) + 20 W (ACU overhead power) or 68.4 W.

An FPGA effort is underway to change the requirement to allow the current to fold back from the 2.25 A a hardcoded number as the voltage rises towards normal operation. For example if only 60 W is available at the ASCs, the FPGA will still reserve 20 W for safe ACU operation and will still try to supply 2.25 A where possible, but at 21.5 V or just before entering normal mode, the dead bus current will have reduced to about 1.85 A.

VI. Conclusion

The results of this test sequence verified correct operation of the ACUs in an electrical spacecraft simulator, both during normal operation and off-nominal conditions. The short circuit, overvoltage, under voltage and load step transients provided by RSIL were effectively managed by the ACUs and DASCs, proving the technology for future advancements in Technology Readiness Level.

Acknowledgments

This work is funded through the NASA Science Mission Directorate. Any opinions, findings, and conclusions or recommendations expressed in this paper are those of the authors and do not necessarily reflect the views of NASA. The authors wish to acknowledge the ACU and RSIL development teams of Casey Theman, Don Fong, Chris Miller, and James Dolce, Lockheed Martin personnel, JHU/APL personnel and Thermal Energy Conversion Branch personnel for their invaluable input and technological expertise.

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