

# Packaging Technology for SiC High Temperature Electronics

## - Most Recent Progress

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# Packaging Technology for SiC High Temperature Electronics

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## Outline

### Background

- SiC high temperature electronics/sensors in R&D for aerospace applications
- Packaging systems
  - Concepts/functions
  - Conventional electronic packaging material issues at high temperature

### HTCC packaging system for high temperature application

- HTCC alumina, Pt/HTCC alumina prototype package and PCB
- Parasitic parameters of a 32-I/O package

### Recent test results

- Test results with SiC ICs at 500 and 700°C
- Test results with SiC ICs in simulated Venus environment

### Summary

### Acknowledgements

# Background: High Temperature Devices and Packaging

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## Background

500°C SiC electronics and MEMS sensors have been demonstrated

- JFET ICs, MEMS based pressure sensor and Schottky diode based gas chemical sensors
- Applications include aerospace engine control and long term Venus probes
- Packaging system needed for device application and long term test

Failure mechanisms of conventional packaging materials at high temperatures

- Plastic materials melt, de-polymerize, and burn at high temperatures
- Conductor and alloys (solder) melt and oxidize rapidly at high temperatures
- High thermal stress due to thermal expansion mismatch - mechanical failure at structure level
- Challenges at material and structure levels

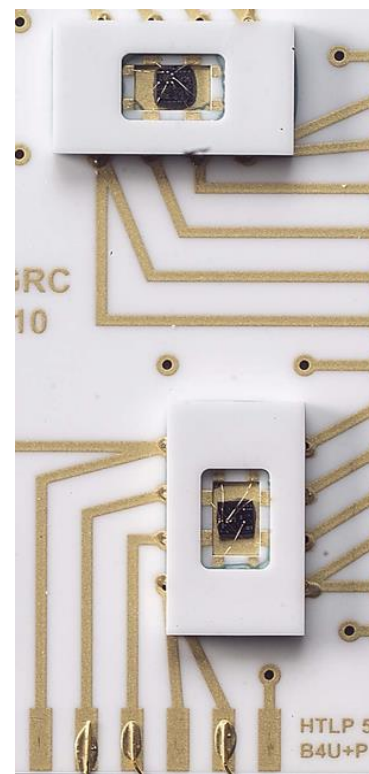


## Background: Packaging Concepts

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### Packaging Technology for Electronics/Sensors

- Packaging is essential to microelectronics and sensors
  - Mechanical support
  - Electrical interconnection
  - Electromagnetic, chemical environment
- Chip-level packaging
  - Substrate and metallization
  - Die-attach
  - Wire-bonding
- Printed Circuit Board (PCB)
  - Interconnecting packaged chips and passives
- PCB edge connectors
  - Subsystem level packaging
- Sensor packaging may include some of these elements but in different format



# Co-fired Alumina High Temperature Packaging System

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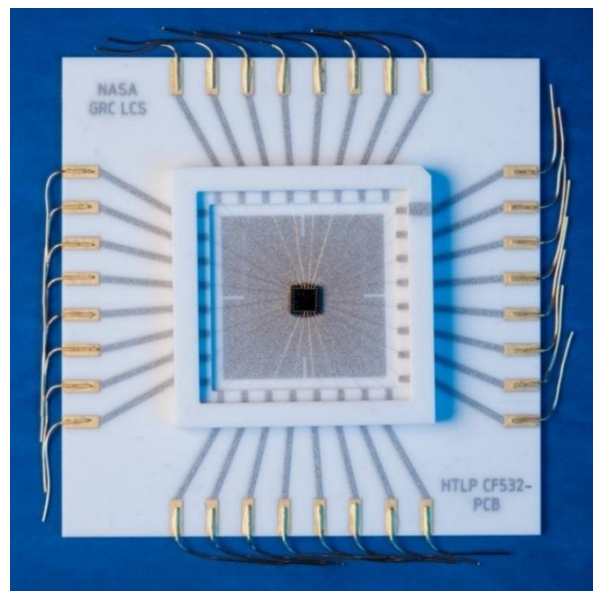
## High temperature co-fired (HTCC) alumina

- Co-fired at  $T > 1500^{\circ}\text{C}$
- A few percent of glass used in co-fired alumina systems
- Metallization for conventional co-firing process
  - Low CTE ( $8.8 \times 10^{-6}/\text{C}^{\circ}$ ) high melting point metals/alloys
  - W, Mo, MoMn co-fired in noble gas
- Dielectric performance of selected HTCC alumina tested at high temperatures in 2012

## Pt metallization

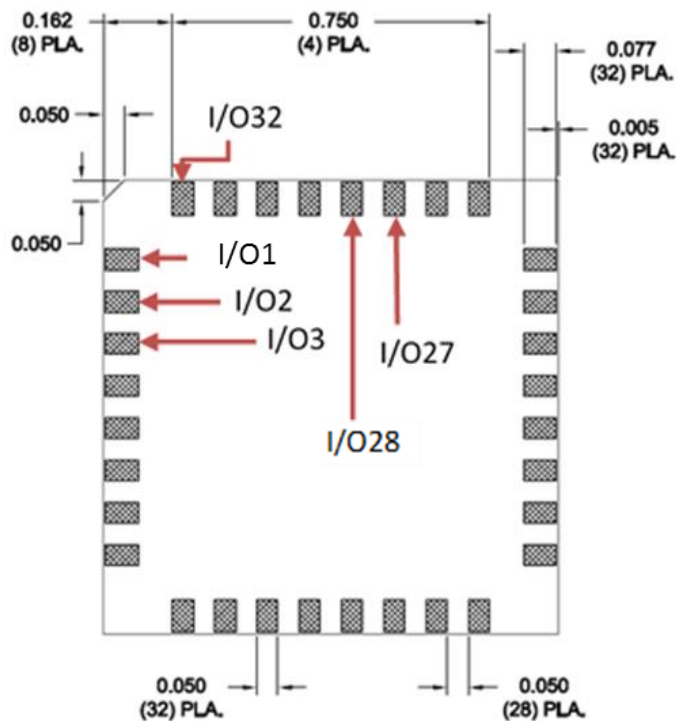
- Low CTE
- Chemically stable, co-fired in air
- Alloy with Au, Au is always surface rich at elevated temperatures
- Aluminum oxide as binder - thermodynamically more stable compared with glasses

## Test Assembly of a SiC IC with HTCC Alumina Packaging System



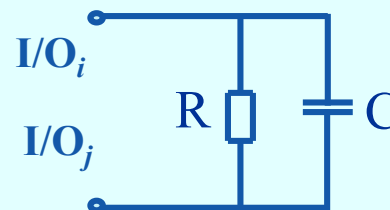
- Packaged SiC chip with Pt/HTCC alumina package and PCB
- PCB measures 2 inch x 2 inch, Pt traces co-fired with alumina
- 1 mil Au alloy wire thermo-sonically bonded
- High temperature die-attach

## Parasitic R//C of Neighboring I/Os



1.07 inches

### Parasitic Equivalent



### R//C model

R – DC leakage and AC dielectric loss

C – Dielectric polarization

$$1/Z(T, \omega) = G(T, \omega) + j\omega C(T, \omega)$$

R//C measured between I/O1 - I/O2, and I/O2 - I/O3

- I/O1 connected to all five bias pads
- DC resistance measured separately

## AC Parasitic Capacitance and Conductance of Neighboring I/O1 – I/O2

f (Hz) \ T (°C)	T <sub>R</sub>	T (°C)										
		100	150	200	250	300	350	400	450	500	550	
120	1.0	0.7	0.6	0.4	0.3	0.5	0.4	0.6	0.7	1.4	1.4	
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.001	<0.001	
1K	0.4	0.2	0.5	0.5	0.3	0.4	0.5	0.5	0.5	0.5	0.4	
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	
10K	0.5	0.4	0.5	0.5	0.4	0.4	0.4	0.5	0.5	0.4	0.4	
	<0.001	0.0013	<0.001	<0.001	<0.001	<0.001	<0.001	0.003	<0.003	<0.003	<0.003	
100K	0.5	0.3	0.5	0.4	0.3	0.4	0.4	0.5	0.5	0.4	0.4	
	0.01	0.016	0.014	0.016	0.016	0.011	0.014	0.029	0.035	0.026	0.045	
1M	0.5	0.4	0.5	0.4	0.3	0.4	0.4	0.5	0.5	0.4	0.5	
	<0.010	<0.010	0.013	0.012	0.011	0.006	0.009	0.018	0.021	0.022	0.026	

> 50°C margin above 500°C

pF  
μS

$C < 1.5 \text{ pF}$ ,  $R > 20 \text{ M}\Omega$

Usable for many envisioned 500°C SiC ICs



## AC Parasitic Capacitance and Conductance of Neighboring I/O2 – I/O3

f (Hz) \ T (°C)	T <sub>R</sub>	100	150	200	250	300	350	400	450	500	550
120	0.7	0.6	0.5	0.4	0.3	0.4	0.4	0.6	0.5	0.6	0.6
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
1K	0.3	0.3	0.4	0.4	0.2	0.4	0.3	0.5	0.3	0.5	0.5
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.0013	0.001	<0.001
10K	0.4	0.3	0.4	0.4	0.3	0.3	0.4	0.4	0.4	0.4	0.3
	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001
100K	0.3	0.3	0.4	0.4	0.2	0.3	0.3	0.4	0.4	0.4	0.3
	0.005	0.005	<0.005	<0.005	<0.005	0.005	0.013	<0.010	0.014	0.012	<0.010
1M	0.3	0.4	0.4	0.4	0.2	0.3	0.3	0.4	0.4	0.4	0.3
	<0.010	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020	<0.020

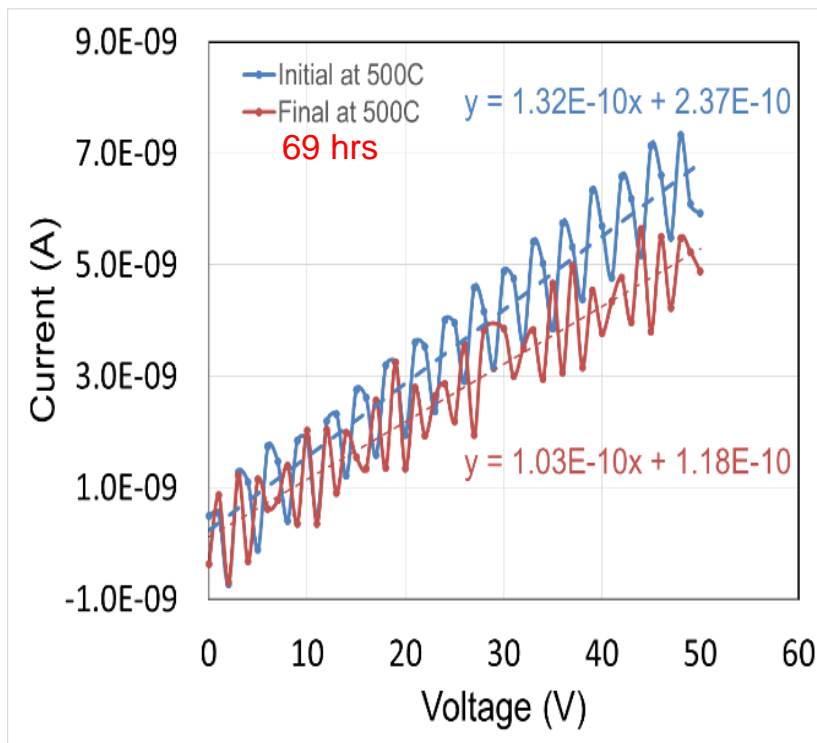
> 50°C margin above 500°C

pF  
μS

$C < 1.5 \text{ pF}$ ,  $R > 20 \text{ M}\Omega$

Usable for packaging many envisioned 500°C SiC ICs

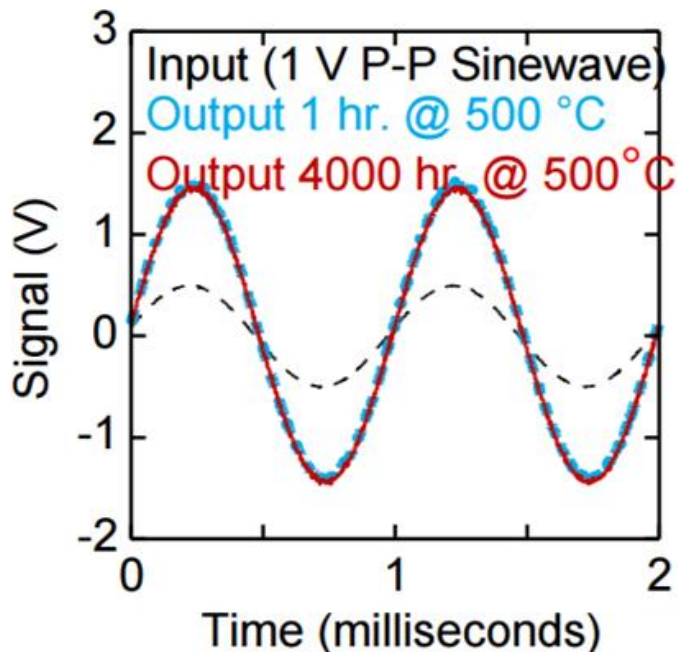
## DC Resistance of Neighboring I/Os



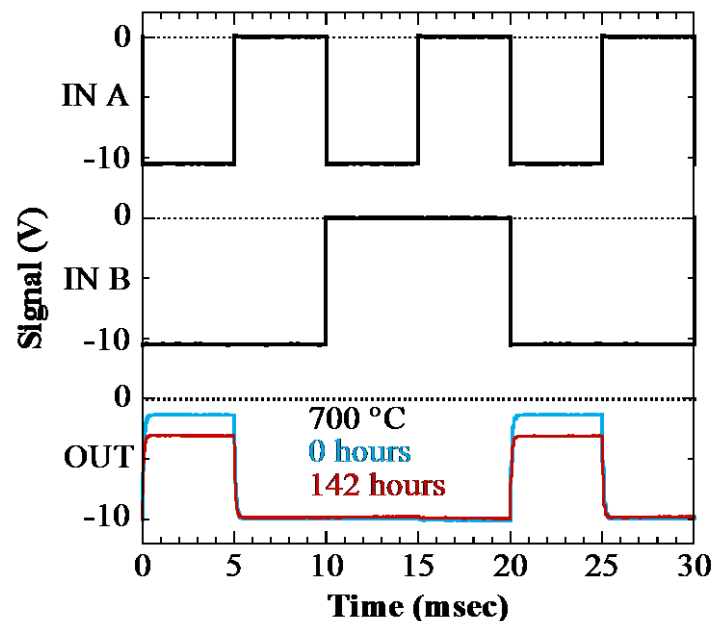
### DC I - V Curves

- I-V curve between I/O27 and I/O28
- 500°C
- Wide DC bias range: 0 - 50V
- SMU: integration time 16.67 msec, time delay 0.1 sec
- I/O28 not connected to SiC die, I/O27 connected to isolated two-terminal test structure on SiC die
- Package mounted on PCB
- Slope of linear fits: 7.6 GΩ initially 9.7 GΩ after 69.4 hrs
- DC resistance slightly underestimate
- Noise from running oven

## Extensive test with SiC high temperature ICs – Recent progress



Input (dark) and output (blue) waveforms of OPAMP in closed loop with SiC epi-resistors of ratio of 8 to 1 in 500 °C air ambient after 4000 hours (5.6 months)



NOR logic gate test waveforms measured at the start and 142 hours into 700 °C electrical testing.

# Test of HTCC system with SiC high temperature ICs in GEER

## - Recent progress

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### Simulated Venus atmosphere conditions

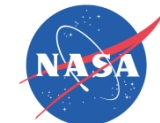
- Implemented in the NASA Glenn Extreme Environments Rig (GEER)
- GEER consists of 800 liter 304 stainless steel pressure vessel
- AC-phase controlled electric heaters
- Gases delivered by custom gas mixing system consisting of seven mass flow controllers
- Each constituent filled to achieve the molar mixing ratios of the simulated Venus surface atmospheric composition
- Simulated gas composition based on widely accepted data reported in Ref.
- The vessel heated at a rate of 7 °C/hour
- 460 °C and pressure ranging from 9.33MPa to 9.45Mpa

Ref.: Kliore A., Moroz V.I., and Keating G.M (1986) *The Venus International Reference Atmosphere*. Pergamon, Oxford.

# Test of HTCC system with SiC high temperature ICs in GEER

## - Recent progress

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### Simulated Venus Atmosphere Gas Mixture

Gas	Mixing (Mole) Ratio
CO <sub>2</sub>	0.965
N <sub>2</sub>	0.035
SO <sub>2</sub>	18.0 x 10 <sup>-5</sup>
OCS	5.10 x 10 <sup>-5</sup>
H <sub>2</sub> O	3.00 x 10 <sup>-5</sup>
CO	1.20 x 10 <sup>-5</sup>
H <sub>2</sub> S	0.20 x 10 <sup>-5</sup>
HCl	5.00 x 10 <sup>-7</sup>
HF	2.50 x 10 <sup>-9</sup>

## Test of HTCC system with SiC high temperature ICs in GEER - Recent progress

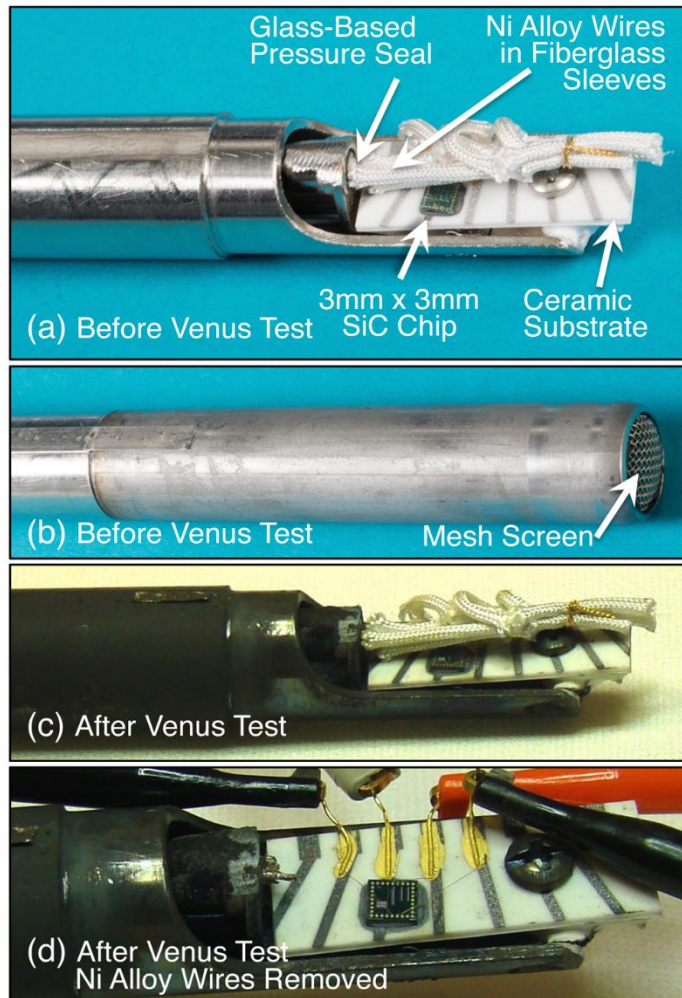
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### Test of Packaging Material System in GEER

- Facilitate electrical test of SiC ICs
- Performance of packaging materials
  - Substrate materials
    - Aluminum oxides (and nitride) chemical stability in hot acidic and S contained environment
      - Bulk and surface
  - Substrate metallization
    - Precious metallization still noble in hot high pressure acidic and S environment?
  - Au alloy wire-bond
    - Is Au still noble in hot high pressure acidic environment?
    - Surface effects of impurities
    - Effects of supercritical CO<sub>2</sub> flow
  - Die-attach
    - Stability of metal oxides in hot high pressure acidic environment
  - If hermetic seal or encapsulation is required / feasible?

# Test of HTCC system with SiC high temperature ICs in GEER

## - Recent progress

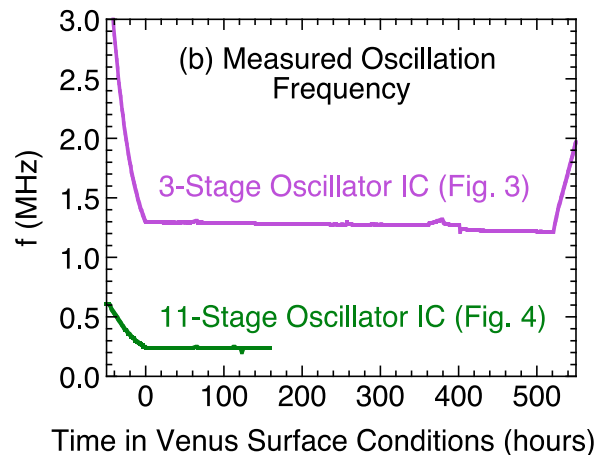
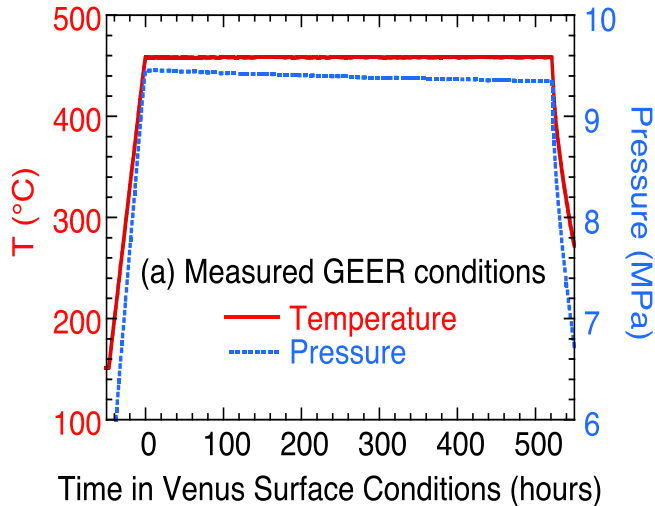


## Packaging and Connections

- HTCC 92% alumina substrate
- Pt metallization traces
- Glass and Pt particles die-attach
- 254  $\mu\text{m}$  (10 mil) diameter Au wires bonded to Pt traces using oven-cured gold particles
- 24  $\mu\text{m}$  (1 mil) diameter gold alloy wires thermo-sonically bonded connecting SiC chip to substrate
- Substrate mounted on the feed-through using alumina-based high temperature adhesive and small stainless steel screw
- 4-Nickel 201 conductors mineral insulated in Inconel 600 jacket through Swagelok
- Fiberglass sleeves for separation / insulation

# Test of HTCC system with SiC high temperature ICs in GEER

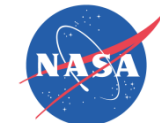
## - Recent progress



### Packaged SiC ring oscillator IC test data

- Recorded GEER vessel temperature and pressure
- Measured SiC ring oscillator IC output signal frequencies
- 3-stage SiC JFET ring oscillator IC functioned at 1.26 MHz over the entire 521 hours (21.7 days)
- 11-stage ring oscillator IC (bottom trace, green) functioned at 245 kHz for 109 hours
  - Functional following post-test disconnection from its feed-through
  - Short-circuited during Venus conditions testing
- No electrical or mechanical failure of Pt/HTCC material system observed





## Summary

Pt/HTCC alumina packaging material system for SiC high temperature electronics

- ◆ Extensively tested with various SiC analogue and digital integrated circuits at 500 °C for thousands of hours
- ◆ Successfully tested together with SiC ICs at 700°C for over one hundred forty hours
- ◆ Successfully tested together with two SiC ring-oscillator ICs in simulated Venus environment for over 500 hours for the first time\*
  - 460°C, 90 Bar, corrosive
  - Both Au wire-bond and die-attach tested
  - No failure observed
- ◆ Study of packaging materials in GEER continues

\* P.G. Neudeck, R.D. Meredith, L. Chen, D.J. Spry, L.M. Nakley, and G.W. Hunter, AIP Advances, Vol. 6, Issue 12, 2016.



# Thank You Very Much for Your Attention!

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