National Aeronautics and Space Administration

Micron MT29F128G08AJAAA 128GB Asynchronous Flash Memory Total Ionizing Dose Characterization Test Report

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1. Purpose

The purpose of this test was to characterize the Micron MT29F128G08AJAAA's parameter degradation for total dose response and to evaluate and compare lot date codes for sensitivity. In the test, the device was exposed to both low dose and high dose rate (HDR) irradiations using gamma radiation. Device parameters such as leakage currents, quantity of upset bits and overall chip and die health were investigated to determine which lot is more robust.

2. Test Samples

Five (5) parts from each lot of MT29F128G08AJAAA were provided to Code 561 for total ionizing dose (TID) testing. All specifications and descriptions are according to Revision J 8/16 (PDF# 09005aef83e0bed4). More information can be found in Table 1.

Table 1: Part Identification Information

Qty	Part Number	LDC	REAG#	Package
5	MT29F128G08AJAAAWP-ITZ	201504	16-017	TSOP-48
5	MT29F128G08AJAAAWP-ITZ	201504BYGGFZR.21	16-018	TSOP-48

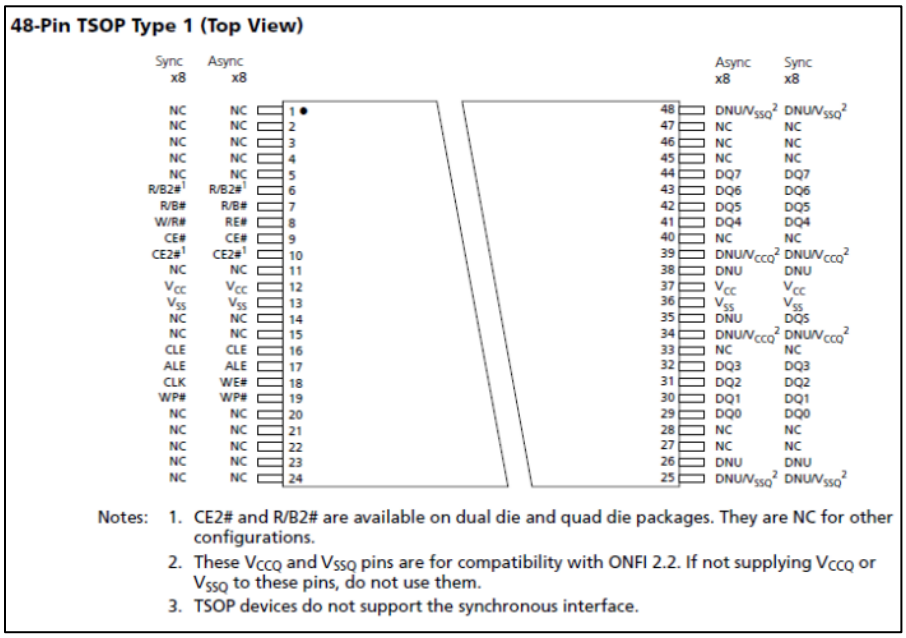

Figure 1: Pin out for flash component

3. General

Radiation testing was performed by exposing the parts to gamma radiation at a dose rate determinant on the possible test duration. Ten parts were irradiated on a single test coupon. Prior to the first radiation dose, all ten parts were electrically tested. After each exposure level, the parts were tested again and returned to radiation within the time limits (within 2 hours) defined by MIL-STD-883, Method 1019. All parts were biased during the irradiation steps described in Table 2. Electrical and functional characterization was performed daily starting at approximately 8:00am. The parts were re-subjected to irradiation at approximately 4:00pm after testing was completed.

Table 2: Device Grouping and Step-Stress Instructions

Test Levels (krad(Si))	Notes
0	During pre-radiation testing, a single DUT from 16-017 exhibited an electrical failure where in it could not be programmed. This was replaced by another device from this LDC.
1	Device #5 (16-017) exhibited minor integrity issues with chip select #2
5	- Same as above -
10	Device #4 (16-017) exhibited minor integrity issues with chip select #1 + same note as 1krad(Si)
15	- Same as above -
20	Device #4 (16-017) exhibited chip select instability after >75% of AC tests + same note as 15krad(Si)
30	Device #1 & #3 (16-017) exhibited minor integrity issues with both chip select #1 & #2 during checkboard programming
40	Chip select failures were noted on both lots: 16-017: #1 (both), #3 (1st), #4 (both), #5 (both) – total of 7/10 16-018: #2 (1st), #5 (1st) – total of 2/10

4. Electrical Tests

Electrical tests were performed using a Triad Spectrum flash memory tester. DC electrical specification thresholds were set in accordance with the MT29F128G08AJAAA datasheet. Additionally, a sequential set of programmed patterns were utilized to assess the functionality of the flash devices. These are shown within the AC Test Order section of Table 3.

All test conditions listed for the following parameters are tested:

Table 3: List of Electrical Tests Performed

	Test Step	Thresholds
DC Test	**read id**	
	Leakage Current	**40uA**
	Icc read	**200mA**
	Icc write	**200mA**
	Icc erase	**200mA**
	Icc standby	**20mA (idle)**
AC Test Order	**read Checkerboard PHY 0s**	
	program 0s	
	read 0s	
	erase	
	read 1s	
	program 1s	
	read 1s	
	erase	
	read 1s	
	program Checkerboard PHY 1s	
	read Checkerboard PHY 1s	
	erase	
	read 1s	
	program Checkerboard PHY 0s	
	read Checkerboard PHY 0s	

5. Failure Criteria

The parameter limits are defined as those listed in the MT29F128G08AJAAA datasheet. DC parameters thresholds were not exceeded during any of the irradiation steps. If functional failure was observed for any of the AC Test steps, those results were noted and compared relative to the dosing step, the individual device's previous dose step measurements and within the group of LDC for that device.

6. Source Requirements

The total dose source is in a room air source gamma ray facility, which is compliant with MIL-STD-883, Method 1019. Dosimetry is NIST traceable.

7. Bias Conditions and Fixtures

The biased parts were fixtured using TSOP-48 sockets on a copper wiring board. The biased part configuration was consistent with the standby mode in the following table.

Table 4: Bias Conditions

Mode	CE#	CLE	ALE	WE#	RE#	DQS	DQx	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/V_{CCQ}[2]	2
Bus idle	L	X	X	H	H	X	X	X	
Command input	L	H	L	↑	H	X	input	H	
Address input	L	L	H	↑	H	X	input	H	
Data input	L	L	L	↑	H	X	input	H	
Data output	L	L	L	H	↓	X	output	X	
Write protect	X	X	X	X	X	X	X	L	

Notes:
1. DQS is tri-stated when the asynchronous interface is active.
2. WP# should be biased to CMOS LOW or HIGH for standby.
3. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

8. Procedure and Setup

General test procedures were in accordance with MIL-STD-883, Method 1019, Condition D. Parts were serialized randomly. ESD procedures were followed during test and transfer of the devices between irradiation chamber and characterization. Exposures were performed at ambient laboratory temperature. Approximate cumulative test levels were provided by the values in Table 2.

All data from the evaluation of the parameters in Table 3 were logged in excel spreadsheet files (in .xlsx format) using result logs from the Triad tester. Data for all parts were measured and logged.

9. Results

The device performance between LDCs was similar until 20krad(si). Device #4 from 16-017 exhibited an inability to be programmed during the latter steps of the AC tests. Further, this device and #5 (same LDC) exhibited high levels of block errors at 30krad(si). After 40krad(si), three (3) device from lot 16-017 and two (2) devices from lot 16-018 had at least one chip select failure each which were not recoverable after power cycling or erasing the devices.

Regardless of whether the failure of device #3 from 16-017 prior to the test is included in these results, LDC 201504BYGGFZR.21 (16-018) devices performed better than LDC 201504 (16-017) in this set of tests.

10. References

[1] M73A_32Gb_64Gb_128Gb_256Gb_AsyncSync_NAND.pdf Rev. J 8/16 EN
Micron 32Gb, 64Gb, 128Gb, 256Gb Asynchronous/Synchronous NAND