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Inclusion of Body-Bias Effect in SPICE Modeling of 4H-SiC Integrated Circuit Resistors

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Abstract. The direct-current (DC) electrical behavior of n-type 4H-SiC resistors used for realizing 500 °C durable integrated circuits (ICs) is studied as a function of substrate bias and temperature. Improved fidelity electrical simulation is described using the SPICE NMOS model to simulate resistor substrate body-bias effect which is absent from the SPICE semiconductor resistor model.

1. Background

Increasingly capable extreme-temperature-durable 4H-SiC JFET ICs are being demonstrated.

Fig. 1: 3mm-by-3mm SiC JFET ring oscillator chip that *operated for 3 weeks exposed to 460 °C 9.4 MPa caustic Venus surface atmospheric conditions [1].*

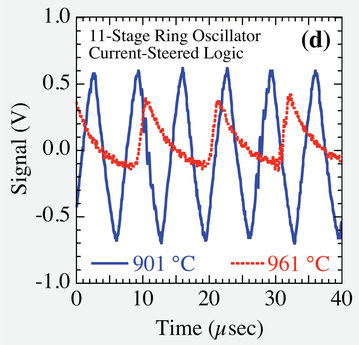


Fig. 2: SiC JFET ring oscillator waveforms *at record high temperature > 900 °C [2].*

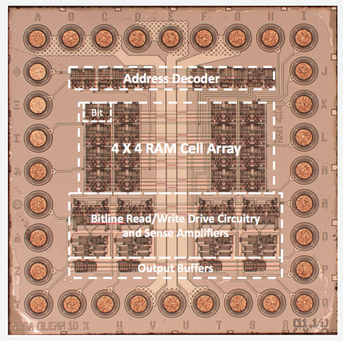
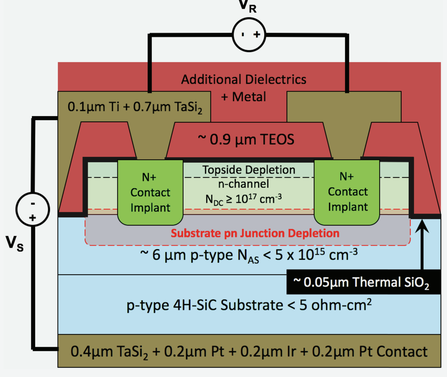


Fig. 3: 3mm-by-3mm SiC RAM chip (195 JFETs) *operational for 5000+ hours at 500 °C* [FR.D1.4 by D. Spry, Friday 9:30 AM].

Circuit engineers need SPICE models to design application-specific 4H-SiC JFET ICs.

2. Body-Bias Effect

As shown below in Fig. 4, the cross-sectional illustration of the SiC resistor structure used to realize the above JFET IC's, **bias-dependent substrate pn junction depletion** affects undepleted thickness (and therefore conductivity) of the resistor n-channel.



- Experimental SiC fabrication, packaging, and measurement setup are described in [2–5].
- For applied resistor bias $V_R > 0$, depletion widths change across the lateral length of the resistor.
- Current vs. voltage (I-V) characteristics and the IC resistor resistance value *depend on both V_R and V_S.*

Fig. 4: Cross-sectional illustration of SiC resistor structure used in JFET IC's, including substrate pn junction depletion that gives rise to resistor body bias effect and applied substrate bias voltage V_s and resistor bias voltage V_R.

3. Measured Impact of Body Bias Effect on Resistor I-V Characteristics

- Body-bias effect causes mild non-linearity (i.e., downward bending) of resistor I-V characteristics (shown in green).
- Amount of non-linearity can be quantified by plotting differential resistance $R_{Diff} = dI/dV$ (shown in blue).

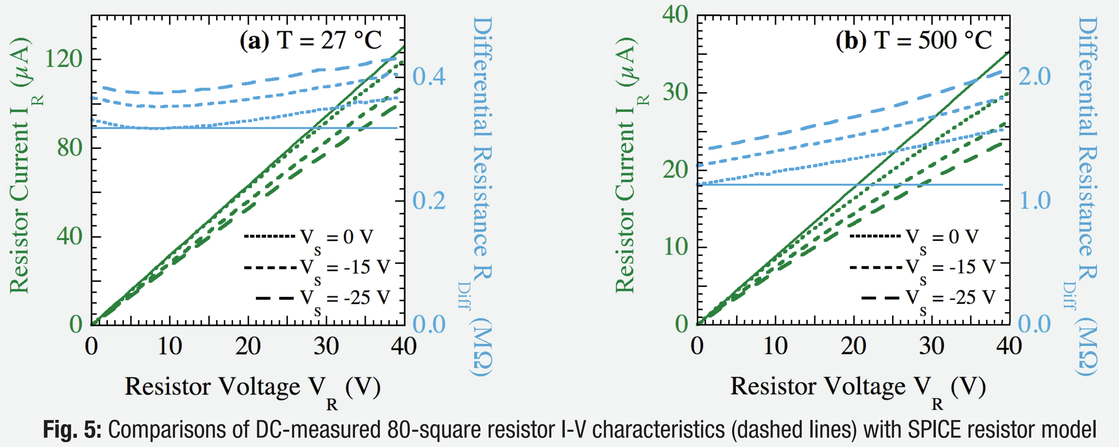


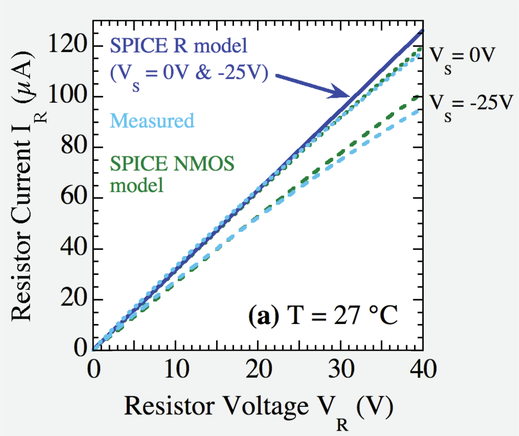
Fig. 5: Comparisons of DC-measured 80-square resistor I-V characteristics (dashed lines) with SPICE resistor model simulations (solid lines) at V_S of 0, -15, and -25 V at (a) 27 °C and (b) 500 °C.

- ***Baseline SPICE resistor model (solid lines) [6] does not account for substrate body-bias effect, so it is incapable of modeling experimentally observed JFET IC resistors (and I-V characteristics) with high degree of accuracy.***
  - ***Fails to model observed I-V bending/nonlinearity with increasing resistor bias V_R.***
  - ***Fails to model observed dependence on substrate bias V_S.***
- Slightly rectifying metal contacts at 27 °C impacts R_{diff} for $V_R < 15$ V.

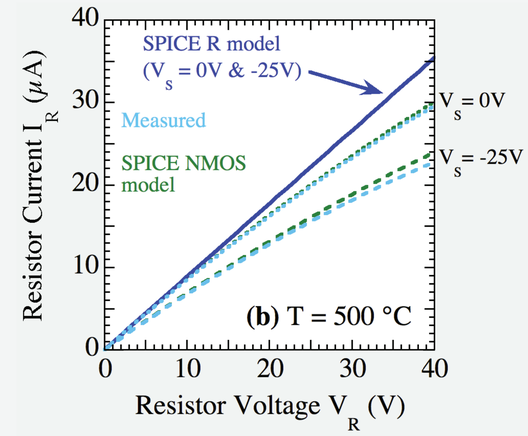
4. Resistor SPICE Model With Body Effect

While Fig. 4 depicts a SiC IC resistor cross section, this resistor structure can also be considered a long-channel JFET with the electrically biased p-epilayer/substrate serving as the gate terminal.

- The resistor can therefore be modeled using the SPICE NMOS LEVEL=1 model [6].
- The magnitude of negative substrate voltage V_S required to completely deplete the n-channel is large since NAS << NDC (Fig. 4), so the JFET operates in the linear region as a substrate-bias controlled resistor.
- The SPICE NMOS LEVEL=1 parameters for modeling IC resistors as N-MOSFETs with body bias effect (such as in green text SPICE listings shown below) can be extracted from Fig. 5 I-V data using the low drain-bias NMOS parameter extraction procedure described in [7].




```
*NASA Glenn SiC IC Resistor I-V Simulation 27C
V1 1 0
V2 2 0
MSICRES 1 2 0 2 sicresfet L=4.8E-4 W=6.0E-6
.MODEL sicresfet NMOS LEVEL=1 VTO=-155 KP=1.773E-6
CJ=6.856E-5 PB=2.87 RSH=0.0 PHI=1.435 GAMMA=0.0 JS=0.0
.DC v1 0 40.0 1.0 v2 0 -25.0 -25.0
.PRINT v(1) mag(i(v1))
.END
```




```
*NASA Glenn SiC IC Resistor I-V Simulation 500C
V1 1 0
V2 2 0
MSICRES 1 2 0 2 sicresfet L=4.8E-4 W=6.0E-6
.MODEL sicresfet NMOS LEVEL=1 VTO=-128 KP=5.474E-7
CJ=8.822E-5 PB=1.99 RSH=0.0 PHI=0.998 GAMMA=0.0 JS=0.0
.DC v1 0 40.0 1.0 v2 0 -25.0 -25.0
.PRINT v(1) mag(i(v1))
.END
```

Fig. 6: I-V comparison of linear R SPICE resistor model (solid dark blue) and NMOS SPICE body-effect resistor model (dashed green) with measured data (dashed light blue) for a 480-by-6μm resistor at (a) 27°C and (b) 500 °C. The SPICE decks for the NMOS model simulations are shown in green text below each plot.

Substantially improved agreement with measured I-V is obtained using the NMOS SPICE model I-V compared with the SPICE R model I-V.

5. Conclusion

For improved accuracy circuit design and modeling of 4H-SiC JFET ICs using SPICE, the NMOS resistor modeling approach described in this report should supercede/replace the standard SPICE R resistor model reported in [6], which ignores the body-bias effect.

6. Future Work

Comparison and design studies of SiC JFET integrated circuits using new SPICE NMOS resistor modeling.

7. Acknowledgements

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8. References

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