Analyzing System on A Chip Single Event Upset Responses using Single Event Upset Data, Classical Reliability Models, and Space Environment Data

Melanie Berg[1], Kenneth LaBel[2], Michael Campola[2], Michael Xapsos[2]

Melanie.D.Berg@NASA.gov

1.AS&D in support of NASA/GSFC

2. NASA/GSFC

To be presented by Melanie Berg at the RADECS 2017 Radiation Effects on Components and Systems (RADECS) Conference, Geneva, Switzerland, October 6, 2017.

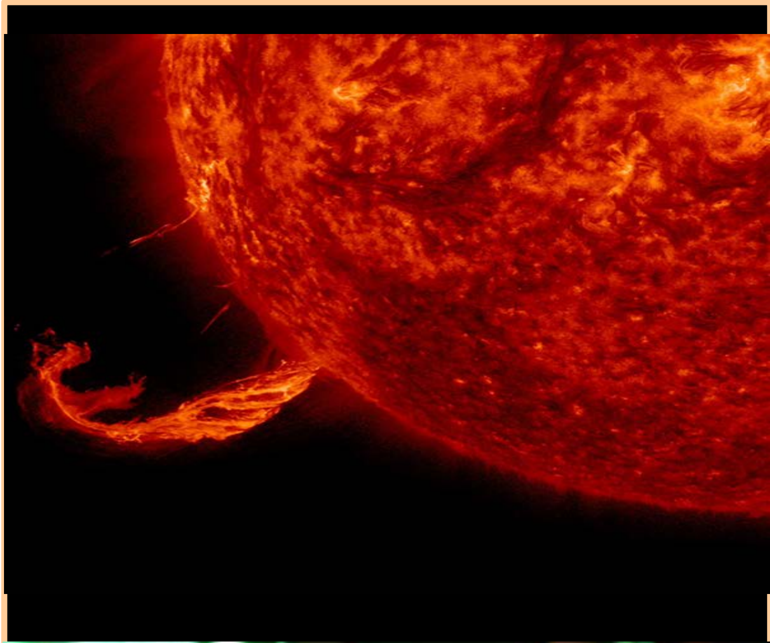
Acronyms

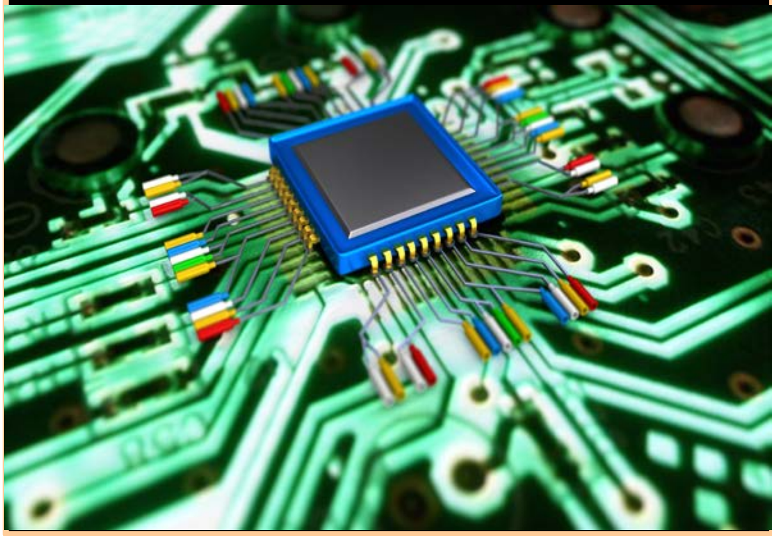
- Combinatorial logic (CL)
- Commercial off the shelf (COTS)
- Complementary metal-oxide semiconductor (CMOS)
- Device under test (DUT)
- Edge-triggered flip-flops (DFFs)
- Electronic design automation (EDA)
- Error rate (λ)
- Error rate per bit(λ_{bit})
- Error rate per system(λ_{system})
- Field programmable gate array (FPGA)
- Global triple modular redundancy (GTMR)
- Hardware description language (HDL)
- Input – output (I/O)
- Intellectual Property (IP)
- Linear energy transfer (LET)
- Mean fluence to failure (MFTF)
- Mean time to failure (MTTF)
- Number of used bits (#Usedbits)
- Operational frequency (fs)
- Personal Computer (PC)
- Probability of configuration upsets ($P_{configuration}$)
- Probability of Functional Logic upsets ($P_{functionalLogic}$)
- Probability of single event functional interrupt (P_{SEFI})
- Probability of system failure (P_{system})
- Processor (PC)
- Radiation Effects and Analysis Group (REAG)
- Reliability over time (R(t))
- Reliability over fluence (R(Φ))
- Single event effect (SEE)
- Single event functional interrupt (SEFI)
- Single event latch-up (SEL)
- Single event transient (SET)
- Single event upset (SEU)
- Single event upset cross-section (σ_{SEU})
- System on a chip (SoC)
- Windowed Shift Register (WSR)
- Xilinx Virtex 5 field programmable gate array (V5)
- Xilinx Virtex 5 field programmable gate array radiation hardened (V5QV)

Problem Statement

- **Conventional methods of applying single event upset (SEU) data to complex systems need improvement.**

- **The problem boils down to extrapolation and application of SEU data to characterize system performance in radiation environments.**



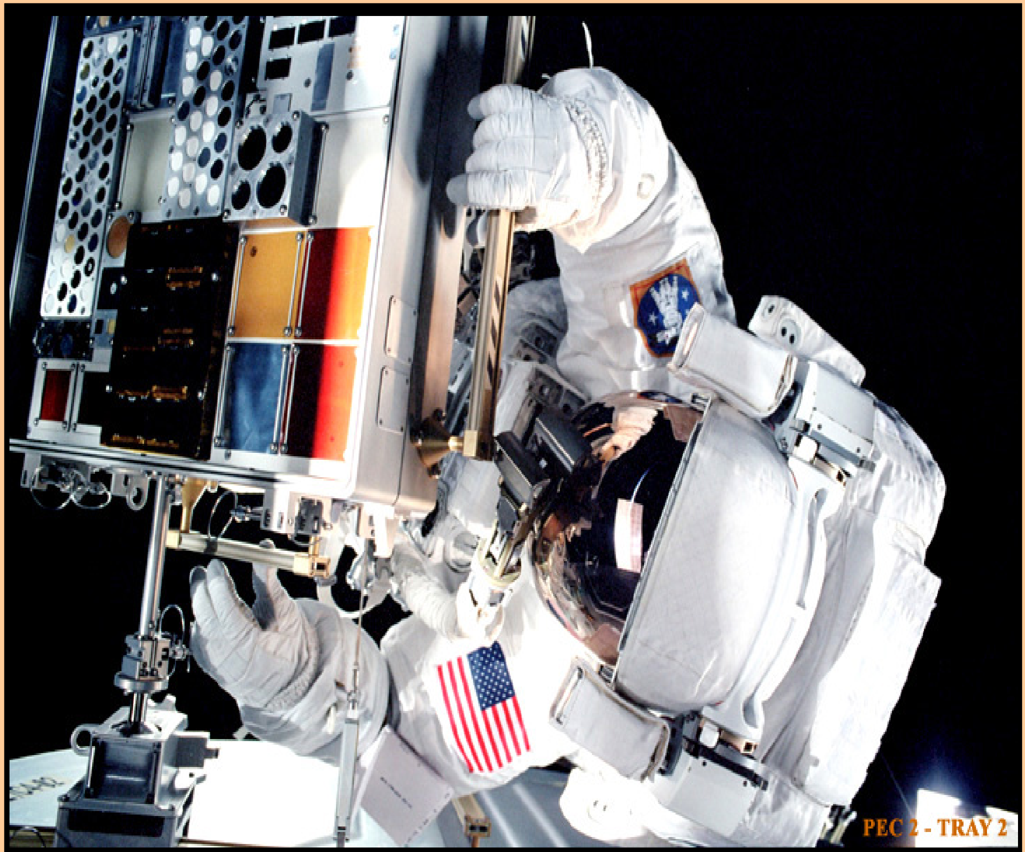


Abstract – Impact to Community

- **We are investigating the application of classical reliability performance metrics combined with standard SEU analysis data.**
- **We expect to relate SEU behavior to system performance requirements…**
  - **Our proposed methodology will provide better prediction of SEU responses in harsh radiation environments with confidence metrics.**

SEU System Analysis Is Not Simple Algebra

- **When a system is targeted for space, single event effect (SEE) data are obtained for all devices that make up that system.**
- **Combining component data is not simple addition.**
- **Co-dependent susceptibilities exist and must be handled accordingly.**



Proposed method should target critical missions subjected to ionizing particles.

Scope of Presentation

- **Full system analysis requires combining SEU data for a variety of devices across a variety of boxes/mediums.**
- **The scope of this presentation is for System-type SEU data analysis for a single device.**
- **In this presentation, a System on a Chip (SoC) field programmable gate array (FPGA) device is used as an example.**
- **Future work will expand to address full systems.**

This presentation is a simplified approach for SEU data extrapolation to complex systems. Future work will incorporate details for a more realistic analysis.

Background (1)
FPGA SEU Susceptibility

SEU Cross Section (σ_{SEU})

- σ_{SEU}s (per category) are calculated from SEU test and analysis.
- σ_{SEU}s are calculated with particles that vary in linear energy transfer (LET).
- FPGA architectures vary and so do their SEU responses.
- Most believe the dominant σ_{SEU}s are per bit (configuration or flip-flops (DFFs)). However, global routes are significant (more than DFFs).

σ_{SEU}s are measured by bit

σ_{SEU}s are measured by bit???

$$P(fs)_{system} \propto P_{Configuration} + P(fs)_{functionalLogic} + P_{SEFI}$$

Design σ_{SEU} | *Configuration σ_{SEU}* | *Functional logic σ_{SEU}* | *SEFI σ_{SEU}*

Sequential and Combinatorial logic (CL) in data path

Global Routes and Hidden Logic

For a system, should σ_{SEU}s be measured by bit????

Background (2)

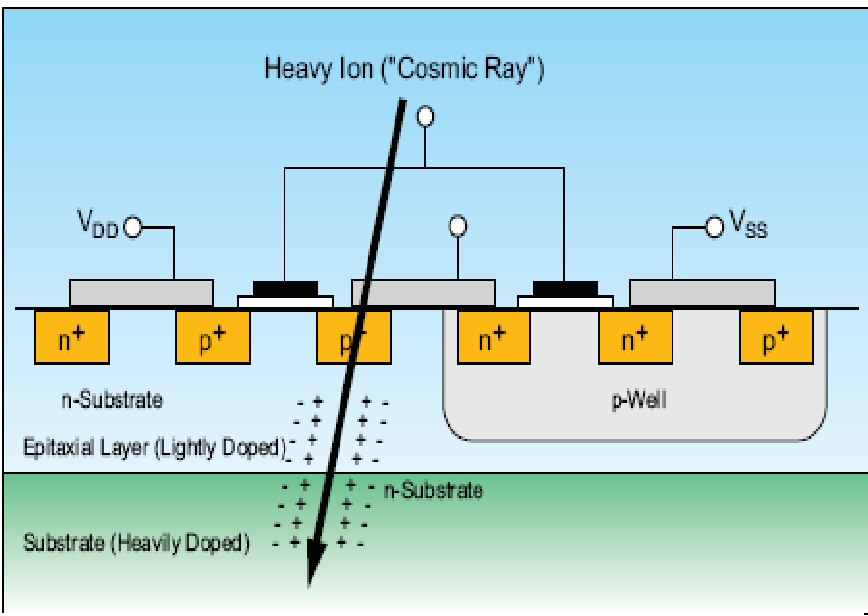
Conventional Conversion of SEU Cross-Sections To Error Rates for Complex Systems First Step

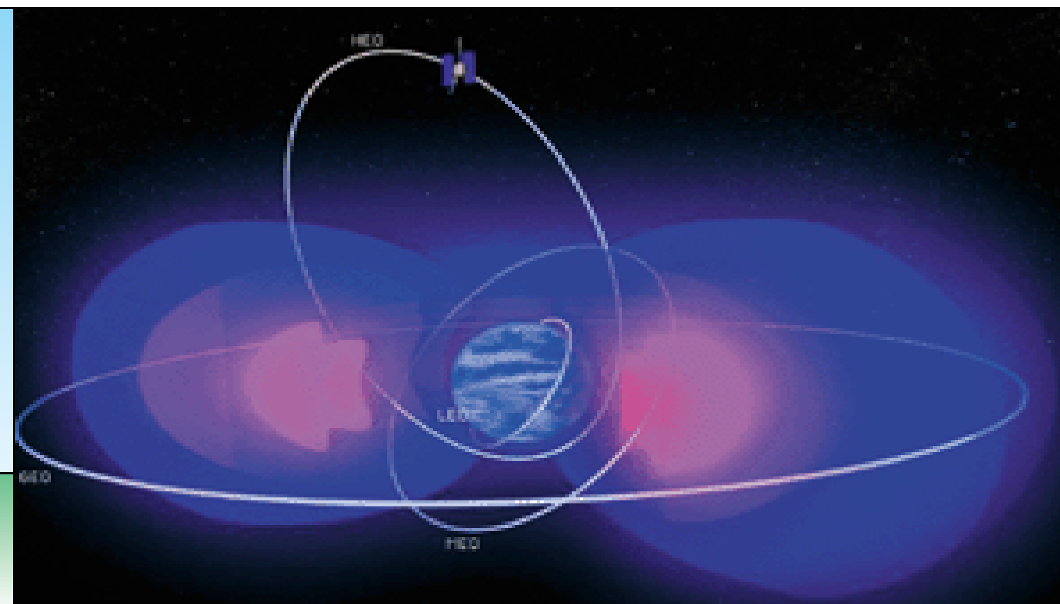
σ_{SEU} = *#errors/fluence*

λ_{system} = *#errors/time*

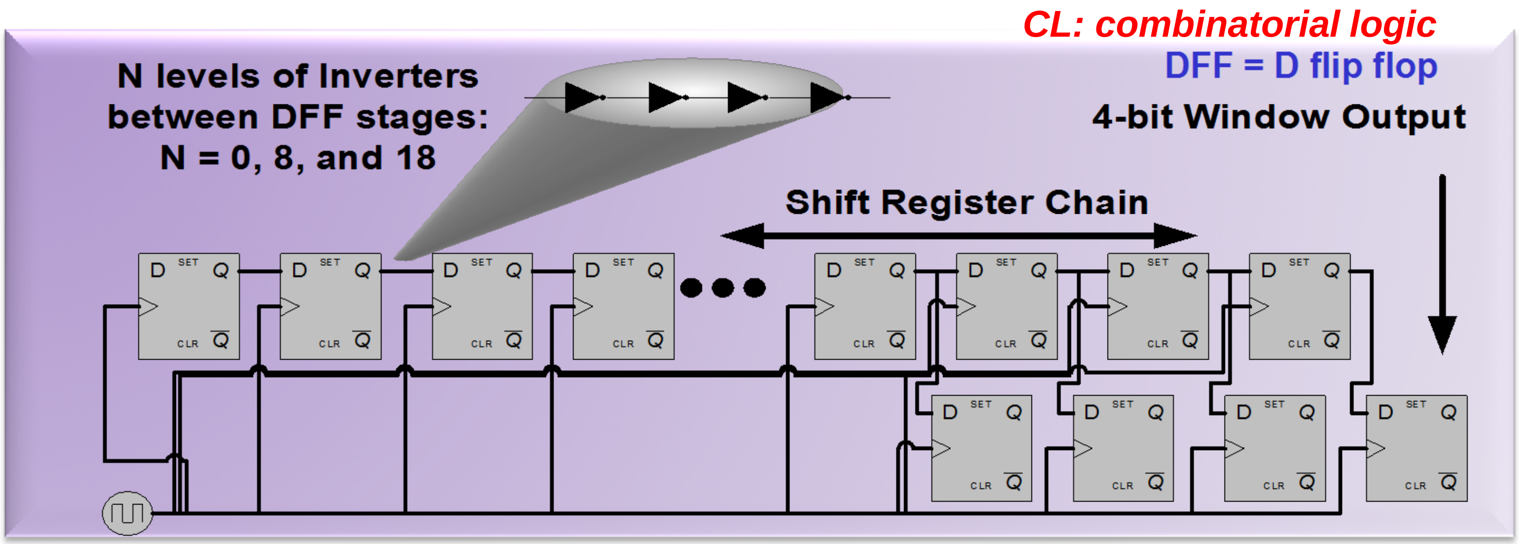
LET: Linear energy transfer

- **Perform SEU accelerated radiation testing across ions with different linear energy transfers (LETs) to calculate σ_{SEU}s per LET.**





Windowed Shift Register (WSR) Test Structures Are Used To Obtain SEU Data



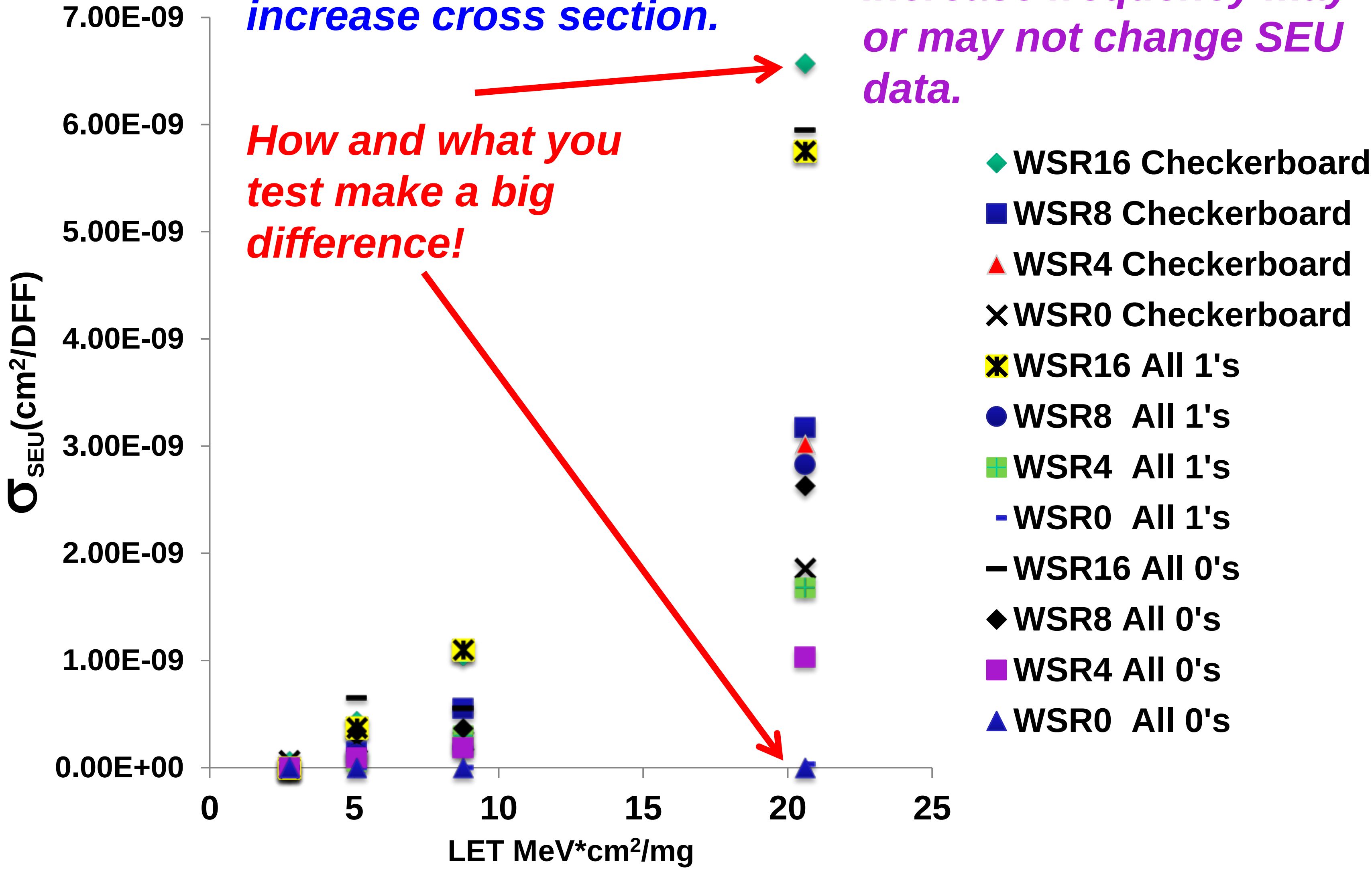
- Shift registers are typical test structures (mapped into device under test (DUT)) used for accelerated radiation testing.
- Purpose is to analyze DFF and CL susceptibility.

Windowed Shift Register (WSR) Microsemi – RTG4 Heavy Ion Data at 100MHz

Add combinatorial logic, increase cross section.

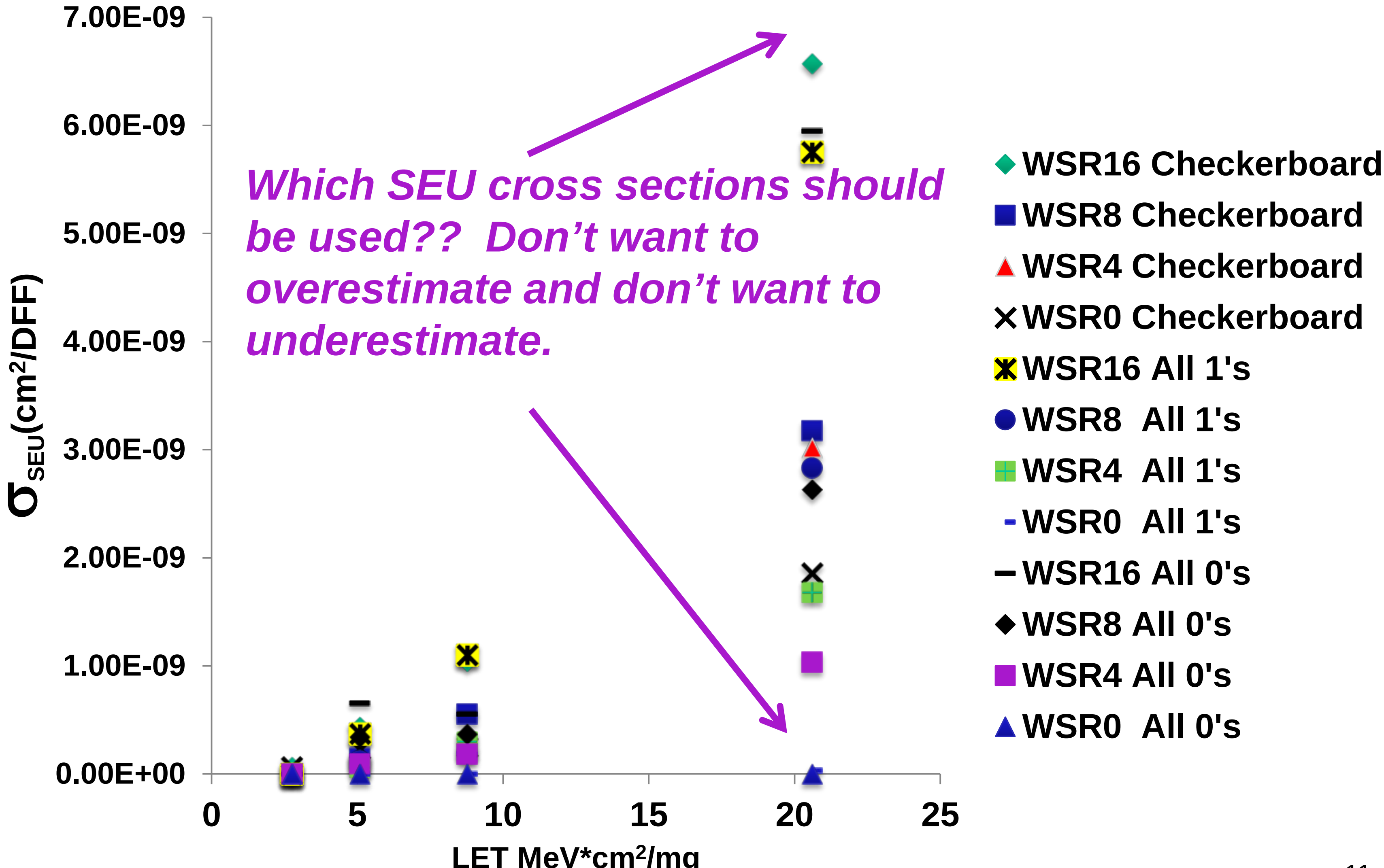
Increase frequency may or may not change SEU data.

How and what you test make a big difference!



What If Tests Do Not Investigate Test Structures Across A Variety of Parameters

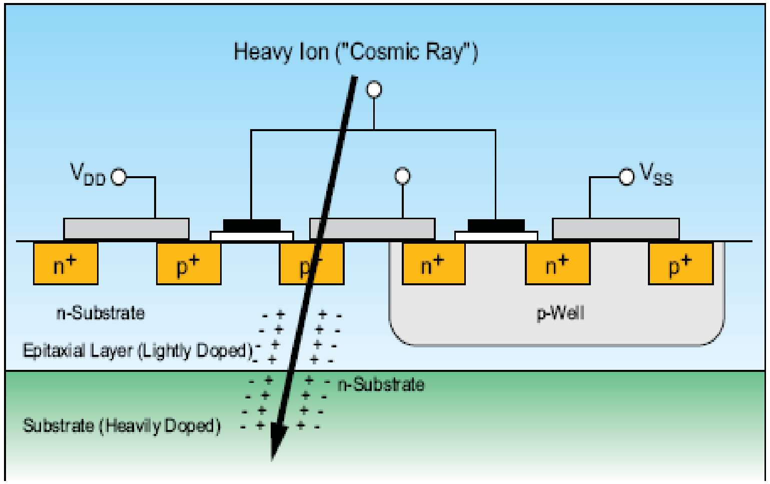
Data might not reflect potential SEU responses!

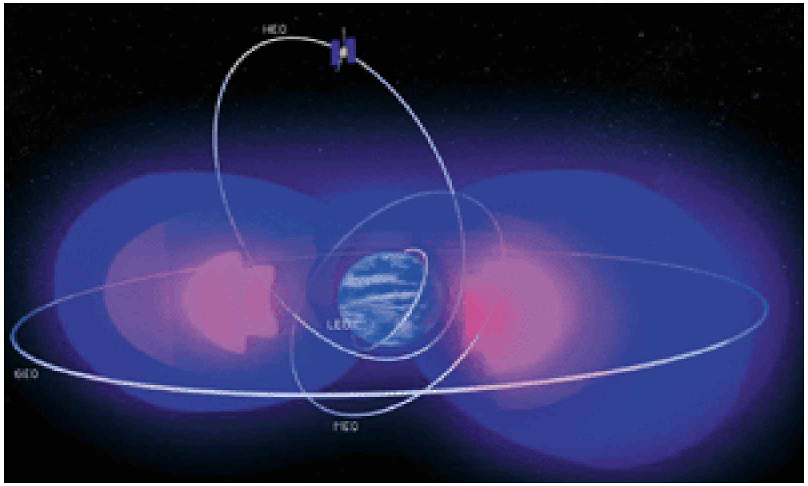


Background (3)

Conventional Conversion of SEU Cross-Sections To Error Rates for Complex Systems Next Step

- **Bottom-Up approach (transistor level):**
  - Given σ_{SEU} (per bit) use an error rate calculator (such as CRÈME96) to obtain an error rate per bit (λ_{bit}).
  - Multiply λ_{bit} by the number of used memory bits (#*UsedBits*) in the target design to attain a system error rate (λ_{system}). Configuration and DFFs.
- **Top-Down approach (system level):**
  - Given σ_{SEU} (per system) use an error rate calculator (such as CRÈME96) to obtain an error rate per bit (λ_{system}).



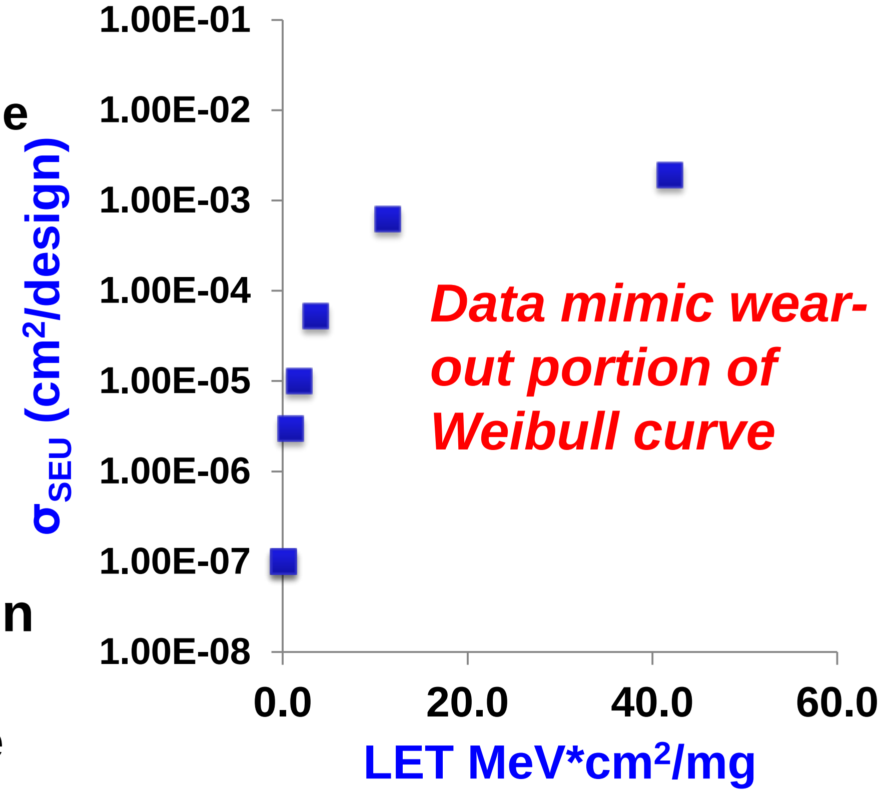


Understand Goal of SEU Testing and Data Application

- Is the goal of SEU testing to analyze test circuits?
  - Efficacy of DFF mitigation.
  - Single event transient (SET) propagation strength.
  - SET width.
  - General test circuit evaluation.
- Or… is the goal of testing to obtain data for eventual system characterization?
- System characterization requires more than conventional test circuit analysis.
  - Test circuits are too simple.
  - Test circuits often do not follow formal design rules (e.g., synchronous, CMOS balancing, or place and route).
  - Design topology affects SEU response.
- Complex system test structures are important for SEU system characterization.
  - Top down approach.
  - Multiple complex test structures and trend evaluation is essential.

Technical Problems with Current Methods of Error Rate Calculation

- For submission to CRÈME96, σ_{SEU} data (in Log-linear form) are fitted to a Weibull curve.
  - The two main parameters for curve fitting are a shape factor and a slope factor.
  - During the curve fitting process, a large amount of error can be introduced.
  - Consequently, it is possible for resultant error rates (for the same design) to vary by decades.
- Because of the error rate calculation process, σ_{SEU} data are blended together and it is nearly impossible to hone in on the problem spots. This can become important for mitigation insertion.



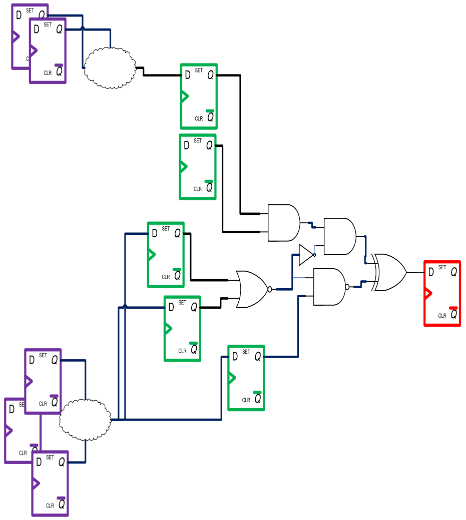
Technical Problems with Bottom-Up Analysis Method (1)

- **Multiplying each bit within a design by λ_{bit} is not an efficient method of system error rate prediction.**
  - **Works well with memory structures… but…complex systems do not operate or respond like memories.**
  - **If an SEU affects a bit, and the bit is either inactive, disabled, or masked, a system malfunction might not occur.**
    - **Using the same multiplication factor across DFFs will produce extreme over-estimates.**
    - **To this date, there is no accurate method to predict system state activity for complex systems.**
    - **Fault injection or simulation will not determine frequency of activity. Any electronic design automation (EDA) tool supplier will agree.**

$$\lambda_{system} < \lambda_{bit} \times \#UsedBits$$

Technical Problems with Bottom-Up Analysis Method (2)

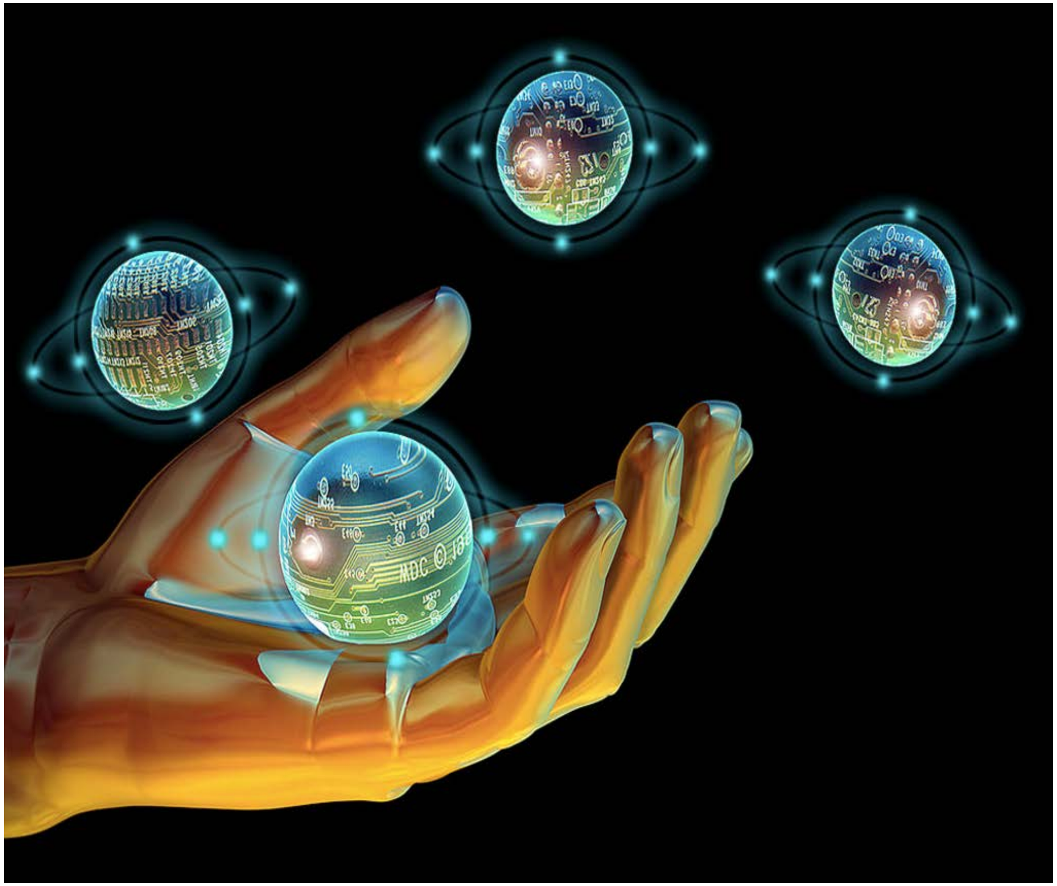
- **There are a variety of components that are susceptible to SEUs (clocks, resets, combinatorial logic, flip-flops (DFFs, etc…)).**
  - **Various component susceptibilities are not accurately characterized at a per bit level.**
  - **Design topology makes a significant difference in susceptibility and is not characterized in error rate calculators (e.g., CREME96).**
  - **As a result, there's a lot of hand-waving during data extrapolation.**



Error rates calculated at the transistor-bit level are estimated at too small of granularity for proper extrapolation to complex systems.

Let's Not Reinvent The Wheel… A Proven Solution Can Be Found in Classical Reliability Analysis

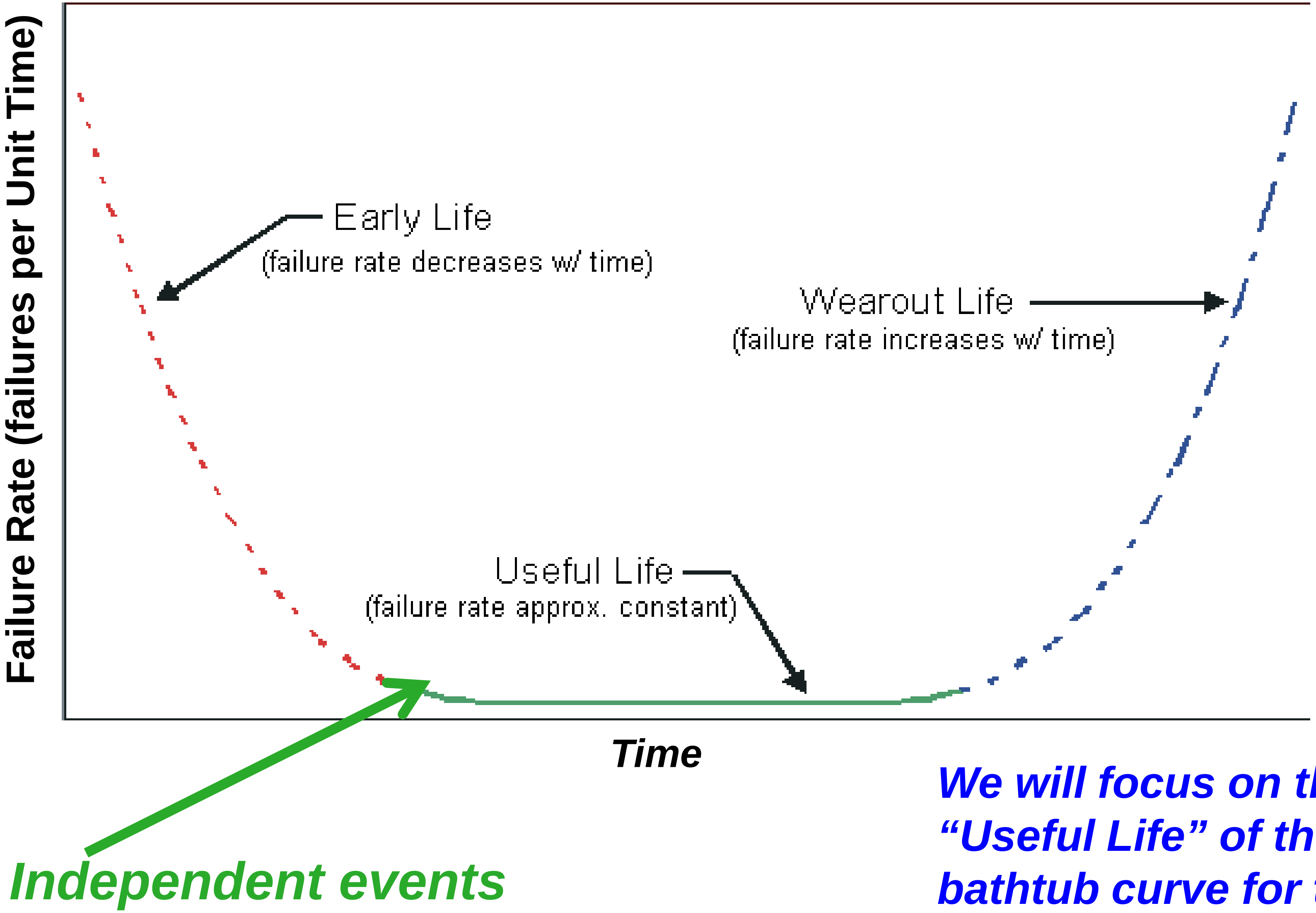
- **Classical reliability models have been used as a standard metric for complex system performance.**
- **The analysis provides a more in depth interpretation of system behavior over time by using system-level MTTF data for system performance metrics.**



$$R(t)=e^{-t/MTTF} \text{ or } R(t)=e^{-\lambda t}$$

Theory is already developed, proven, and should be in our hands!

Weibull Failure Rate ($\lambda(T)$) Bathtub Curve



We will focus on the "Useful Life" of the bathtub curve for this analysis.

Mapping Classical Reliability Models from The Time Domain To The Fluence Domain

- The exponential model that relates reliability to MTTF assumes that during useful-lifetime:
  - Failures are independent.
  - Error rate is constant.
  - MTTF = $1/\lambda$.

$R(t)=e^{-t/MTTF}$ or $R(t)=e^{-\lambda t}$

Weibull slope = 1… exponential.

Parallel between time and fluence.

- For a given LET (across fluence):
  - SEUs are independent.
  - σ_{SEU} is constant.
  - MFTF = $1/\sigma_{SEU}$.

σ_{SEU} = #errors/fluence

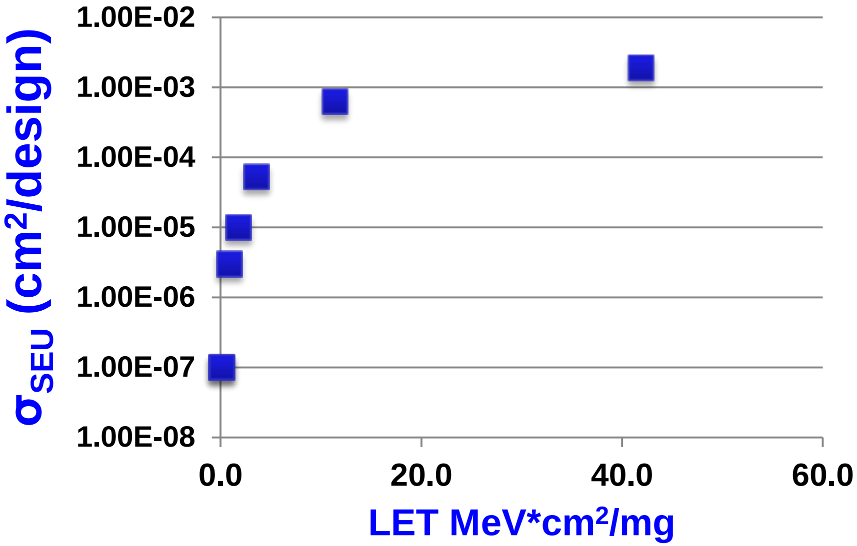
λ_{system} = #errors/time

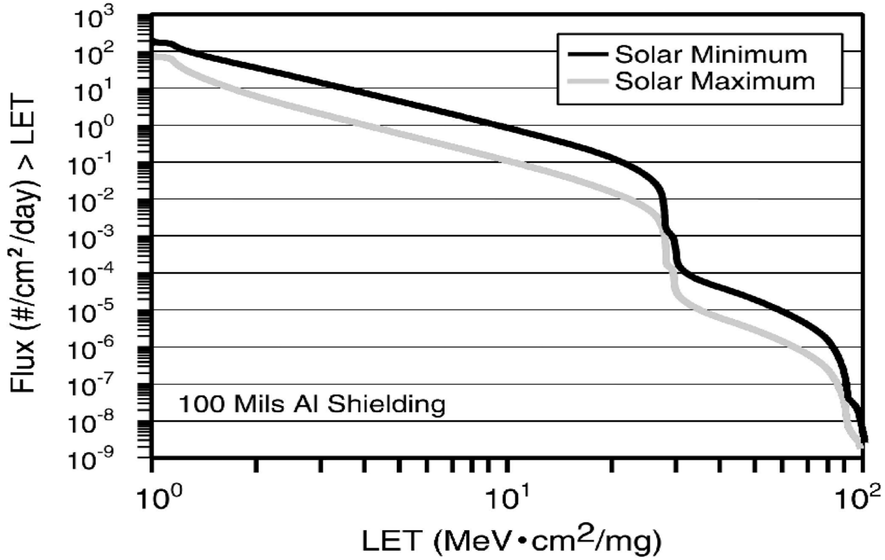
- Hence, mapping from the time domain to the fluence domain (per LET) is straight forward:
  - $t \Leftrightarrow \Phi$
  - MTTF $\Leftrightarrow$ MFTF
  - $\lambda \Leftrightarrow \sigma_{SEU}$

$$R(t)=e^{-t/MTTF} \Leftrightarrow R(\Phi)=e^{-\Phi/MFTF}$$

Creating Reliability Curves from σ_{SEU}s

- σ_{SEU} data are system level.
- A histogram of environment data is created. Bins are determined by LET values at each σ_{SEU} data point.
- For each data point at a given LET, a combination of binned environment data and upper-bound σ_{SEU} data are used to determine system reliability performance.
- A piecemeal approach is performed per data point to determine the weakest points of system performance.





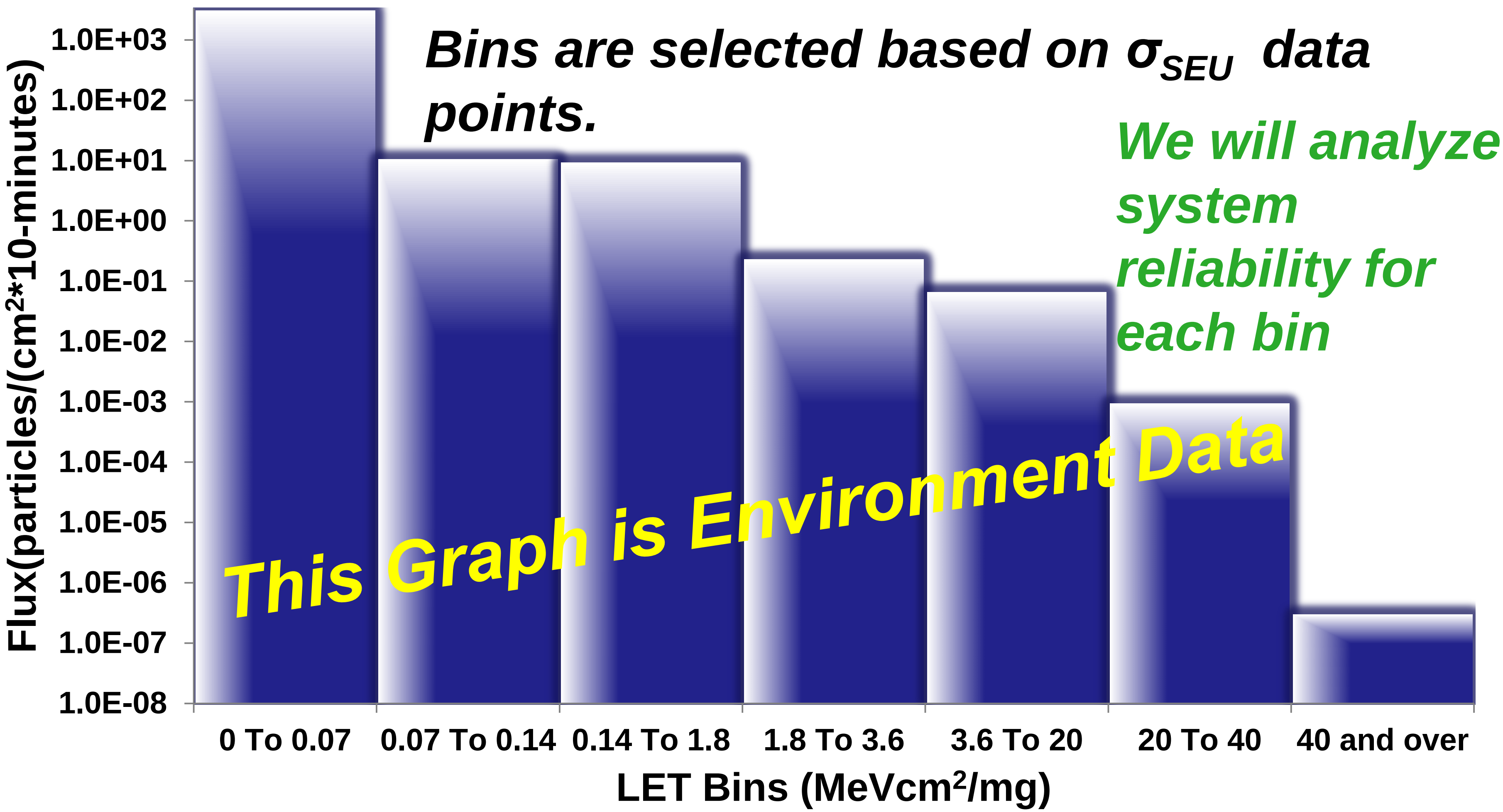
M. A. Xapsos, IEEE NSREC Short Course, Ponte Vedra Beach, FL, 2008.

Example of Proposed Methodology Application

- **Mission requirements:**
  - The FPGA shall contain an embedded microprocessor.
  - Selection shall be made between a Xilinx V5QV (very expensive device) or a Xilinx V5 with embedded PowerPC (relatively cheap device).
  - FPGA operation shall have reliability of 3-nines (99.9%) within a 10 minute window at Geosynchronous Equatorial Orbit (GEO).
- **Proposed methodology:**
  - Create a histogram of particle flux versus LET for a 10-minute window of time for your target environment.
  - Calculate MFTF per LET (obtain SEU data).
  - Graph R(Φ) for a variety of LET values and their associated MFTFs. $R(\Phi)=e^{-\Phi/MFTF}$
  - For selected ranges of LETs, use an upper bound of particle flux (number of particles/cm^2•10-minutes), to determine if the system will meet the mission's reliability requirements.

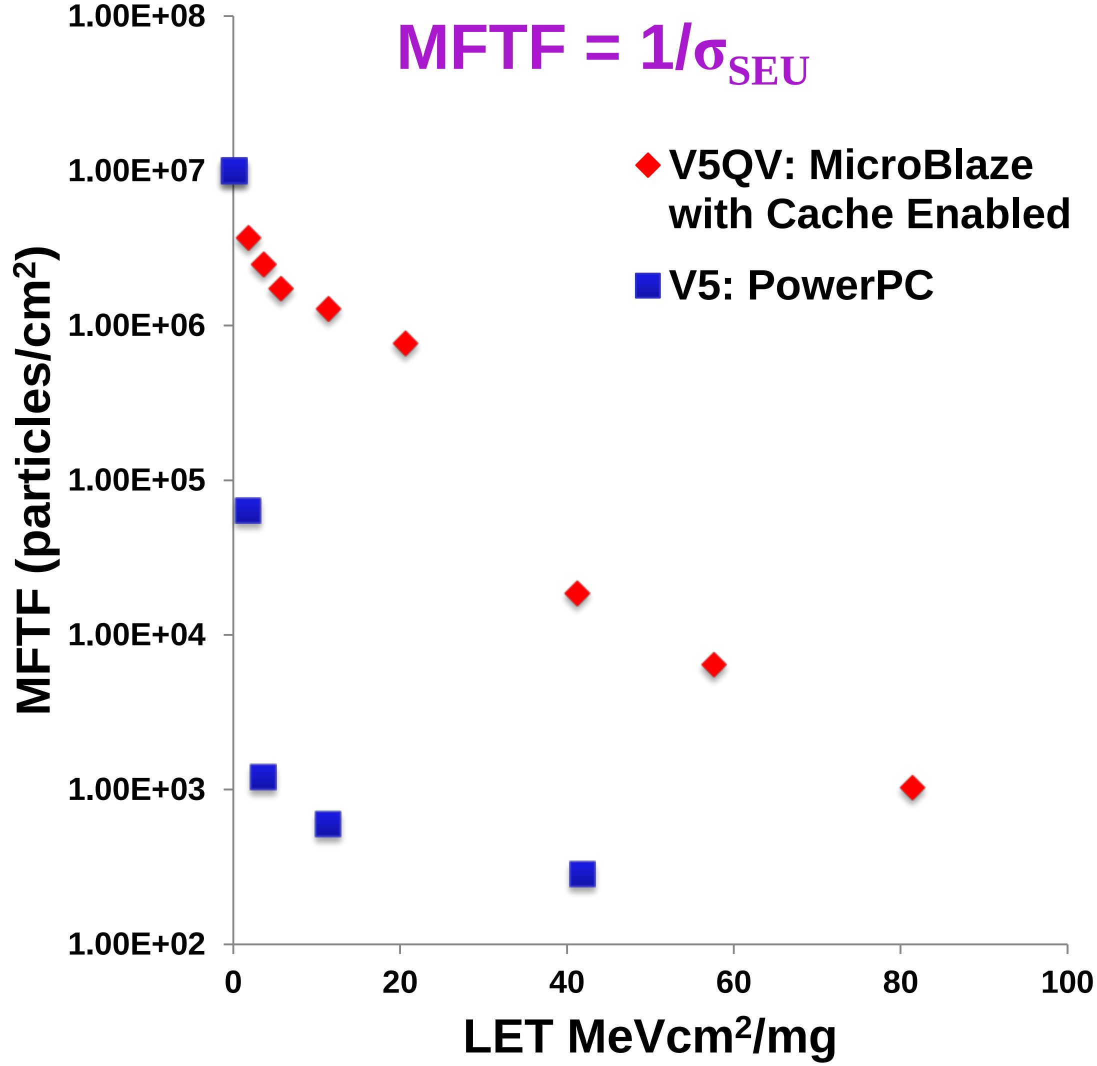
Environment Data: Flux versus LET Histogram for A 10-minute Window

Geosynchronous Equatorial Orbit (GEO) 100-mils shielding



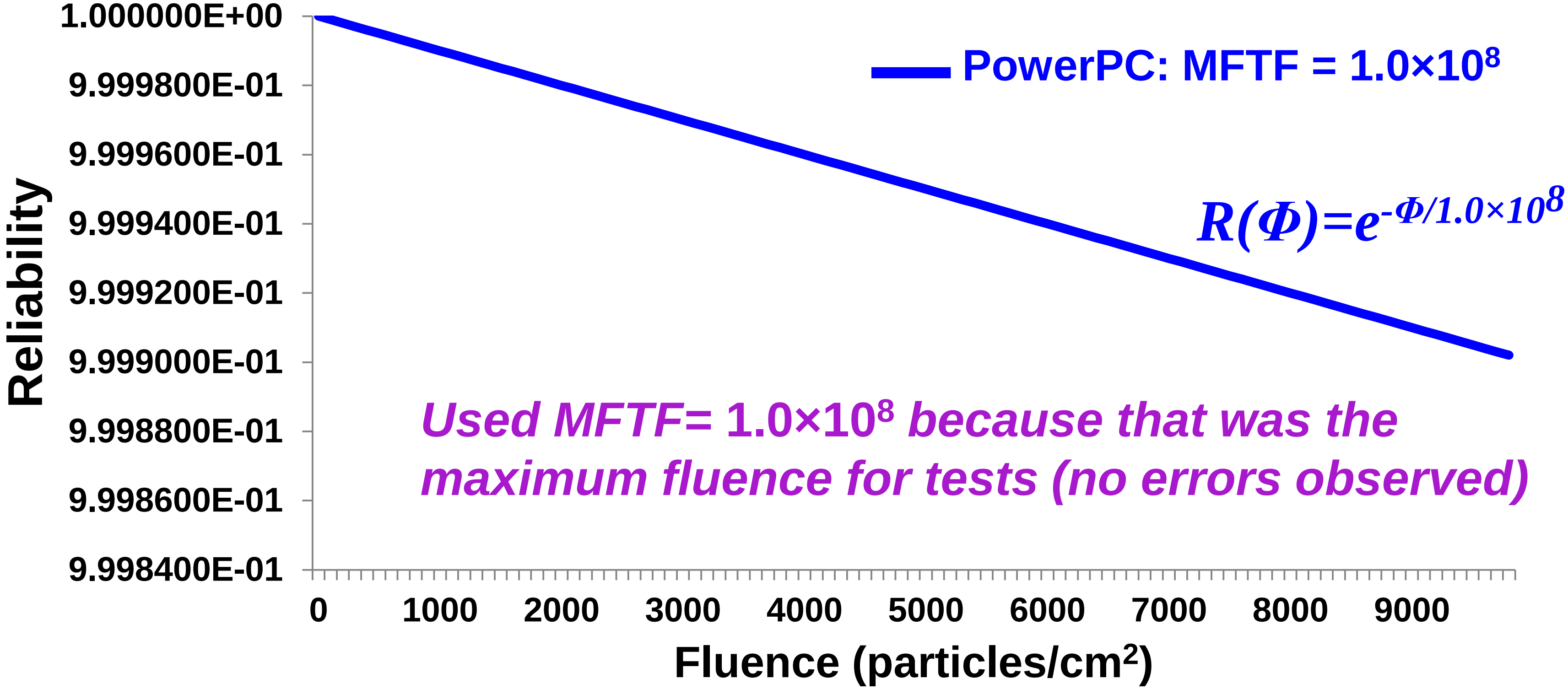
MFTF versus LET for the Xilinx V5 Embedded PowerPC Core and the Xilinx V5QV MicroBlaze Soft Processor Core

- **V5QV:** no system errors were observed below LET=1.8MeV•cm²/mg. Total fluence > 5.0×10^{8} particles/cm².
- **PowerPC:**
  - No system errors were observed below LET=0.07MeV•cm²/mg with total fluence = 1.0×10^{8} particles/cm².
  - Hence, at 0.07, we will assume an upper-bound MFTF = 1.0×10^{8} particles/cm².
  - More tests would increase the MFTF for this bin.



Reliability across Fluence up to LET=0.07MeV•cm²/mg

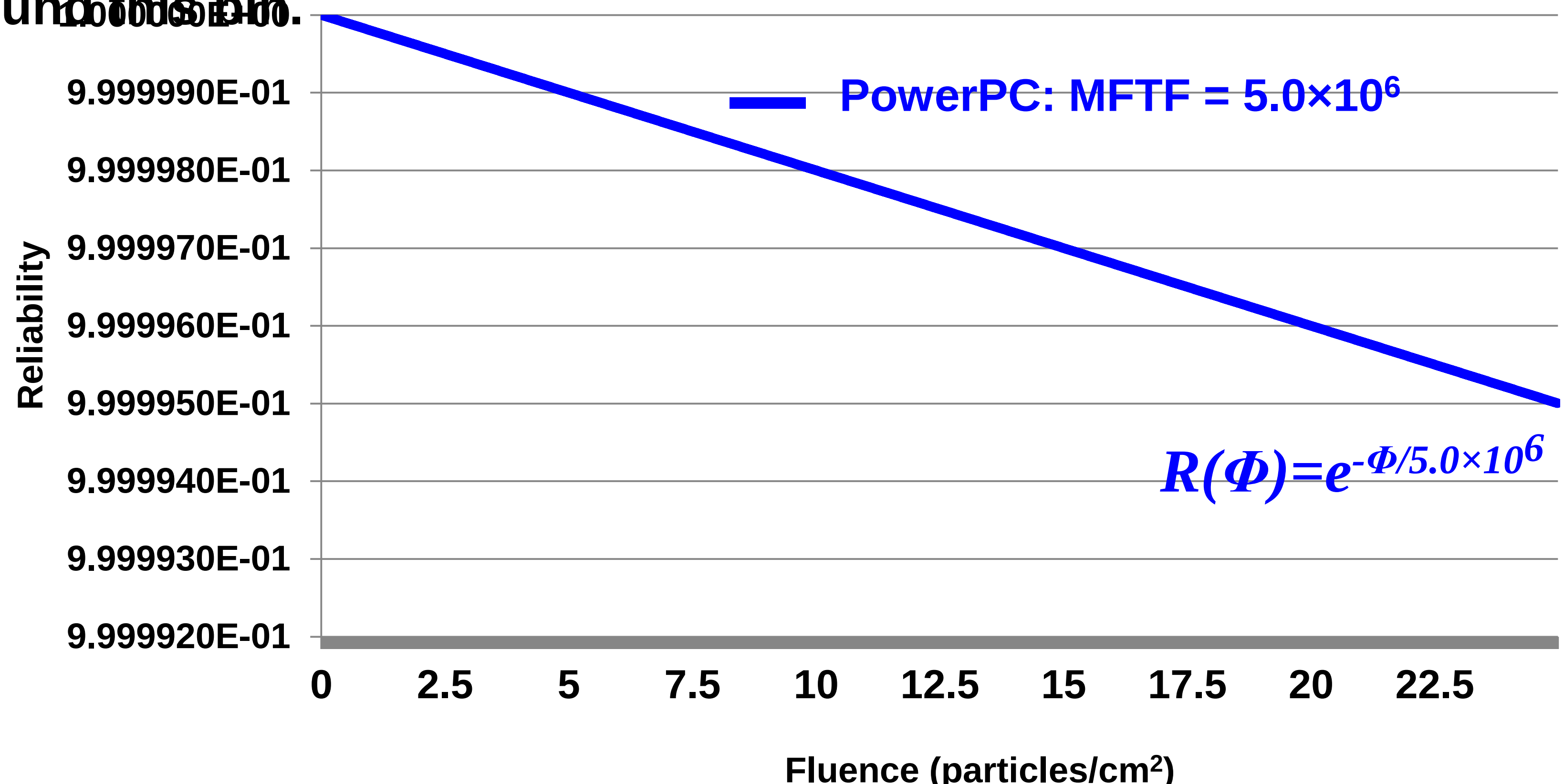
Binned GEO Environment data show approximately 3000 particles/(cm²•10-minutes), in the range of 0.0MeV•cm²/mg to 0.07MeV•cm²/mg. We are using MFTF for 0.07MeV•cm²/mg to upper bound this bin.



Reliability at 3000 particles/(cm²•10-minutes) > 99.99% for the PowerPC design implementation. "9's" could be increased with more tests.

Reliability across Fluence up to LET=0.14MeV•cm²/mg

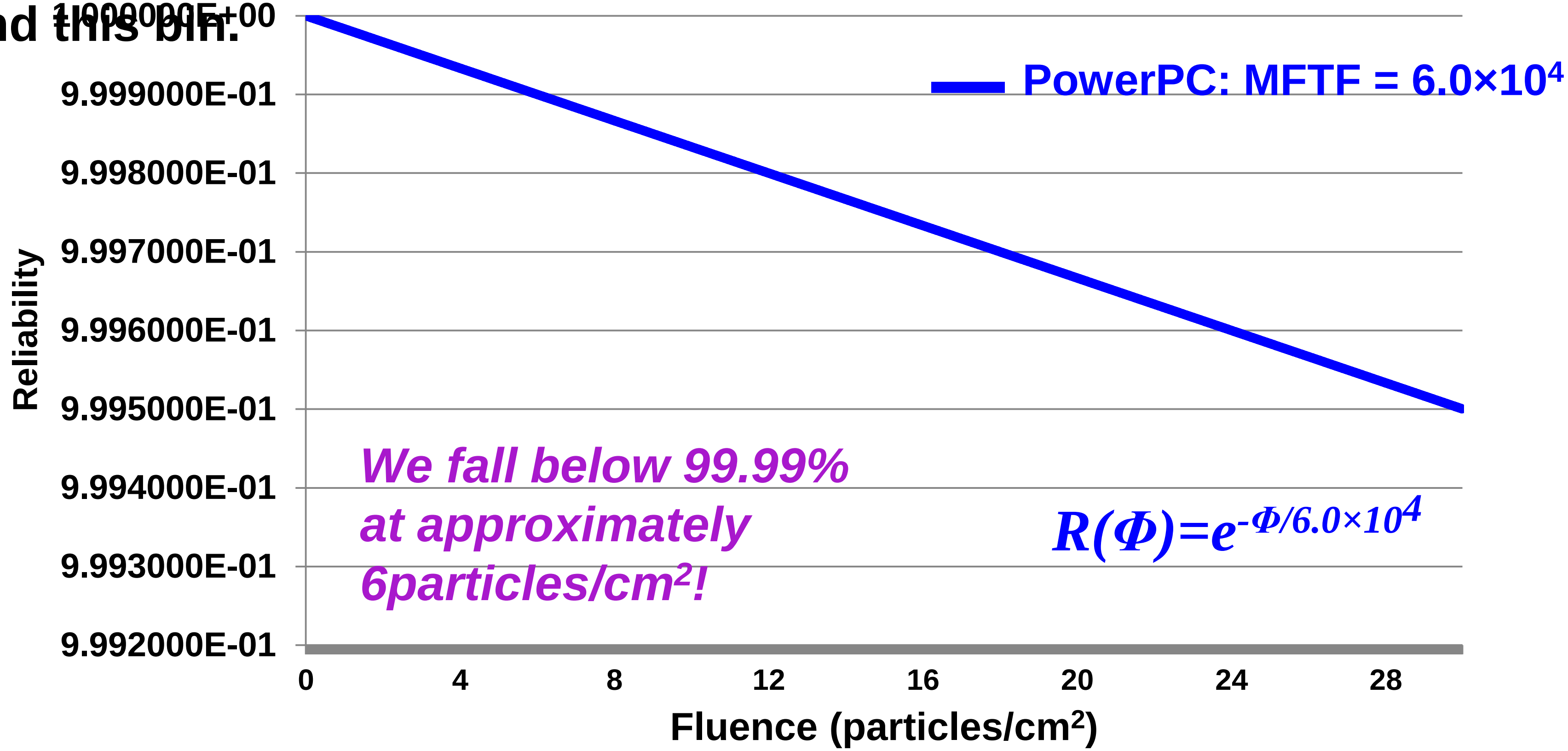
Binned GEO Environment data show approximately 11 particles/(cm²•10-minutes), in the range of 0.07MeV•cm²/mg to 0.14MeV•cm²/mg. We are using MFTF for 0.1MeV•cm²/mg to upper bound this bin.



Reliability at 5 particles/(cm²•10-minutes) > 99.999% for the V5QV PowerPC design implementation.

Reliability across Fluence up to LET=1.8 MeV•cm²/mg

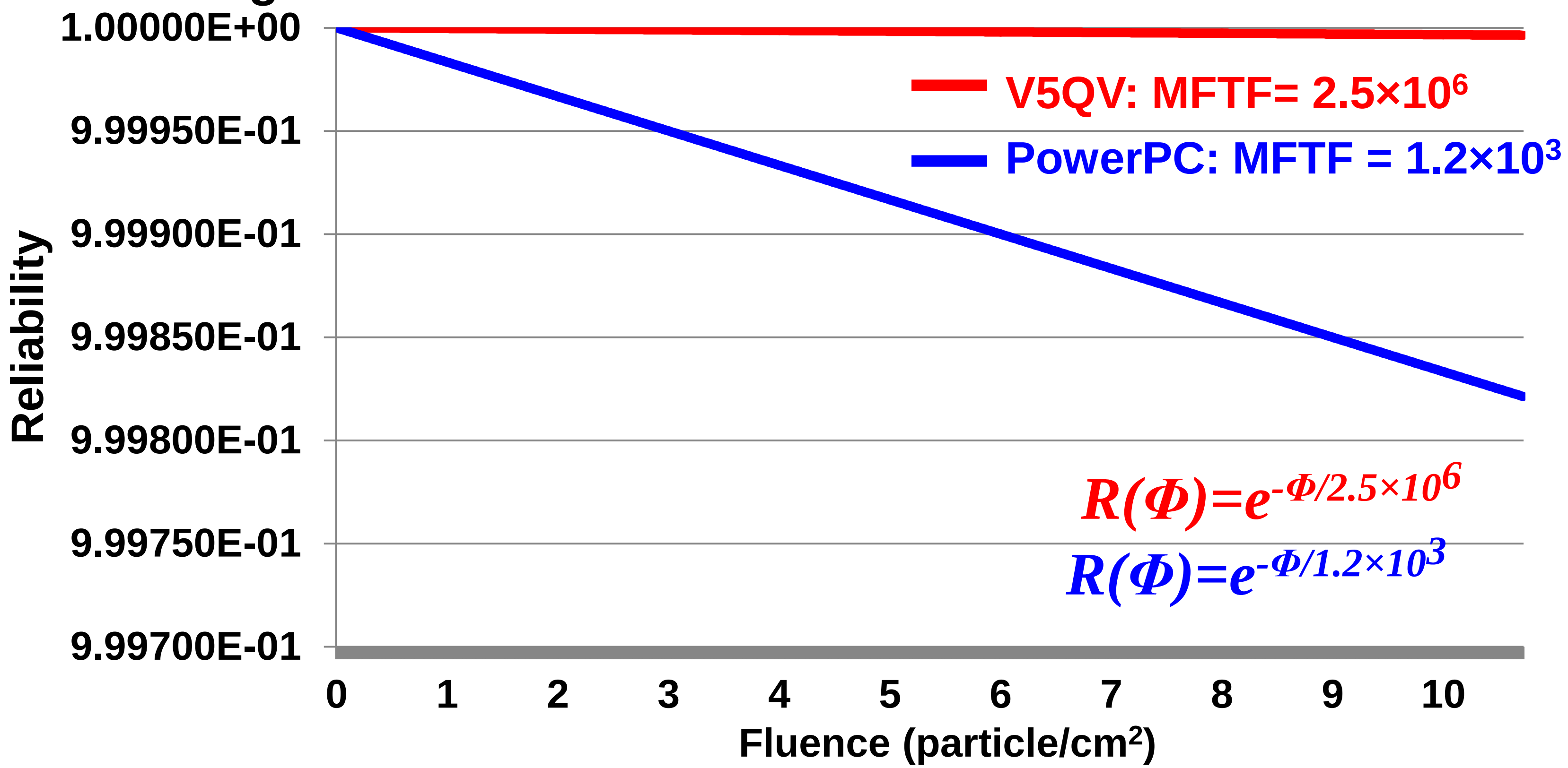
Binned GEO Environment data show approximately 9 particles/(cm²•10-minutes), in the range of 0.14MeV•cm²/mg to 1.8MeV•cm²/mg. We are using MFTF for 1.8MeV•cm²/mg to upper bound this bin.



Reliability at 9 particles/(cm²•10-minutes) > 99.9% for the PowerPC design implementation. This is the most susceptible bin for the system.

Reliability across Fluence up to LET=3.6MeV•cm²/mg

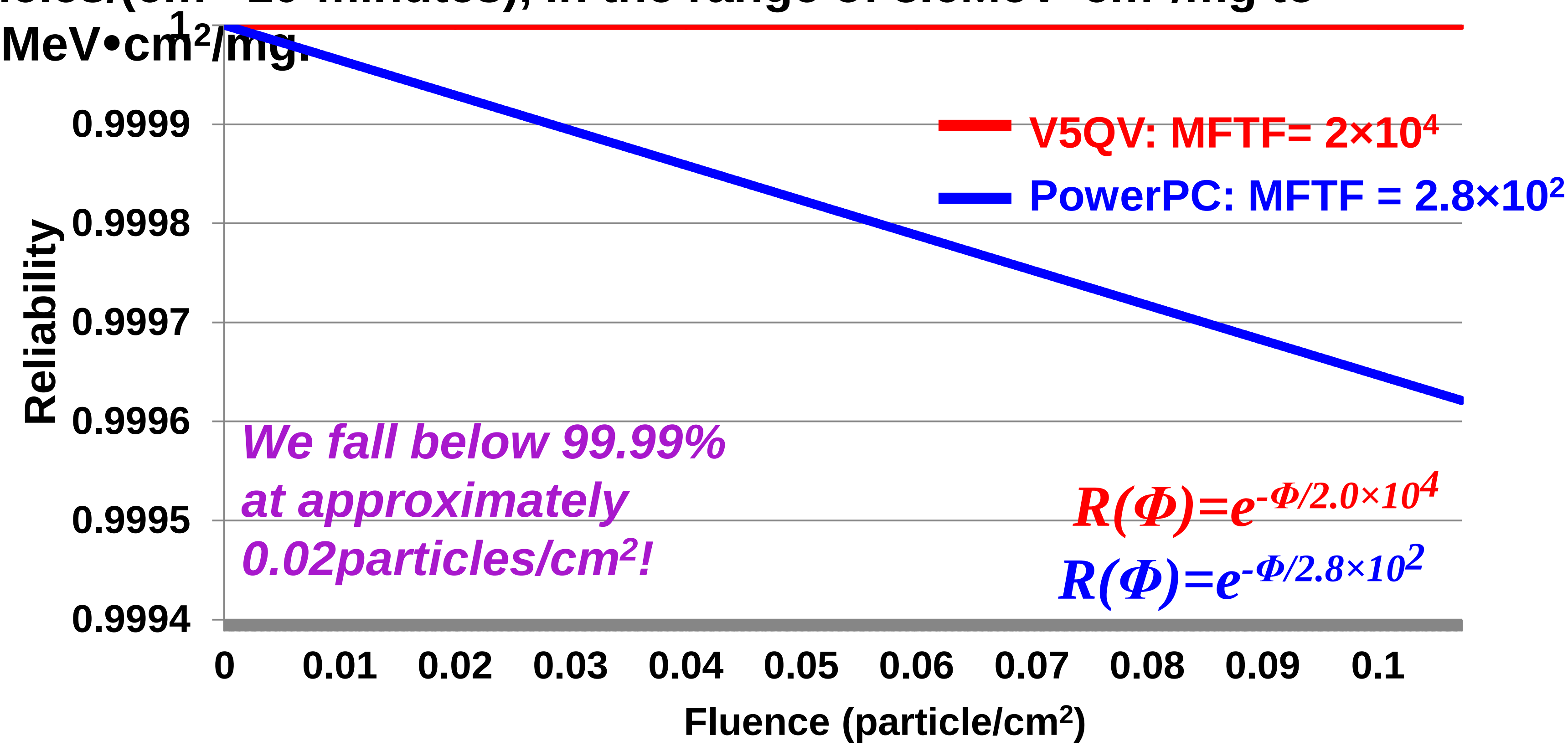
Binned GEO Environment data show approximately 0.23 particles/(cm²•10-minutes), in the range of 1.8MeV•cm²/mg to 3.6MeV•cm²/mg.



Within this LET range, reliability at 0.23 particles/(cm²•10-minutes) > 99.999% for both design implementations.

Reliability across Fluence at LET=40MeVcm²/mg

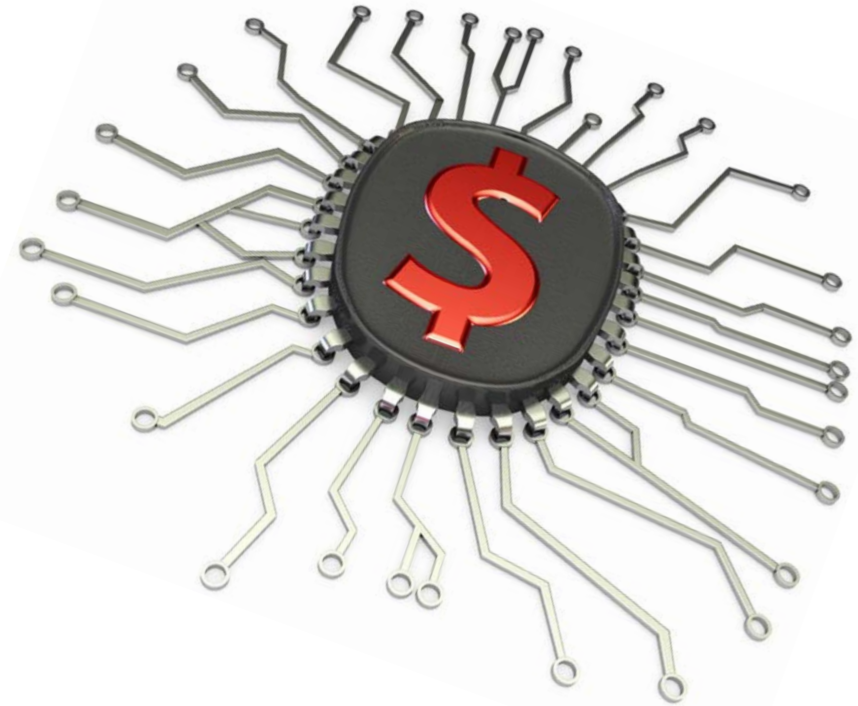
Binned GEO environment data show approximately 0.07 particles/(cm²•10-minutes), in the range of 3.6MeV•cm²/mg to 40.0MeV•cm²/mg.



Within this LET range, reliability at 0.07 particles/(cm²•10-minutes) > 99.9% for both design implementations. We can refine by analyzing smaller bins.

Example Conclusion

- **Using the proposed methodology, the commercial Xilinx V5 device will meet project requirements.**
- **In this case, the project is able to save money by selecting the significantly cheaper FPGA device and gain performance because of the embedded PowerPC.**



Conclusions

- **This study transforms proven classical reliability models into the SEU particle fluence domain. The intent is to better characterize SEU responses for complex systems.**
- **The method for reliability-model application is as follows:**
  - **SEU data are obtained as MFTF.**
  - **Reliability curves (in the fluence domain) are calculated using MFTF; and are analyzed with a piecemeal approach.**
  - **Environment data are then used to determine particle flux exposure within required windows of mission operation.**
- **The proposed method does not rely on data-fitting and hence removes a significant source of error.**
- **The proposed method provides information for highly SEU-susceptible scenarios; hence enables a better choice of mitigation strategy.**
- **This is preliminary work. There is more to come.**

This methodology expresses SEU behavior and response in terms that missions understand via classical reliability metrics.

Acknowledgements

- ***Some of this work has been sponsored by the NASA Electronic Parts and Packaging (NEPP) Program and the Defense Threat Reduction Agency (DTRA).***
- ***Thanks is given to the NASA Goddard Radiation Effects and Analysis Group (REAG) for their technical assistance and support. REAG is led by Kenneth LaBel and Jonathan Pellish.***

Contact Information:

Melanie Berg: NASA Goddard REAG FPGA Principal Investigator:

Melanie.D.Berg@NASA.GOV