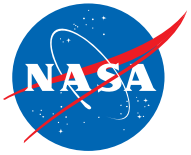


Prolonged 500 °C Operation of 100+ Transistor Silicon Carbide Integrated Circuits

David J. Spry[1], Philip G. Neudeck[1], Dorothy Lukco[2], Liangyu Chen[3], Michael J. Krasowski[1], Norman F. Prokop[1], Carl W. Chang[2], Glenn M. Beheim[1]

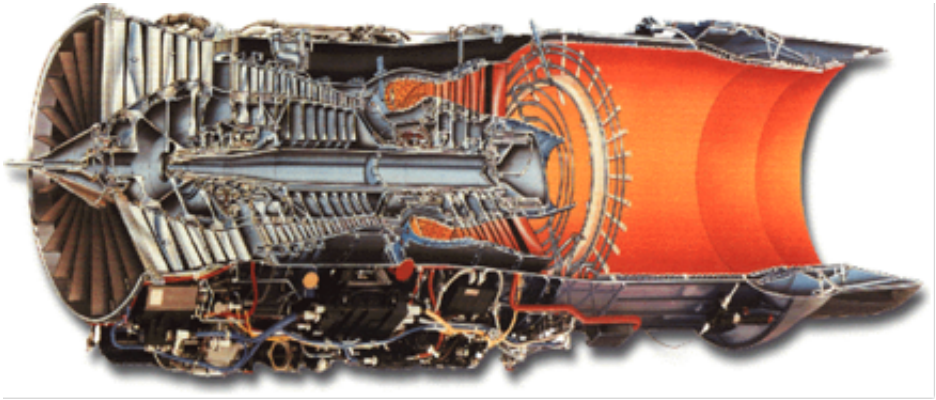
[1]NASA Glenn Research Center

[2]Vantage Partners LLC

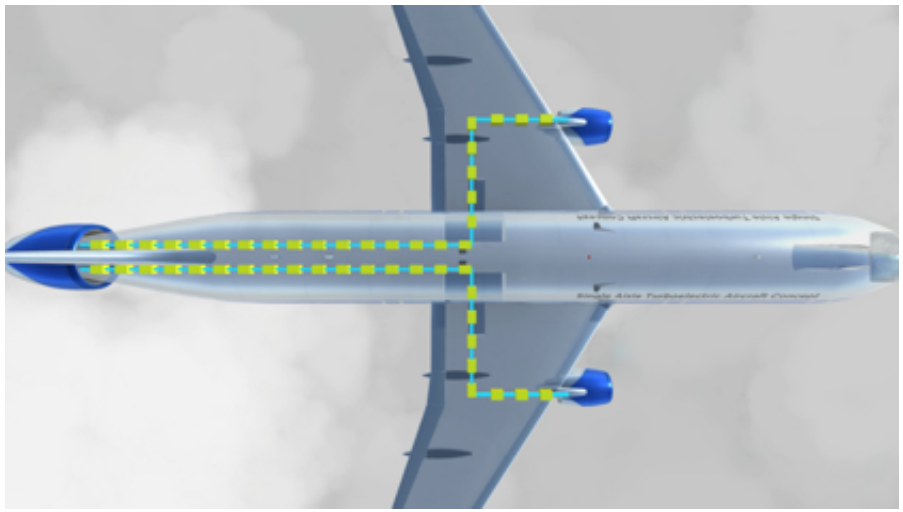
[3]Ohio Aerospace Institute

SiC Electronics Benefits to NASA Missions

Intelligent Propulsion Systems



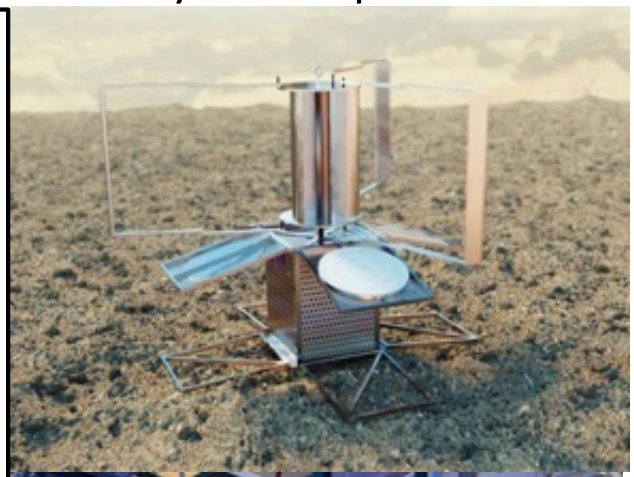
Hybrid Electric & Turbo Electric Aircraft



Venus Exploration

LLISSE = Long-Life In-Situ Solar System Explorer[1]

9.4 Mpa = 92.7X Earth pressure + 460 °C + chemical composition found at the surface of Venus (CO_2, N_2, SO_2, H_20, CO, OCS, HCl, HF, and H_2S)



NASA GRC's internal research effort has been to focused on durable/stable integrated circuit operation at 500 °C for > 1000 hrs.

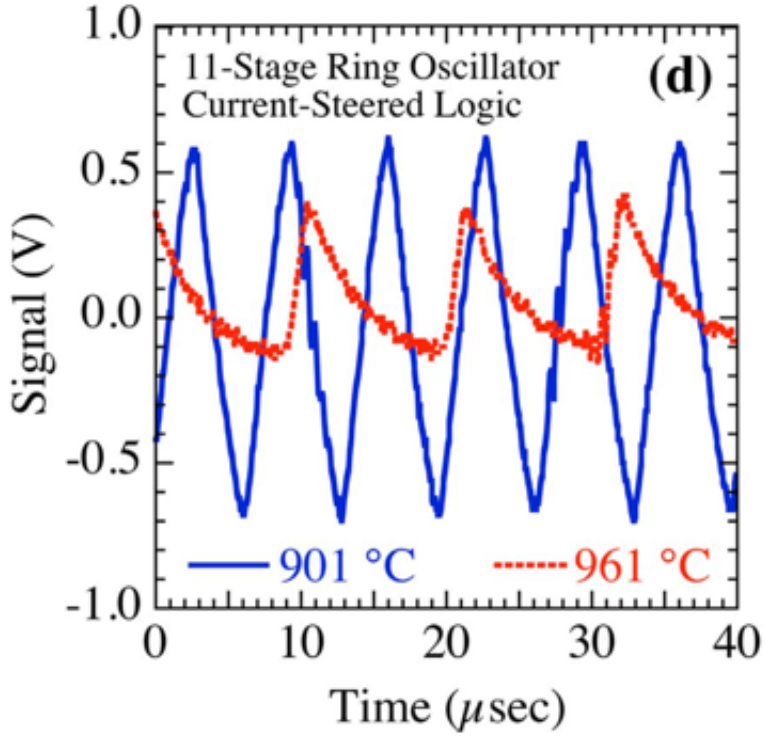
[1]T. Kremic, et al., 48th Lunar and Planetary Science, 2017, 2986.

Recent Advances

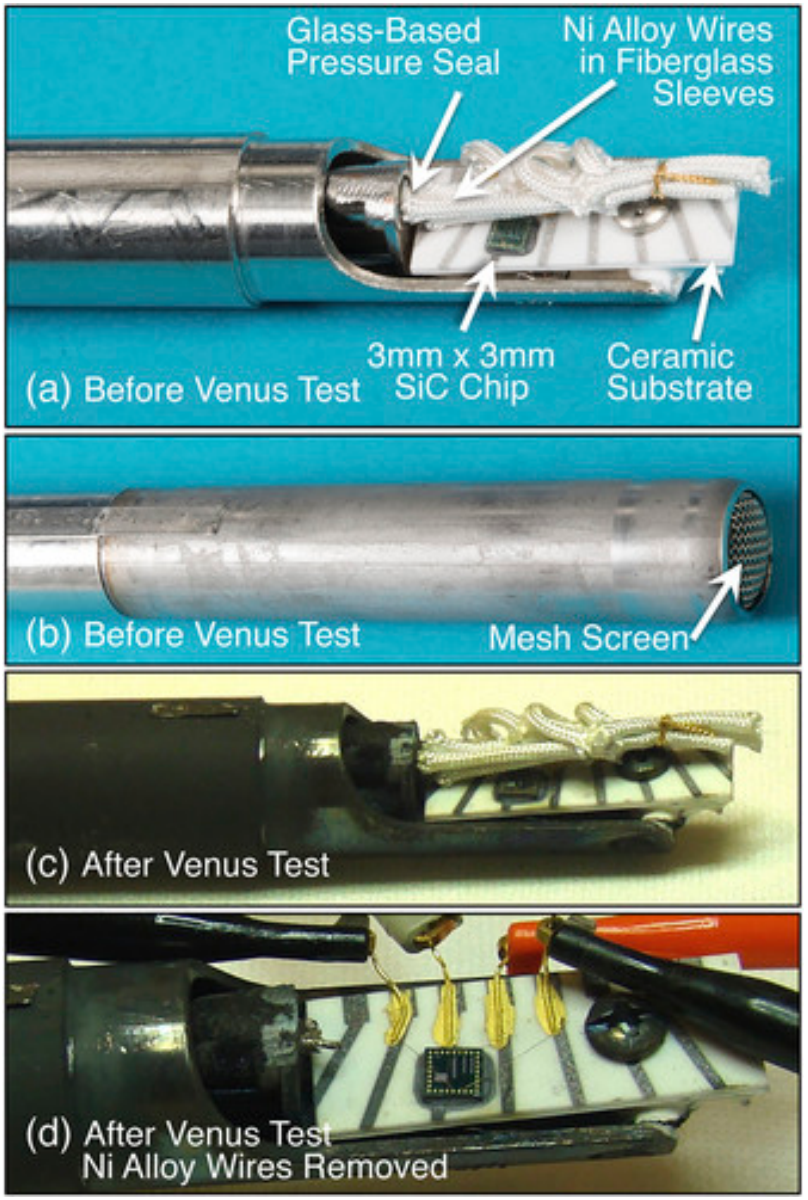
- *Prolonged silicon carbide integrated circuit operation in Venus surface atmospheric conditions*. Neudeck, et al., AIP Advances 6 (2016) 125119.

- *Demonstration of 4H-SiC Digital Integrated Circuits Above 800 °C*, Neudeck, et al., IEEE Electron Device Lett. 38 (2016) 1082-1085.

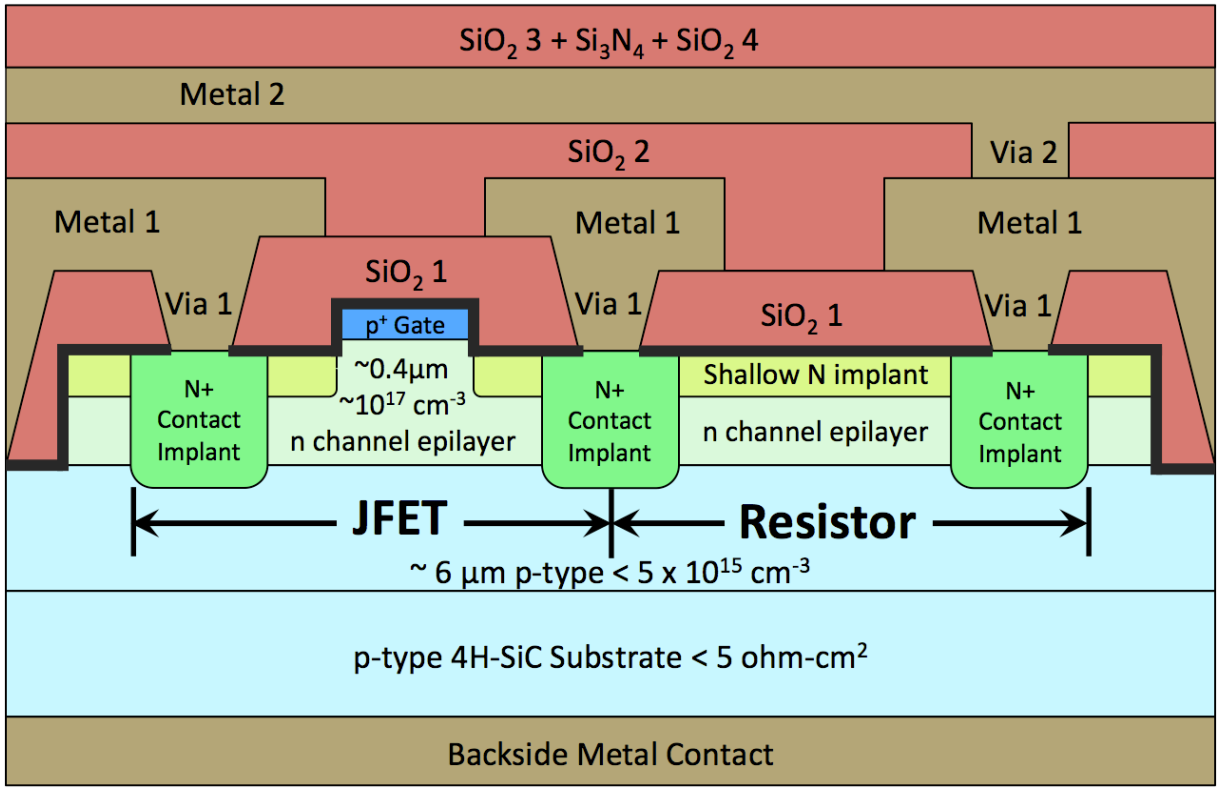
NASA SiC JFET IC operation at T > 900 ° C



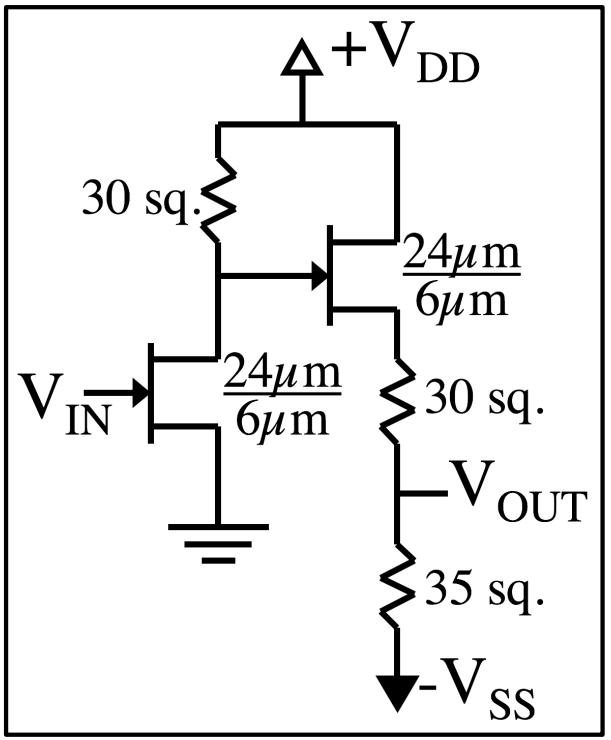
NASA SiC JFET IC operated directly immersed in Venus surface conditions (no package) for 3 weeks (did not fail)



N-channel JFET design[1,2] "Version 10.1"



NOT Logic Gate Schematic

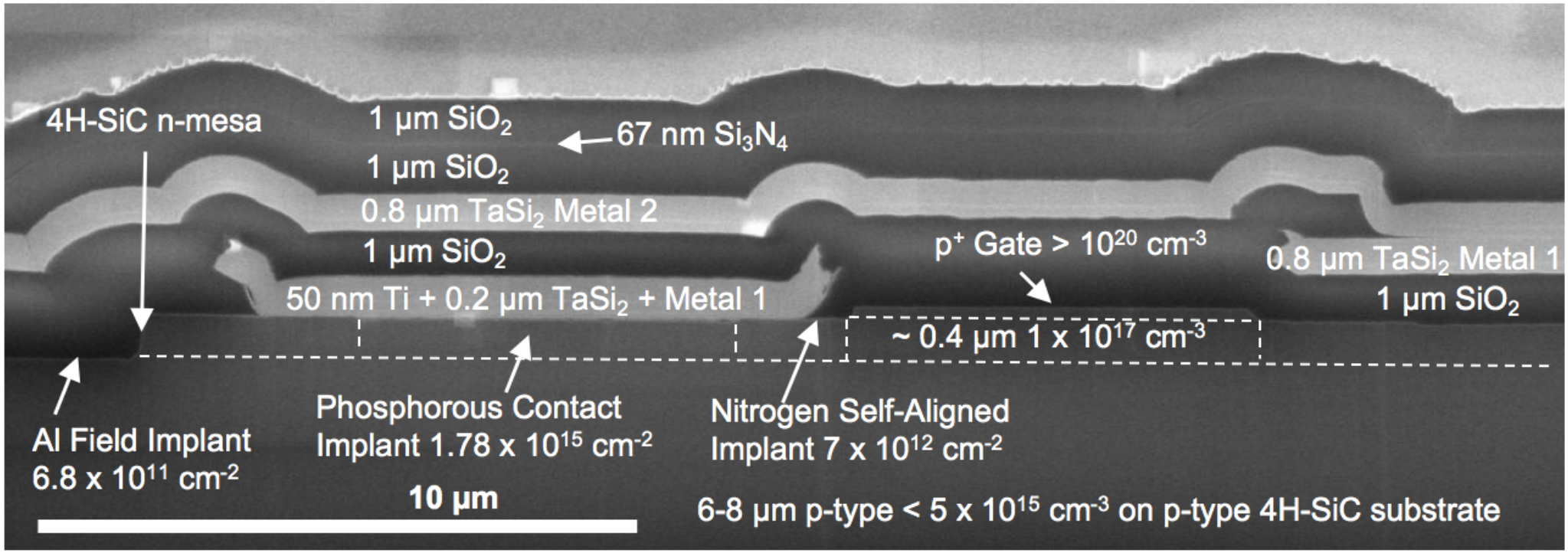


- Normally-on 4H-SiC JFET (fabricated at NASA Glenn)
- Resistors made with same epi as channel → matched T dependence
- Negative threshold voltage V_T → negative signal voltages (0 to -10V)
- 0 V = Binary 1 (high) -10 V = Binary 0 (low)

[1]M. J. Krasowski, US Patent 7,688,117 (2010).
[2]P. G. Neudeck, D. J. Spry, and L. Chen, Proc. IMAPS High Temperature Electronics Conf., 2016, pp. 263-271.

JFET IC Wafer 10.1 vs past work[1-2]

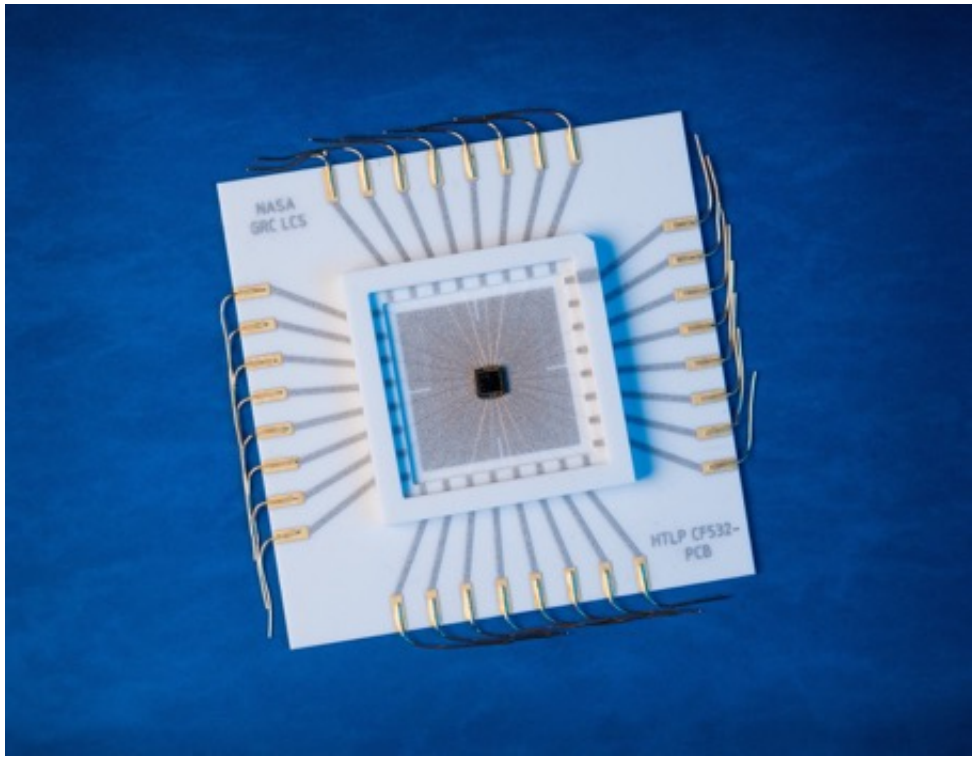
- **Aluminum** Field Stop Implant to impede parasitic field MOSFETs.
- Heavily-implanted SiC contact regions were formed using **phosphorus** implant profile with slightly lower energy & dose.
- Contact was made using 50 nm sputtered **titanium** layer.

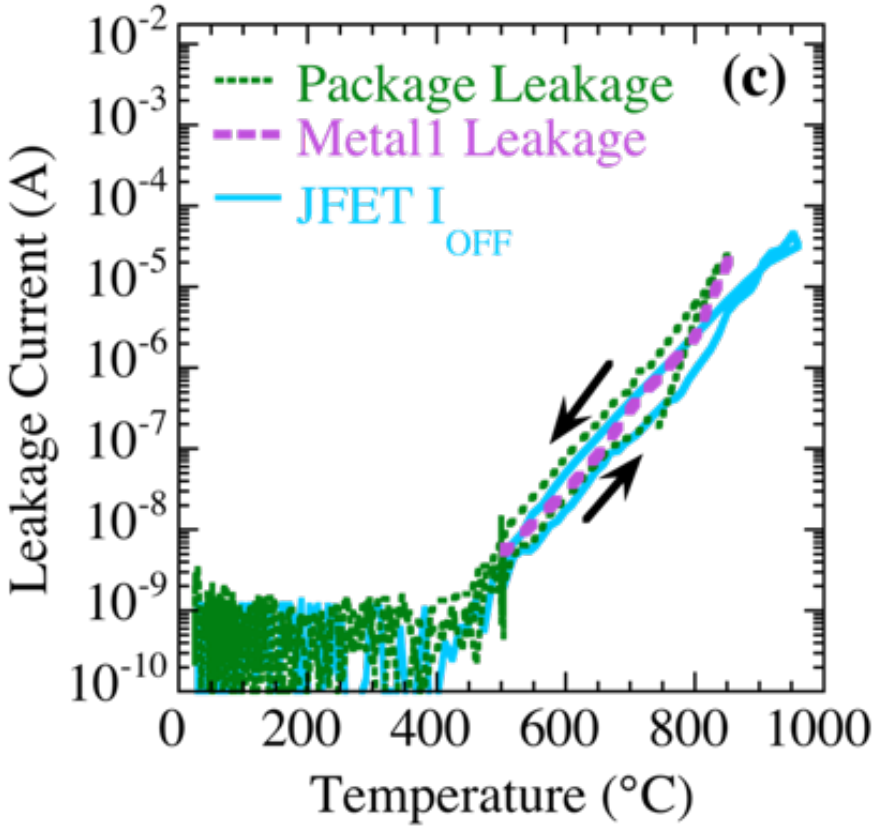


[1]D. J. Spry, et al., Mat. Sci. Forum 828 (2016) 908-912: "IC Wafer/Version 8.1"

[2]D. J. Spry, et al., IEEE Electron Device Lett. 37 (2016) 625-628: "IC Wafer/Version 9.2"

High-T packaging[1,2] (32 pins)

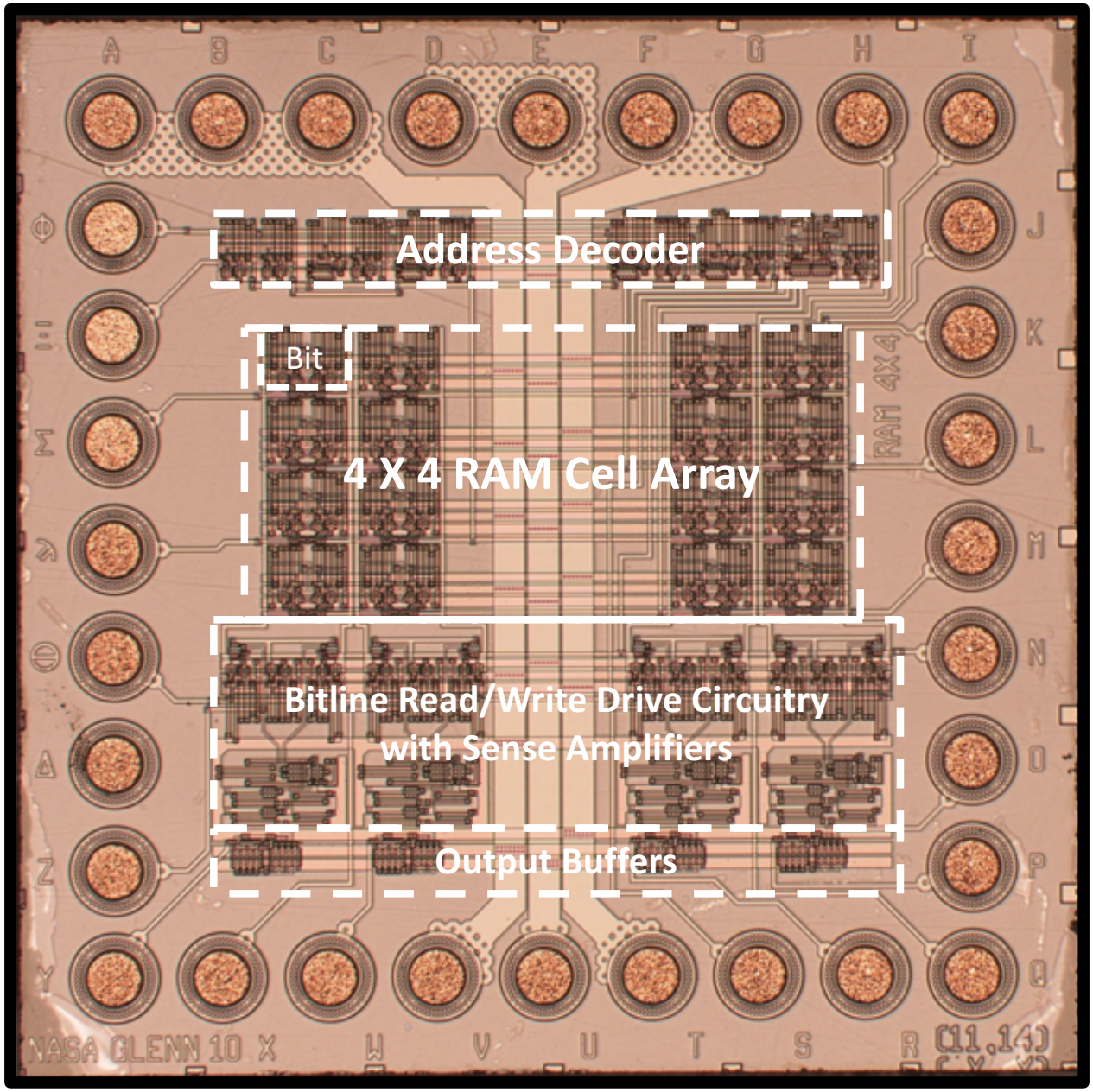




- Package durability and leakage characterized.

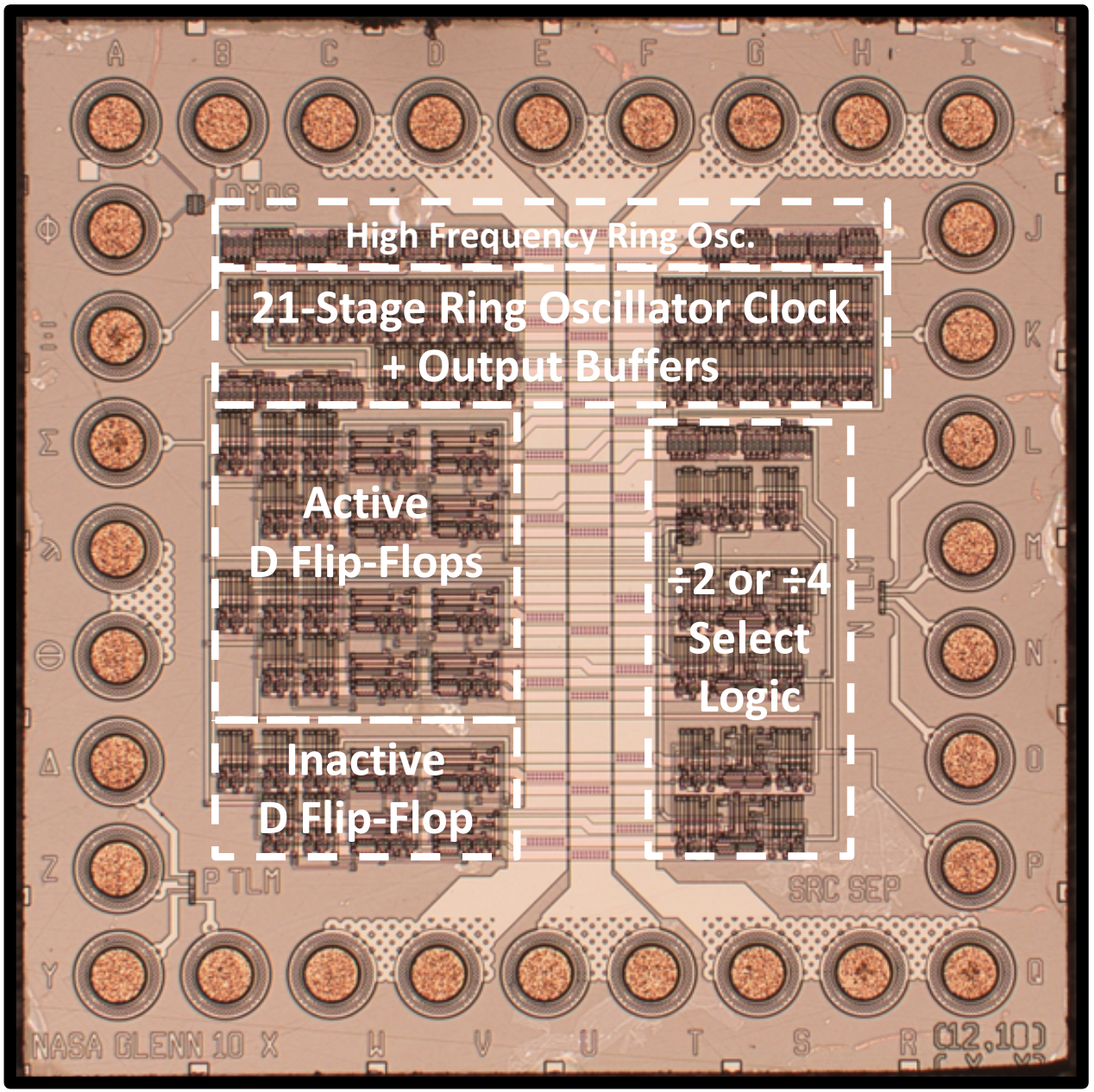
[1]L. Chen, et al., Proc. IMAPS High Temperature Electronics Conference, 2016, pp. 66-72.
[2]P. G. Neudeck, et al., IEEE Electron Device Lett. 38 (2016) 1082-1085.

4X4 Random Access Memory (RAM) Demonstration Chip



- 3mm x 3mm 4H-SiC JFET chip shown prior to packaging.
- 195 JFETs.
- 6-Transistor static RAM cell approach.
- Includes address decoders, read/ write bitline drive with sense amplifiers, output buffers.

÷2/÷4 Clock Demonstration Chip



- 3mm x 3mm 4H-SiC JFET chip prior to packaging.
- 175 JFETs
- 21-Stage ring oscillator provides base frequency clock signal
- SELECT data line:
  - High (0 V) → ÷4 output
  - Low (-10 V) → ÷2 output
- Includes two D-type flip flops governed by select logic
  - 3rd flip flop is inactive due to layout error.
- Optional modulation of high-f ring oscillator signal

Wafer 10.1 IC Functional Yield at 25 °C

Table I. 25 °C Probe Test Yield for 100+ JFET SiC ICs

Demonstration IC	IC JFET Count	# Good/# Tested $r \leq 25$ mm	% Yield $r \leq 25$ mm
16-bit RAM	195	19/27	70%
÷ 2/÷4 Clock	175	19/26	73%

- Probe-test measurements at 25 °C prior to wafer dicing and circuit packaging.
- JFET threshold voltage V_T on depends on distance from the center of the wafer ***r***, due to as-purchased wafer epilayer variation (see Ref. 1).
- Table I is for ***r*** < 25mm (on 38 mm radius wafer), the wafer region where V_T falls within circuit design specifications of $|V_T| < 10$ V.

[1]P. G. Neudeck, D. J. Spry, and L. Chen, Proc. IMAPS High Temperature Electronics Conf., 2016, pp. 263-271.

Wafer 10.1 500 °C Packaged IC Tests

Table II. Summary of 500 °C Packaged IC Tests

Packaged IC Sample	500 °C Test Hours	Status
16-bit RAM #1	1525 h	Suspended
16-bit RAM #2	5040 h	Running
÷2/÷4 Clock #1	470 h	Failed
÷2/÷4 Clock #2	5200 h	Running
÷2/÷4 Clock #3A	4377 h	Running
÷2/÷4 Clock #3B	4377 h	Running
÷2/÷4 Clock #3C	2090 h	Failed

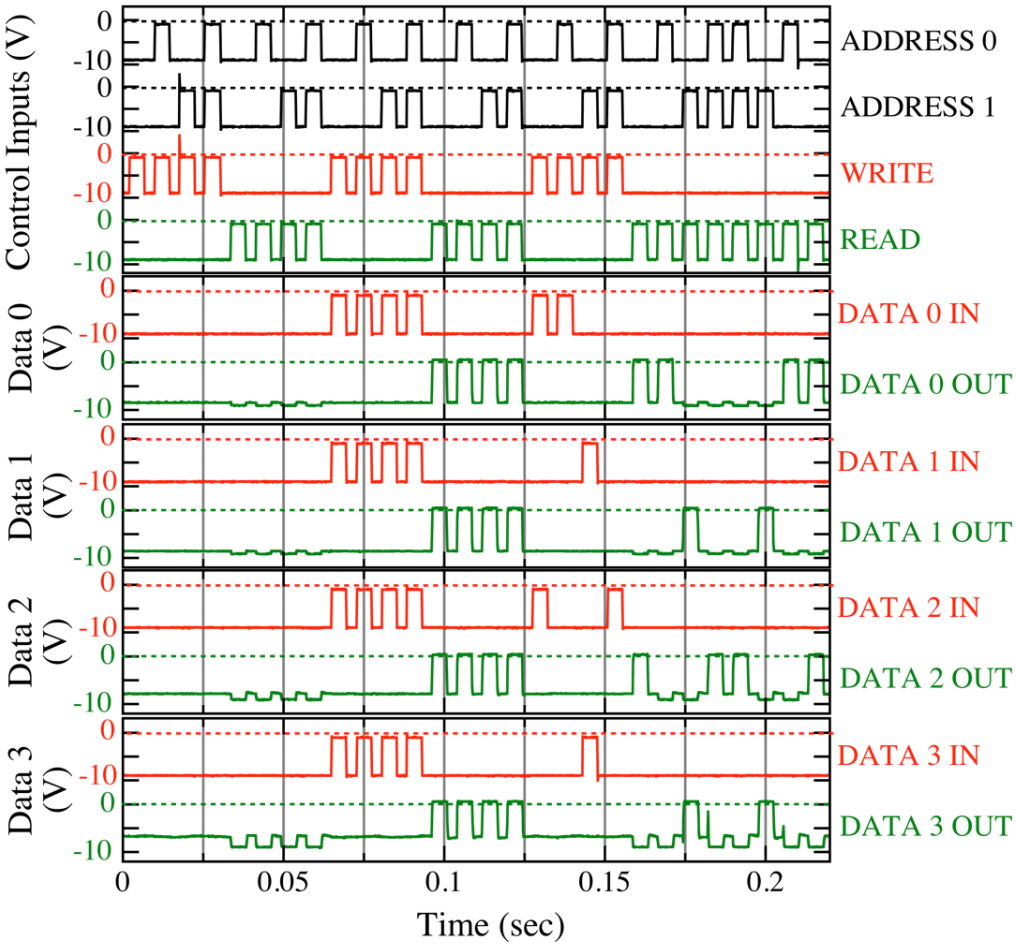
RAM#1 was tested as 12-bit due to damage/failure of one row/word line during packaging.

Clock chips 3A, 3B, 3C reside in same package.

4X4 RAM #2

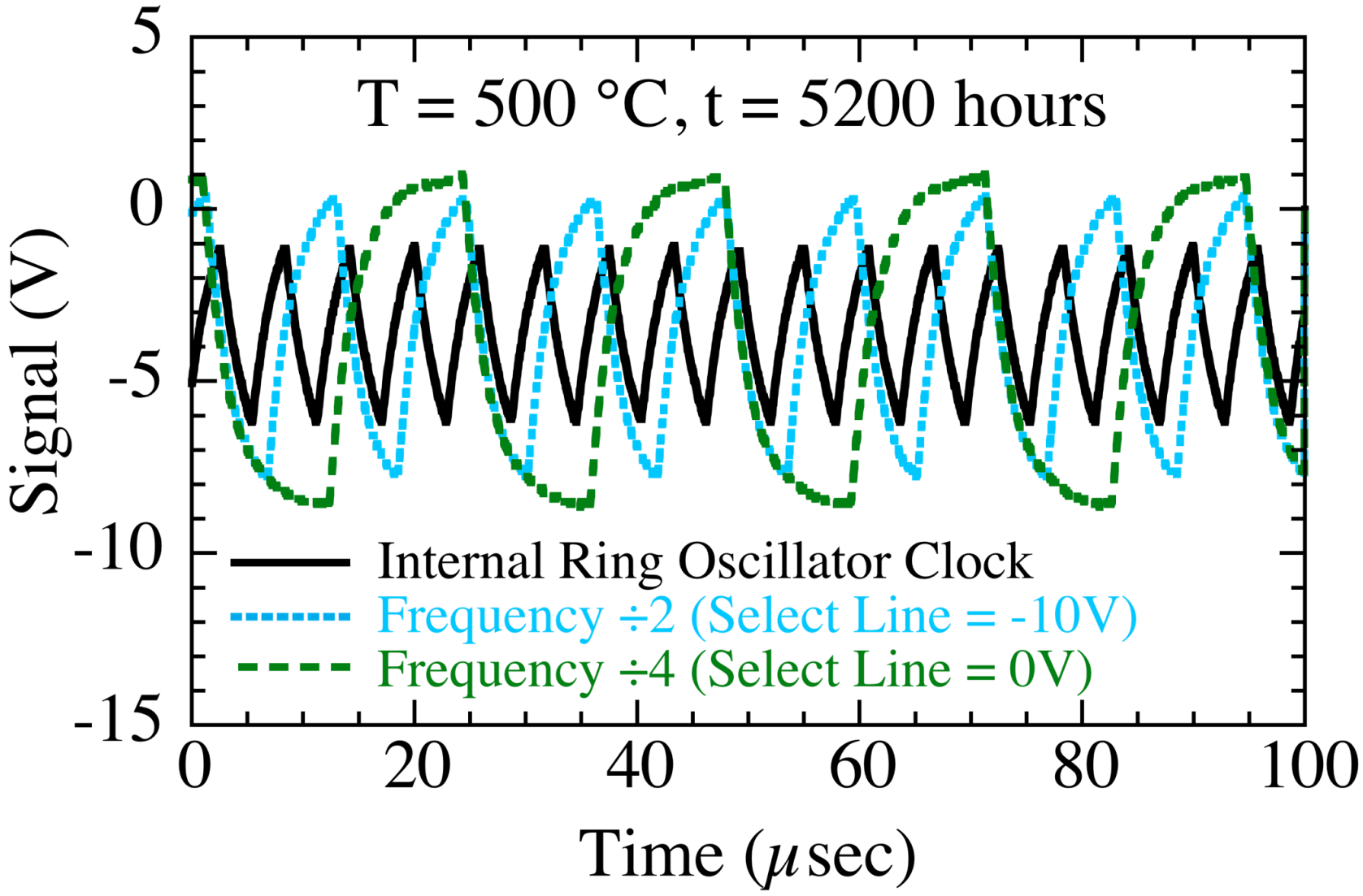
16-Bit (4 x 4) RAM Test Waveforms
T = 500 °C, t = 5040 hours

Write	Read	Write	Read	Write	Read	Reverse Address Order Read	Bitline Column
0000	0000	1111	1111	1100	1100	0011	Data 0
0000	0000	1111	1111	0010	0010	0100	Data 1
0000	0000	1111	1111	1001	1001	1001	Data 2
0000	0000	1111	1111	0010	0010	0100	Data 3



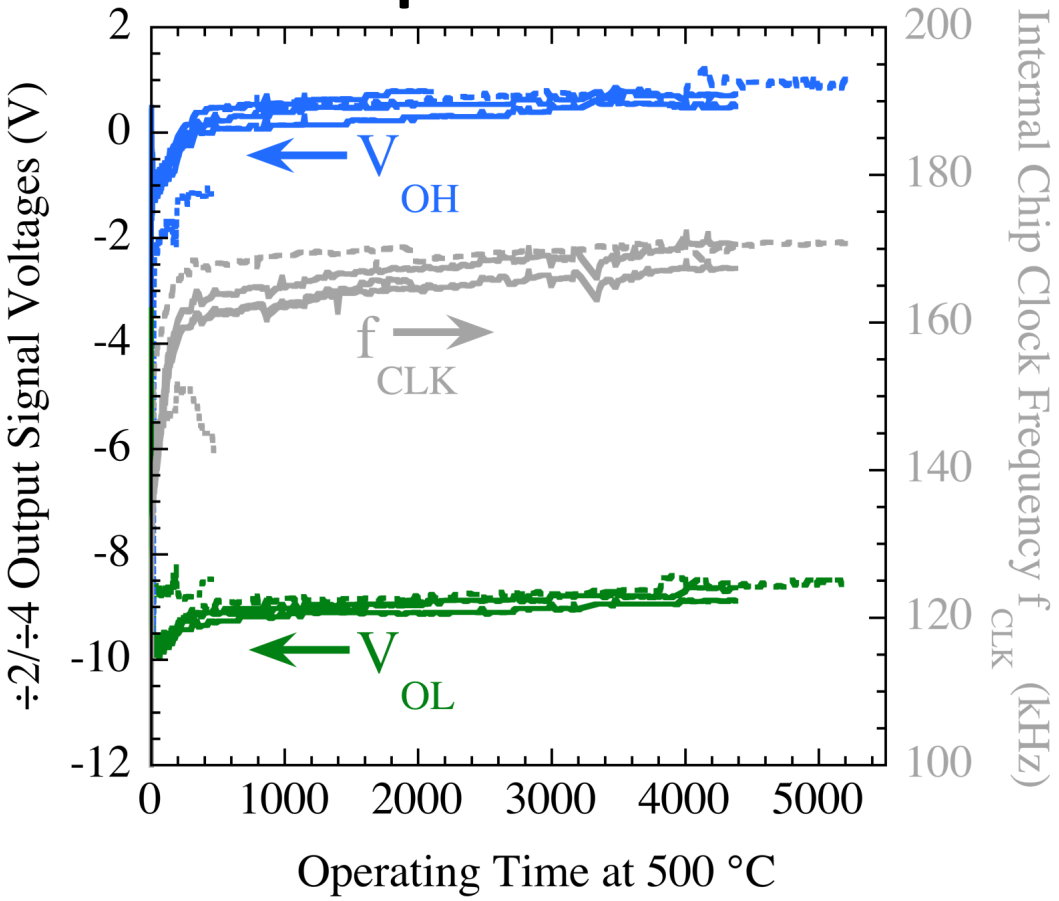
- Measured 16-bit RAM waveforms showing read and write functionality of all bits at 5040 hours of a 500 °C oven test.

÷2/÷4 Clock Chip #2



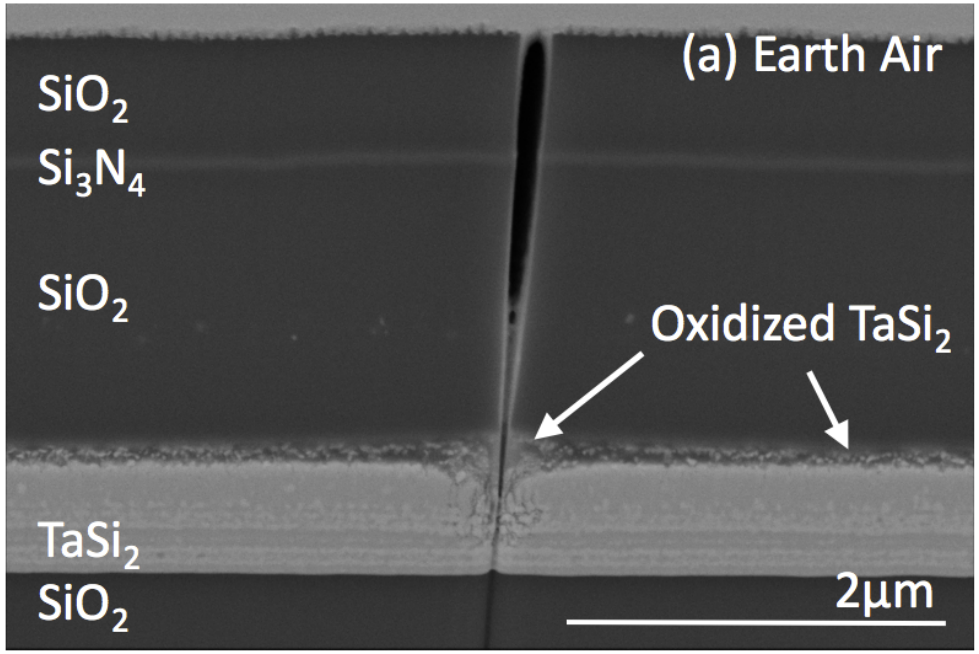
- Measured waveforms showing operation of ÷2/÷4 clock IC at 5200 hours of 500 °C oven testing.

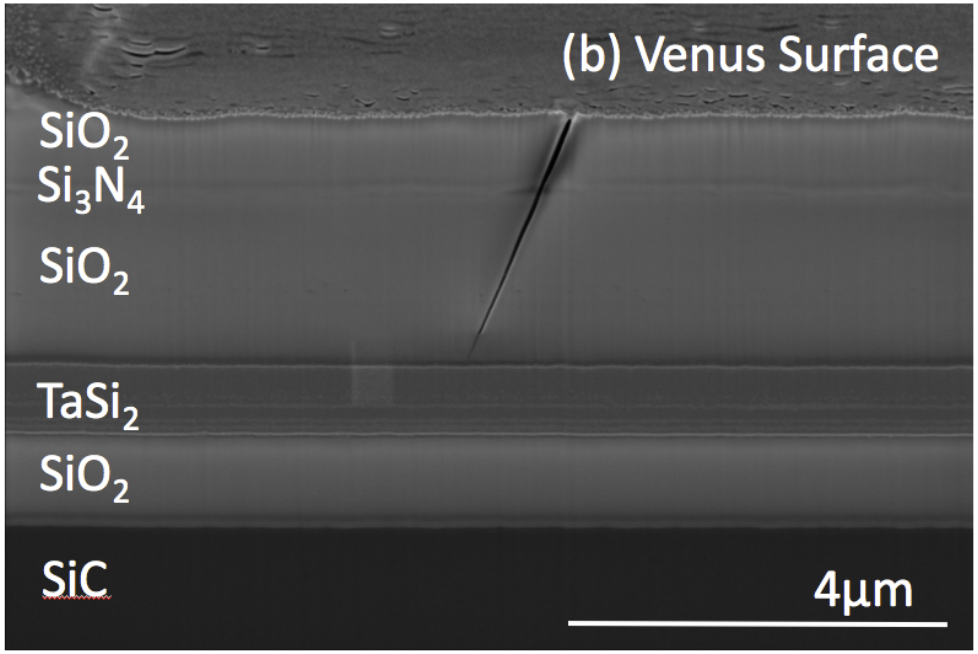
÷2/÷4 Clock Chips vs Time at 500 ° C



- Time evolution of ÷2/÷4 clock IC output voltages and frequency for 5 packaged chips subjected to prolonged 500 °C oven testing.
- After initial burn-in, output characteristics change < 10%
- 3 of 5 chips remain functioning under 500 °C test.

Venus Environment Durability FIB FESEM





(a) Crack typical of prolonged T ≥ 500 °C testing in air (727 °C for this sample)

- In Earth environment, the crack allows the top surface of the $TaSi_2$ film to oxidize which exacerbates failure.

(b) Crack in IC sample tested in Venus surface condition.

- In Venus environment, the crack reaches the top of the $TaSi_2$ but does not propagate through the $TaSi_2$ and there is no observable evidence of $TaSi_2$ film oxidation.

Other samples exposed to Venus

- Platinum forms Platinum Sulfide.
  - 200nm thick films completely converted.
- Many morphologies found dependent on surrounding materials.
- Transition metals react to form sulfides.
- Trace amounts of HCl at 0.5 ppm and HF at 2.5 ppb that were found as reacted products in some samples.
- **Temperature and/or pressure without including the complete chemistry is not a sufficient means of screening electronics for long-term operation in the Venusian surface environment.**
- SiC, SiO_2, Al_2O_3 remain stable.

Summary

- The complexity of 4H-SiC JFET IC's proven durable for 1000's of hours at 500 °C has been substantially increased from 24 transistors to 175+ transistors.

- Testing in high-fidelity reproduction of the Venus surface environment is necessary to continue electronics development and qualification testing building towards long-term Venus surface missions.

Acknowledgements

Funded by **NASA Transformative Aeronautics Concepts Program**

HX5 Sierra

- Kelley Moses
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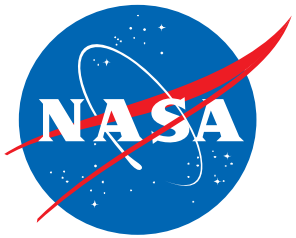
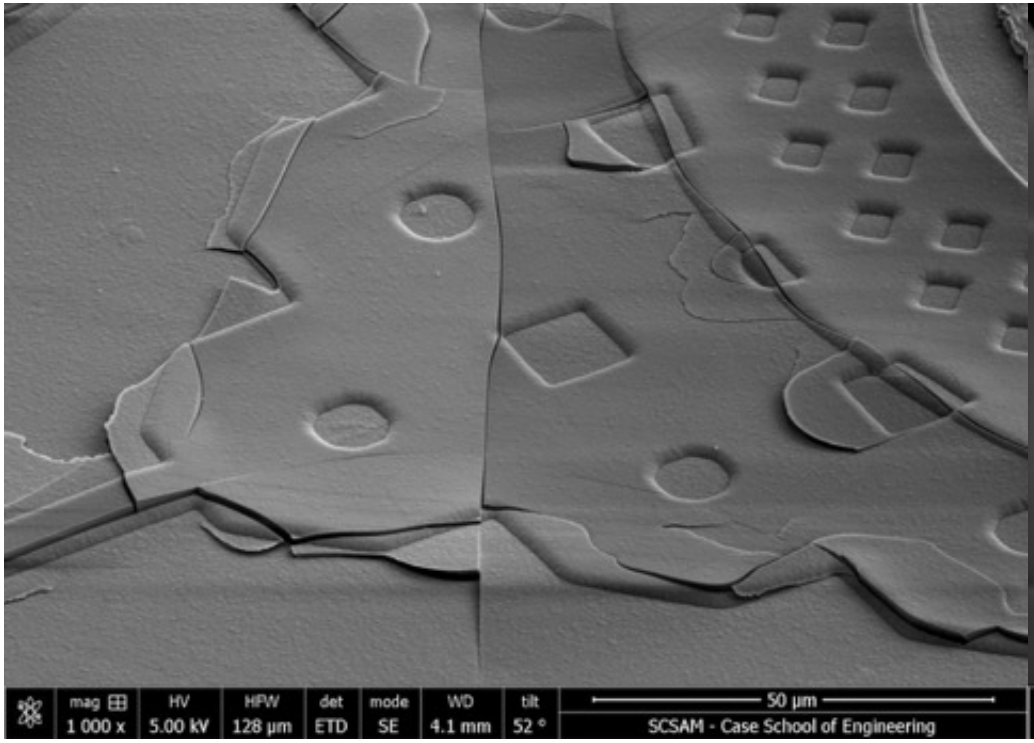
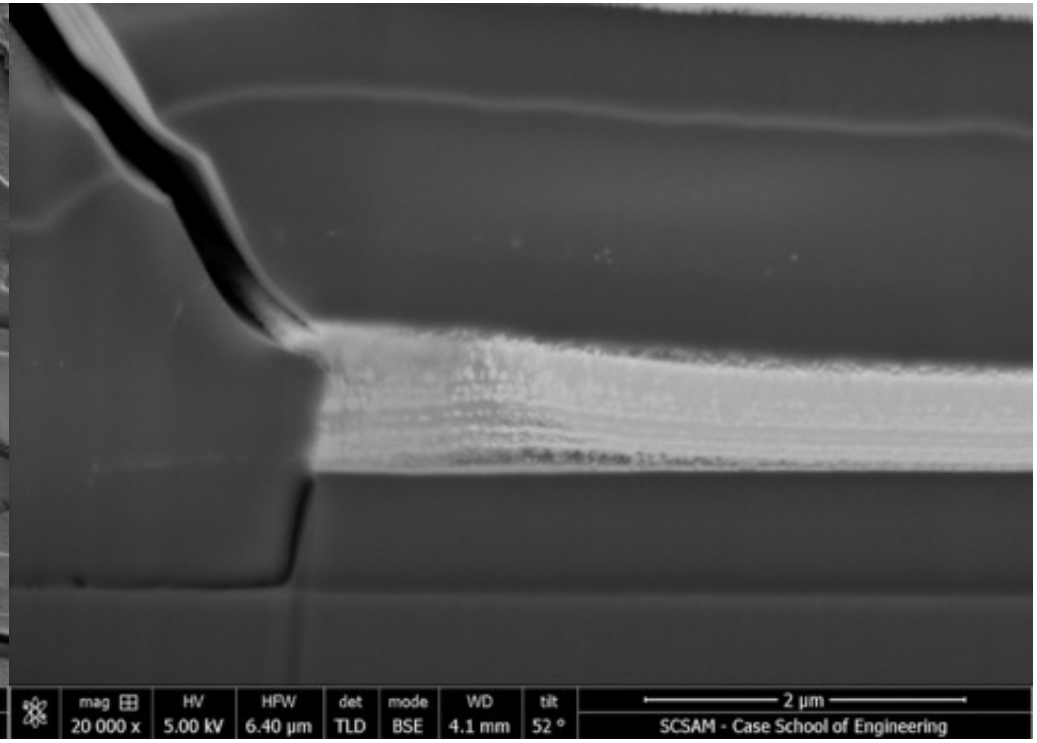

NASA

STARC-ABL: Single-aisle Turboelectric AiRCraft with Aft Boundary Layer propulsion

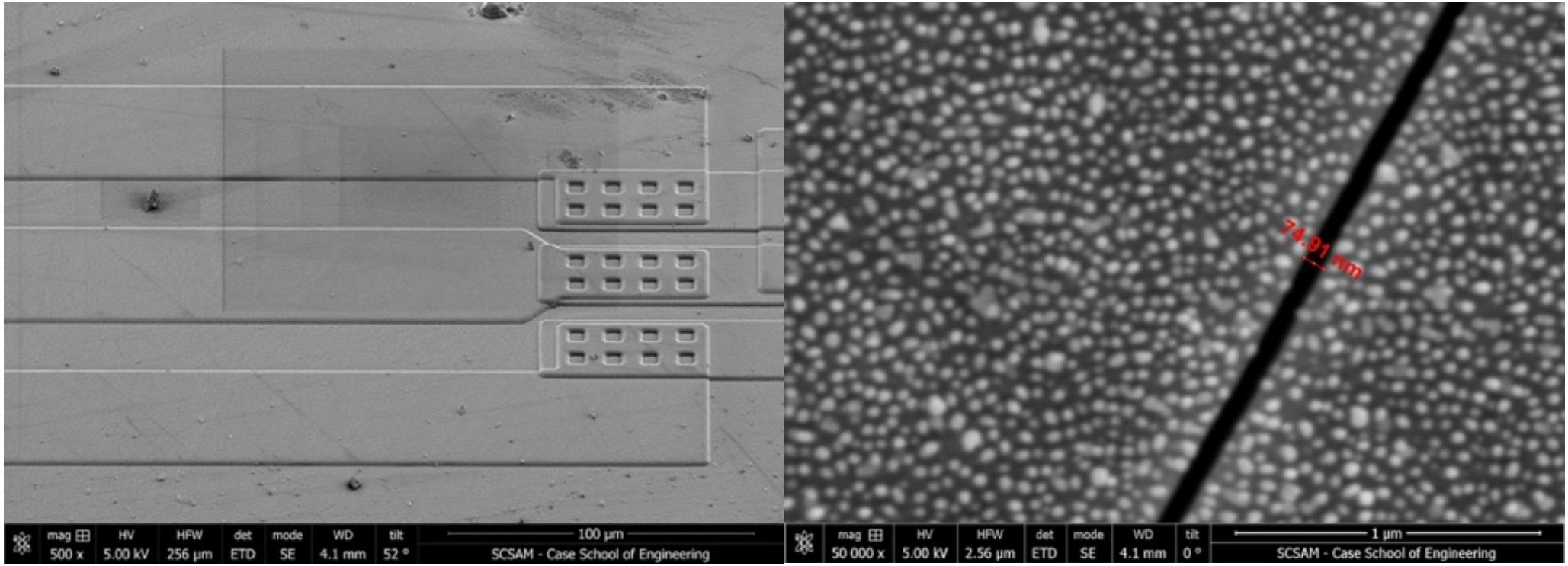
Typical Crack Propagation in Earth Air



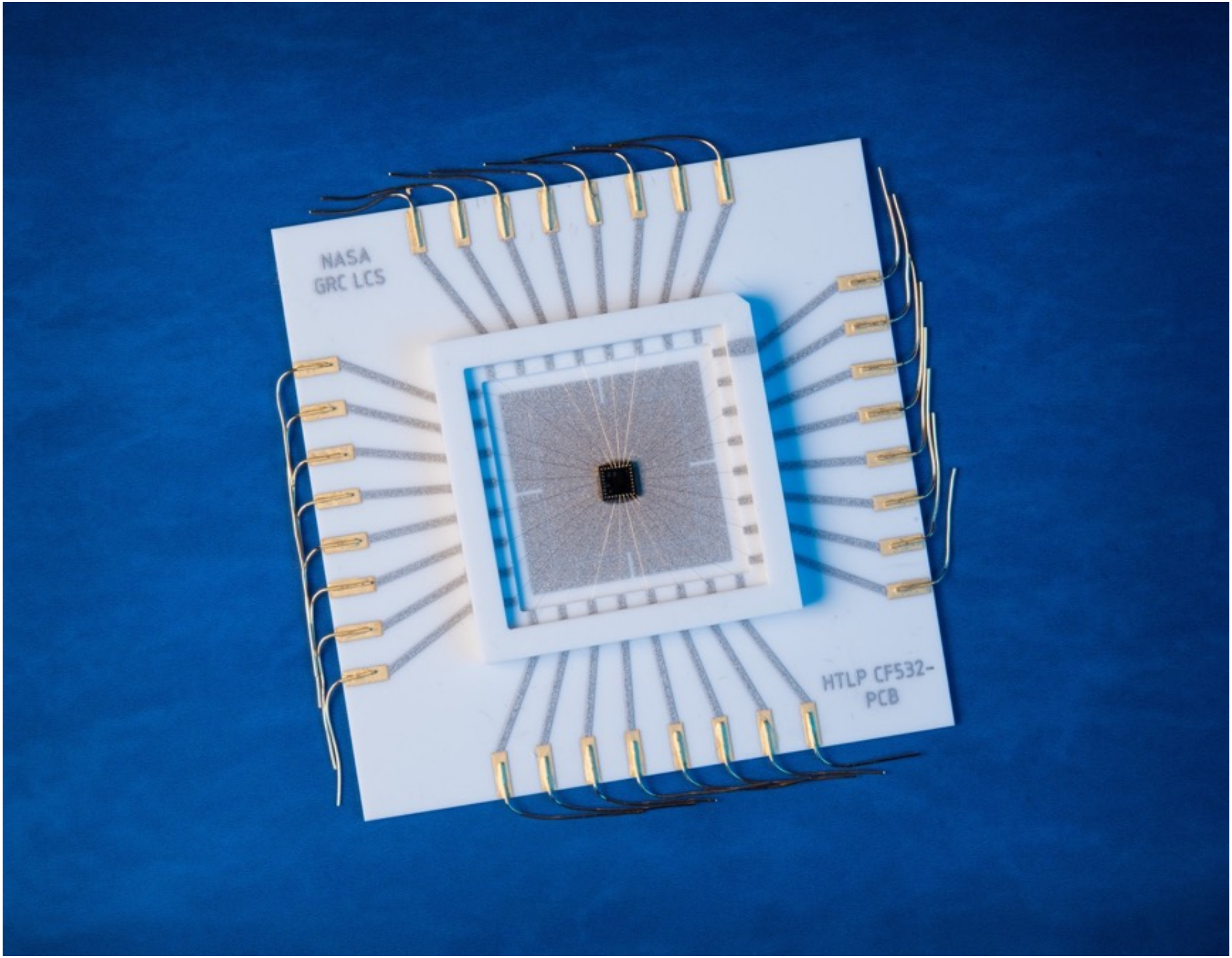


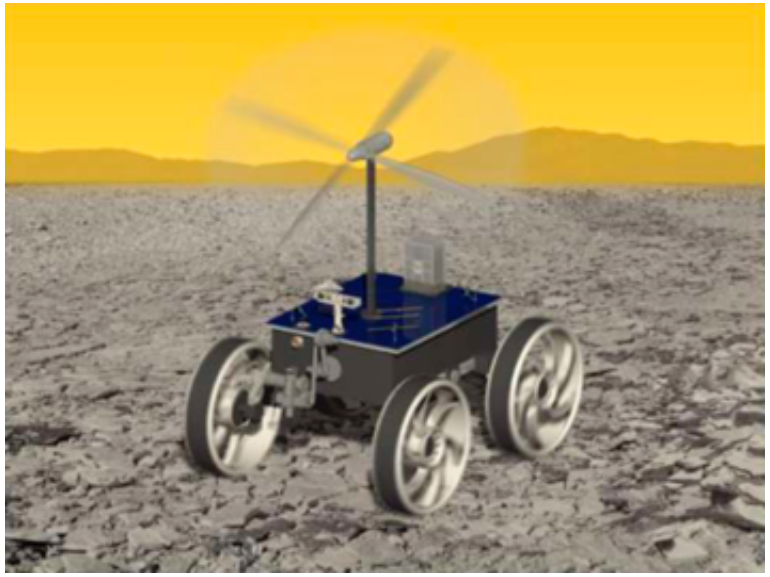
- This sample was at 727 °C sample and a old (Version 9.2) design. Same kind of behavior when seen on some 500 °C samples.
- Cracks related to dicing, handling, design rules, and bonding.
- Various degrees of oxidation and peeling seen.
- Oxidation of TaSi2 surface can be many 10s of microns wide.

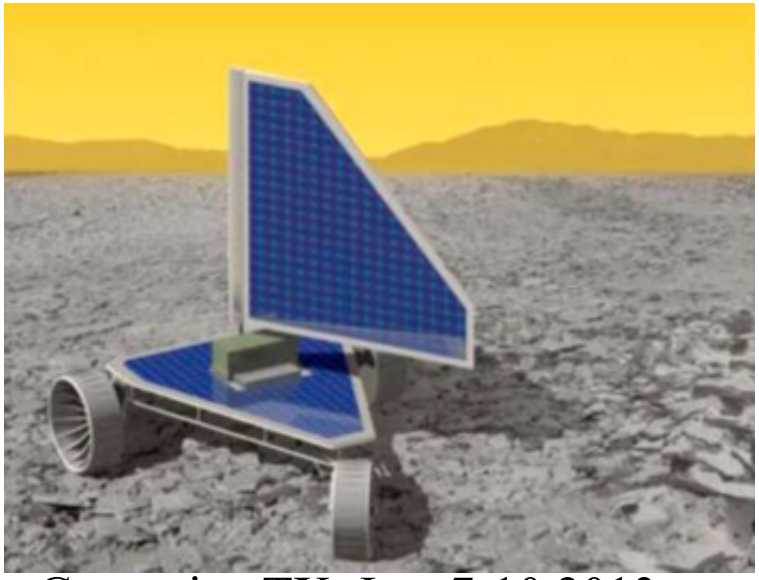
Crack at Venus Surface Conditions



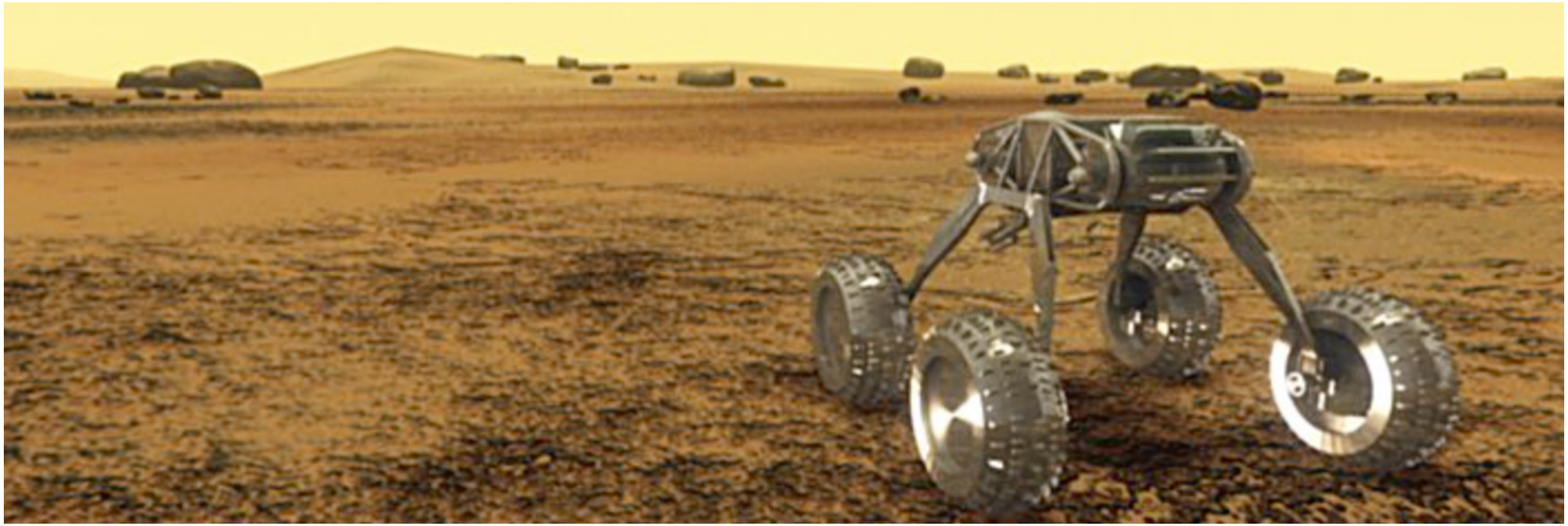
- Only one crack seen on entire sample exposed to Venus.
- Found via optical microscope and then examined on SEM. Hard to find with FESEM.
- Very small (~ 75 nm) when viewed from the top.


NASA
GRC LCS
HTLP CF532-
PCB





AIAA-2013-0586, 5*1st AIAA Aerospace Sciences Meeting*, Grapevine TX, Jan. 7-10 2013



G. Landis, "Robotic Exploration of the Surface and Atmosphere of Venus," *Acta Astronautica, Vol. 59*, 7, 517-580 (October 2006). Paper IAC-04-Q.2.A.08