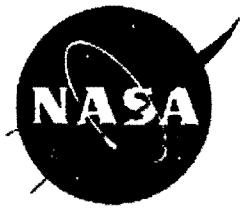


SpaceCube:
Current Missions and Ongoing Platform Advancements

NOTE: Handout Version

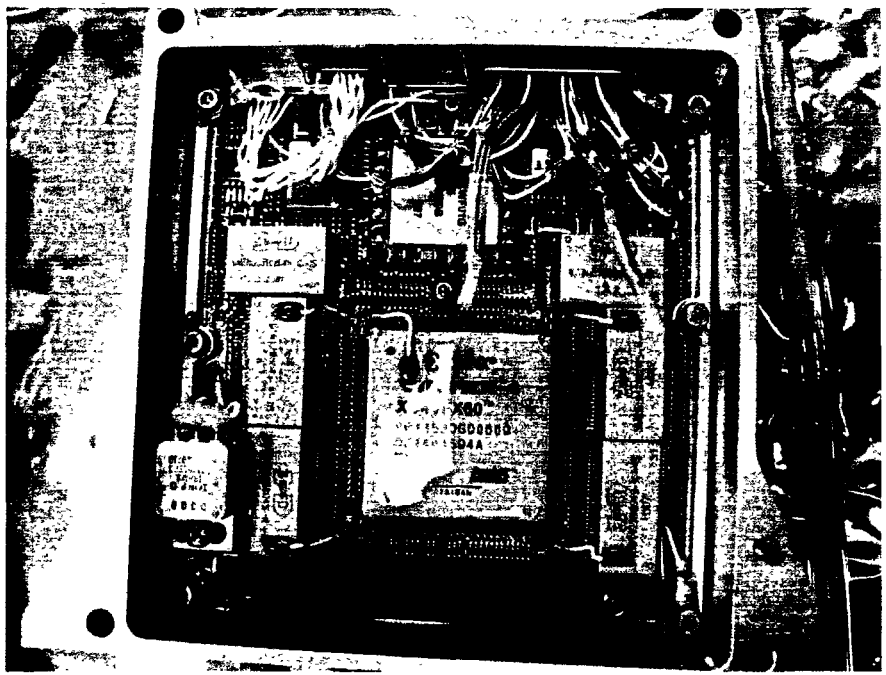
Dave Petrick
NASA/GSFC
Code 587

9/3/2009

GSFC SpaceCube

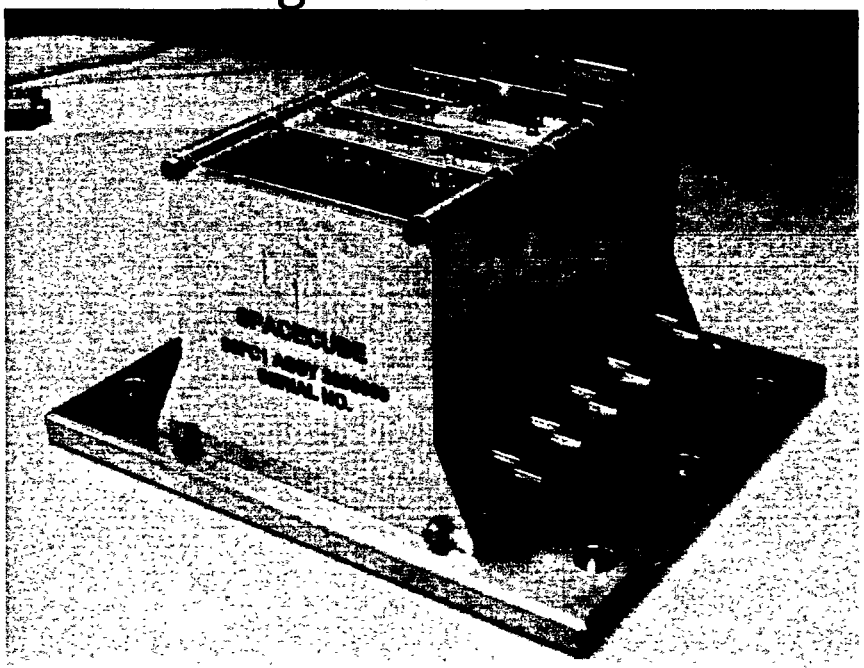
- Small, light-weight, reconfigurable multi-processor platform for space flight applications demanding extreme processing capabilities
- Stackable architecture
- Based on Xilinx Virtex 4 FX60 FPGAs, 2 per processor card
- **Successful flight demonstration on STS-125**

Processor Card



2 Xilinx FPGAs, 2 Aeroflex FPGAs
1GB SDRAM, 1GB Flash

Flight Box



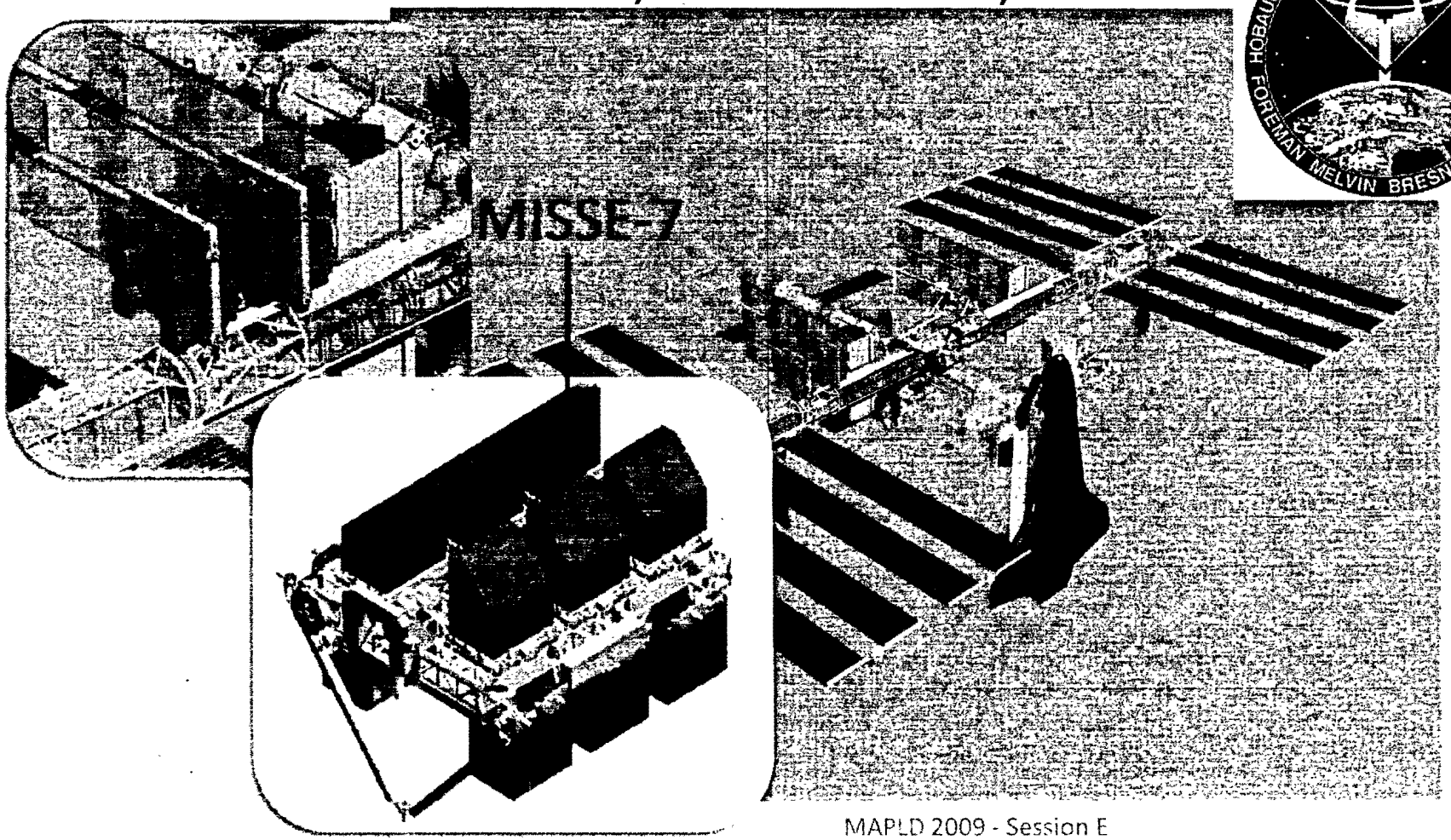
Mechanical: 7.5-lbs, 5"x5"x7"
Power: 37W (STS-125 Application)

Current Tasks

- SpaceCube 1.0: RNS flight spare to ISS (Nov 09)
  - Platform for testing radiation mitigation techniques starting with Rad-Hard by Software (RHBS)
  - Collaborating with industry and universities
- SpaceCube 1.5: Sounding Rocket Avionics
  - DoD **O**perationally **R**esponsive **S**pace payload funding
  - Feature Xilinx Virtex 5 FX100 with gigabit interfaces
- SpaceCube 2.0: Increased performance over SC1.X
  - ESTO funding → Prototype FY10, Engineering Unit FY12
  - For missions requiring high data rates and/or onboard science data processing

MISSE-7 Overview

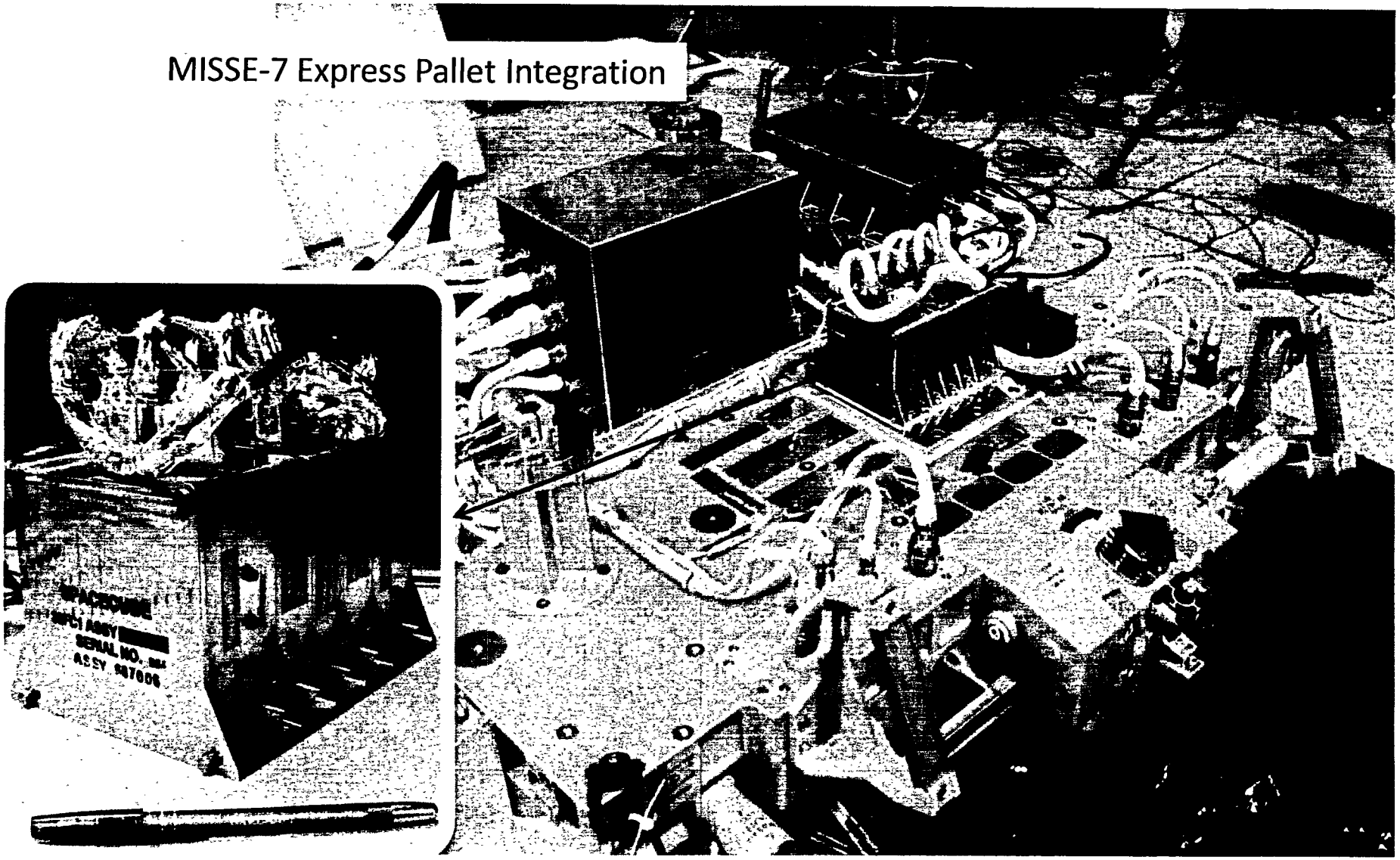
- Materials International Space Station Experiment
- Payload Lead: Naval Research Lab
- STS-129 Shuttle Atlantis, November 12, 2009



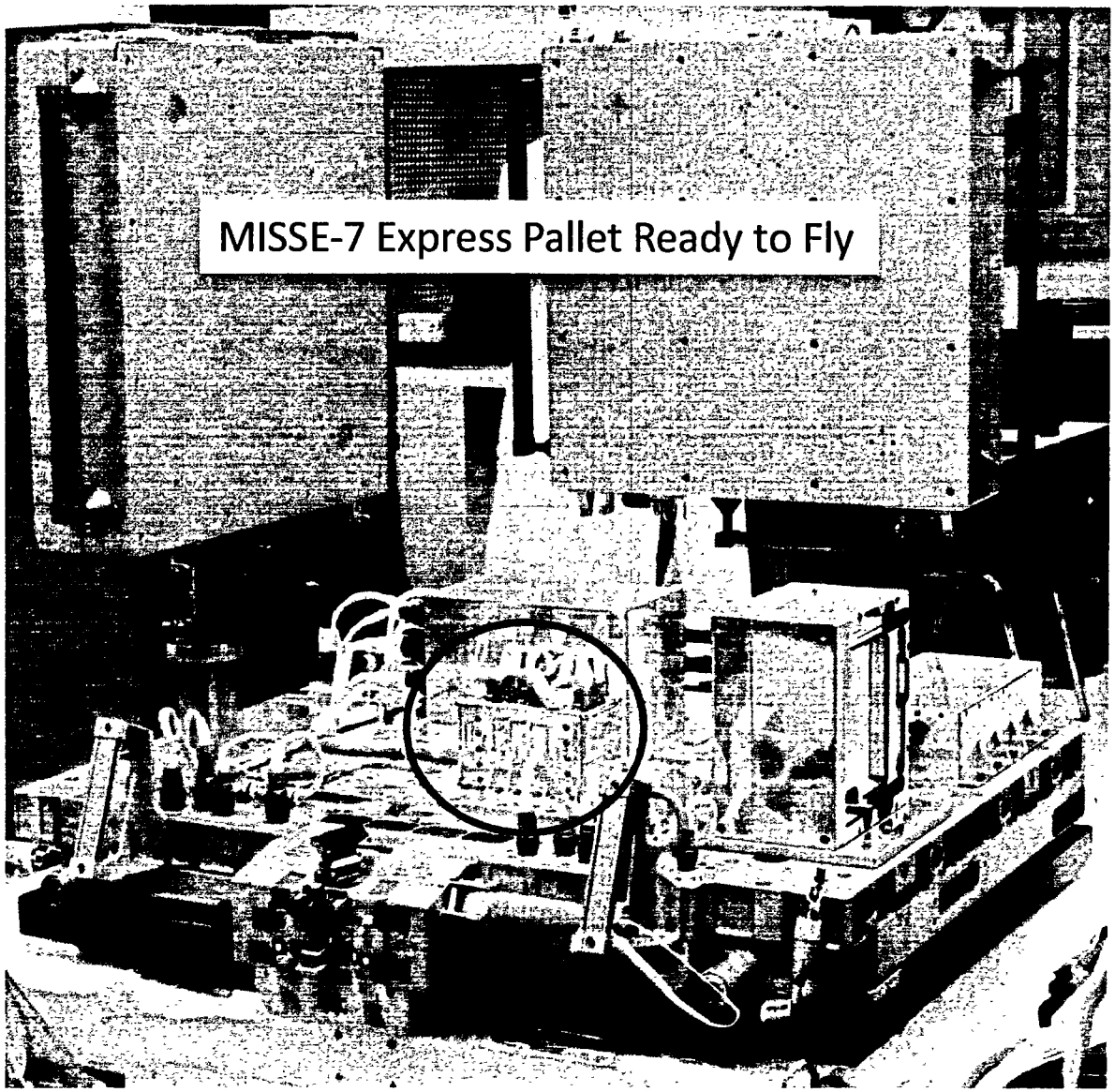
MISSE-7 SpaceCube

- Flight spare SpaceCube from HST SM4, STS-125
  - Re-engineered box for MISSE-7/ELC interface
  - Built adapter plate, custom harness, new software
  - Delivered box to NRL in 9 months!
- Test bed for radiation mitigation techniques
  - Start with "Radiation-Hardened by Software"
- Supports compressed file uploads
- Operations from a laptop

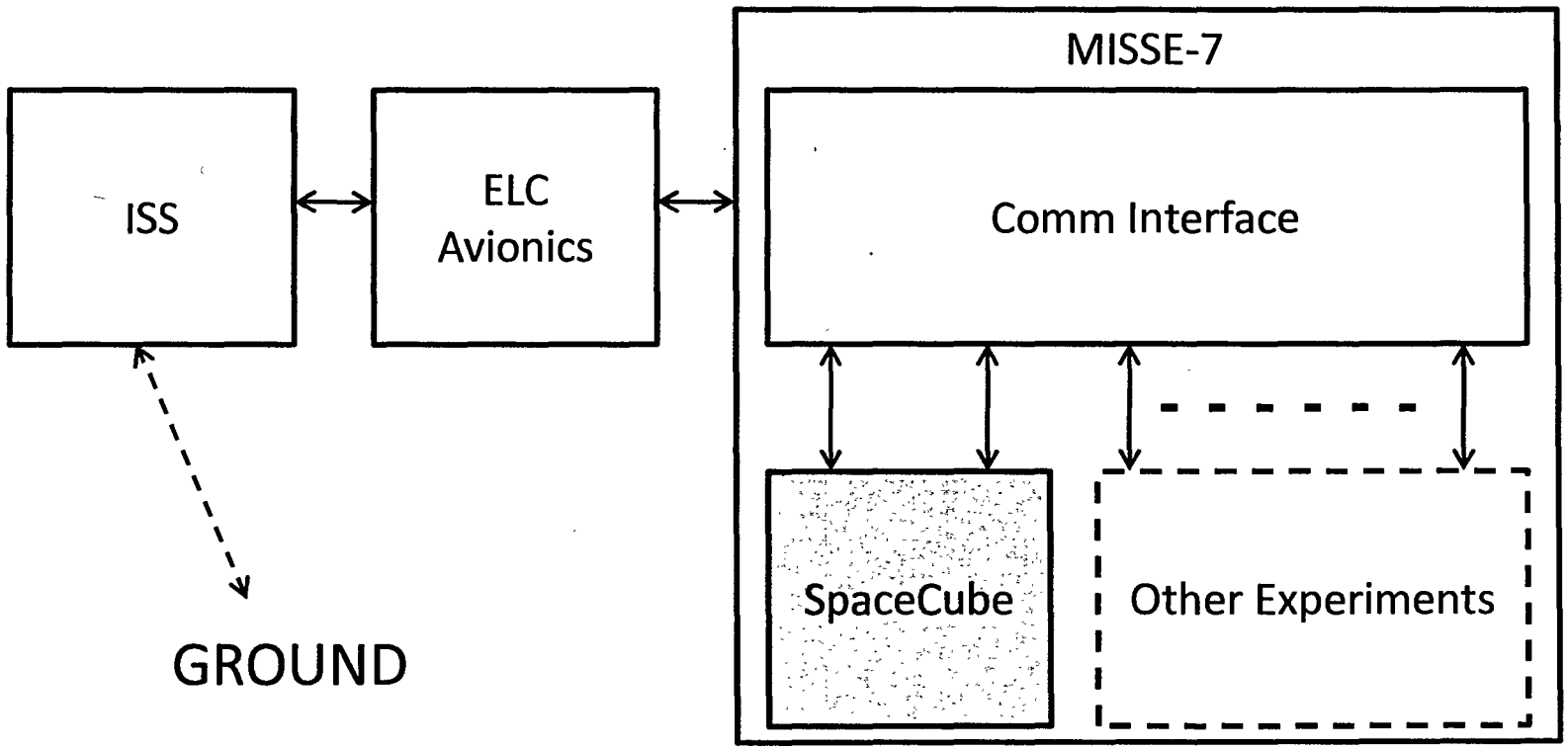
MISSE-7 SpaceCube



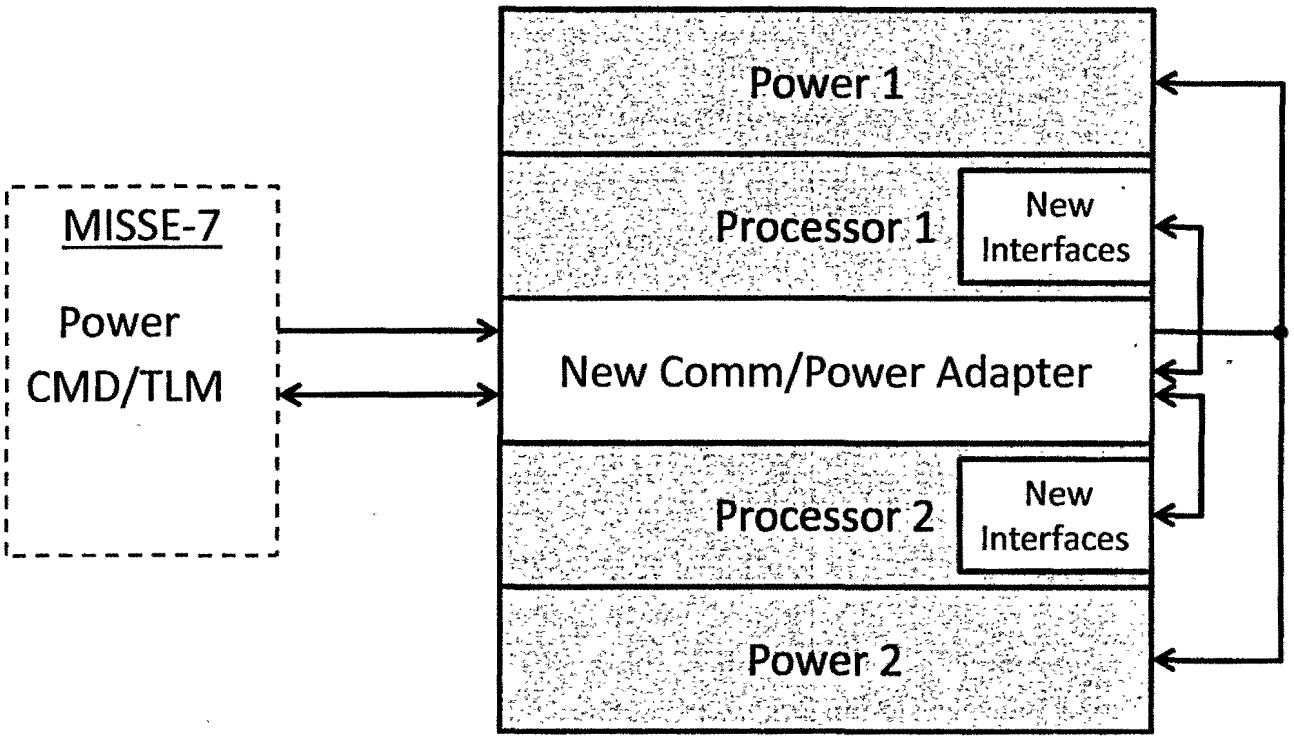
MISSE-7 SpaceCube



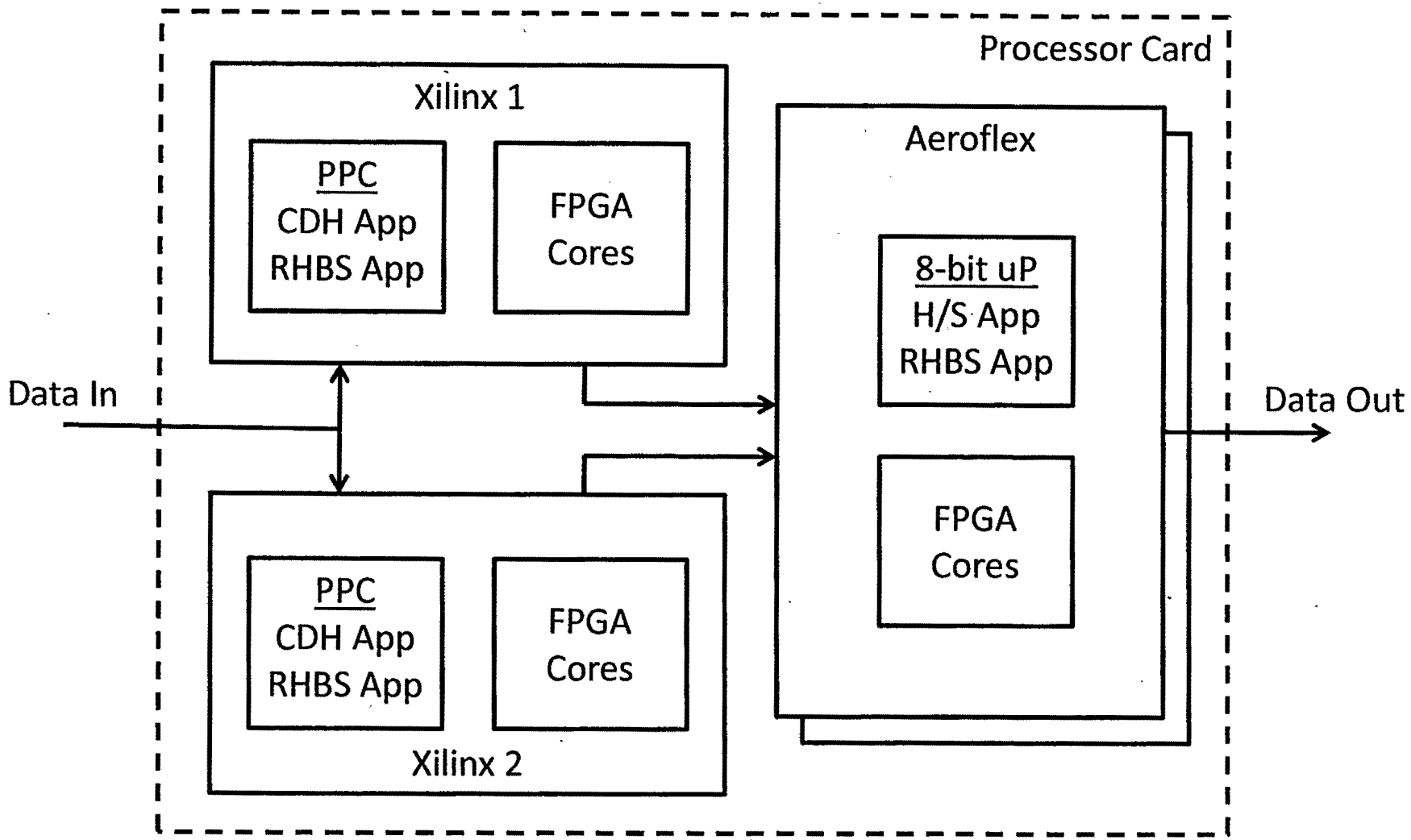
MISSE-7 SpaceCube Block Diagrams



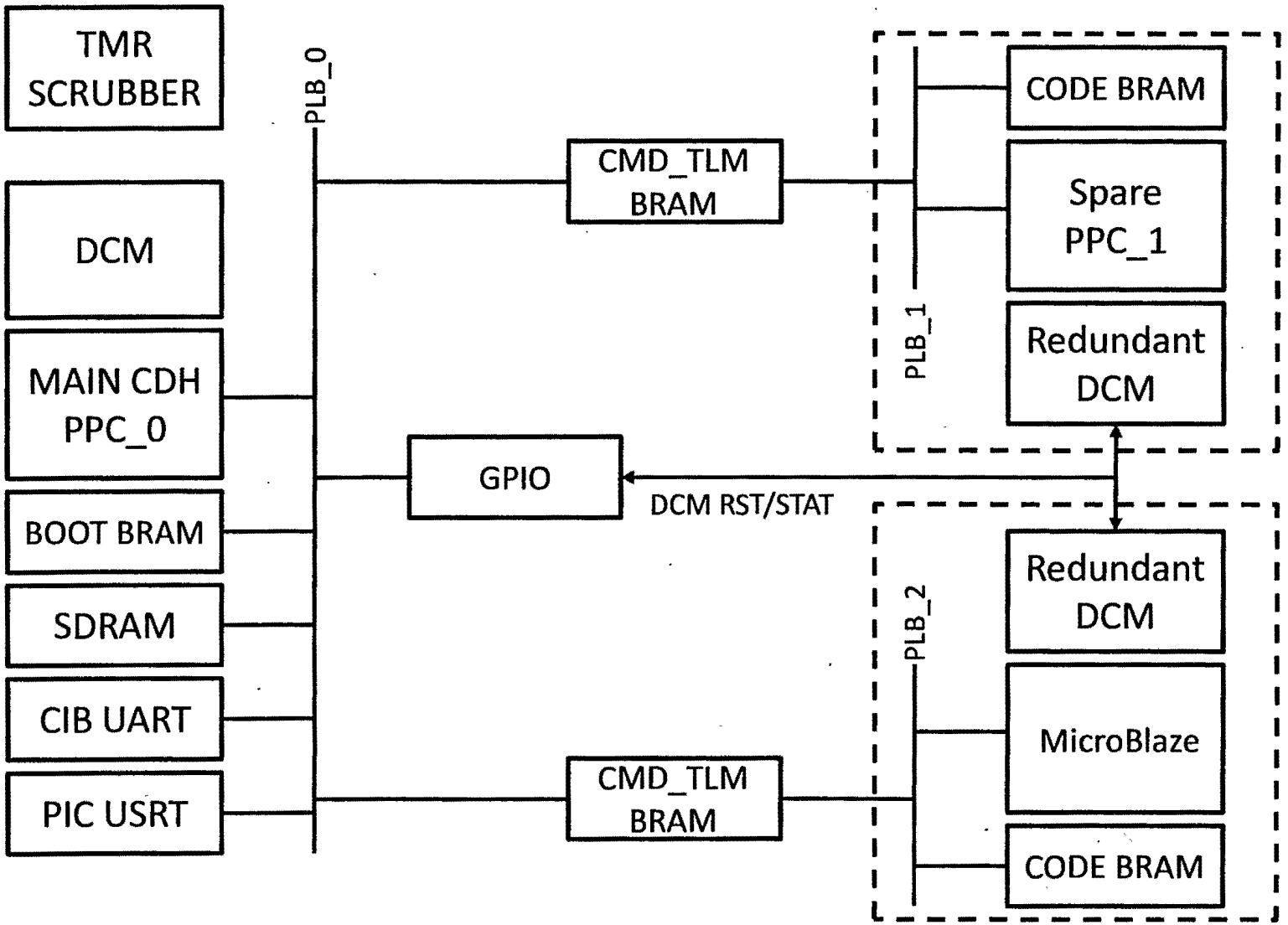
MISSE-7 SpaceCube Block Diagrams



MISSE-7 SpaceCube Block Diagrams



MISSE-7 SpaceCube Block Diagrams



MISSE-7 SpaceCube Future Work

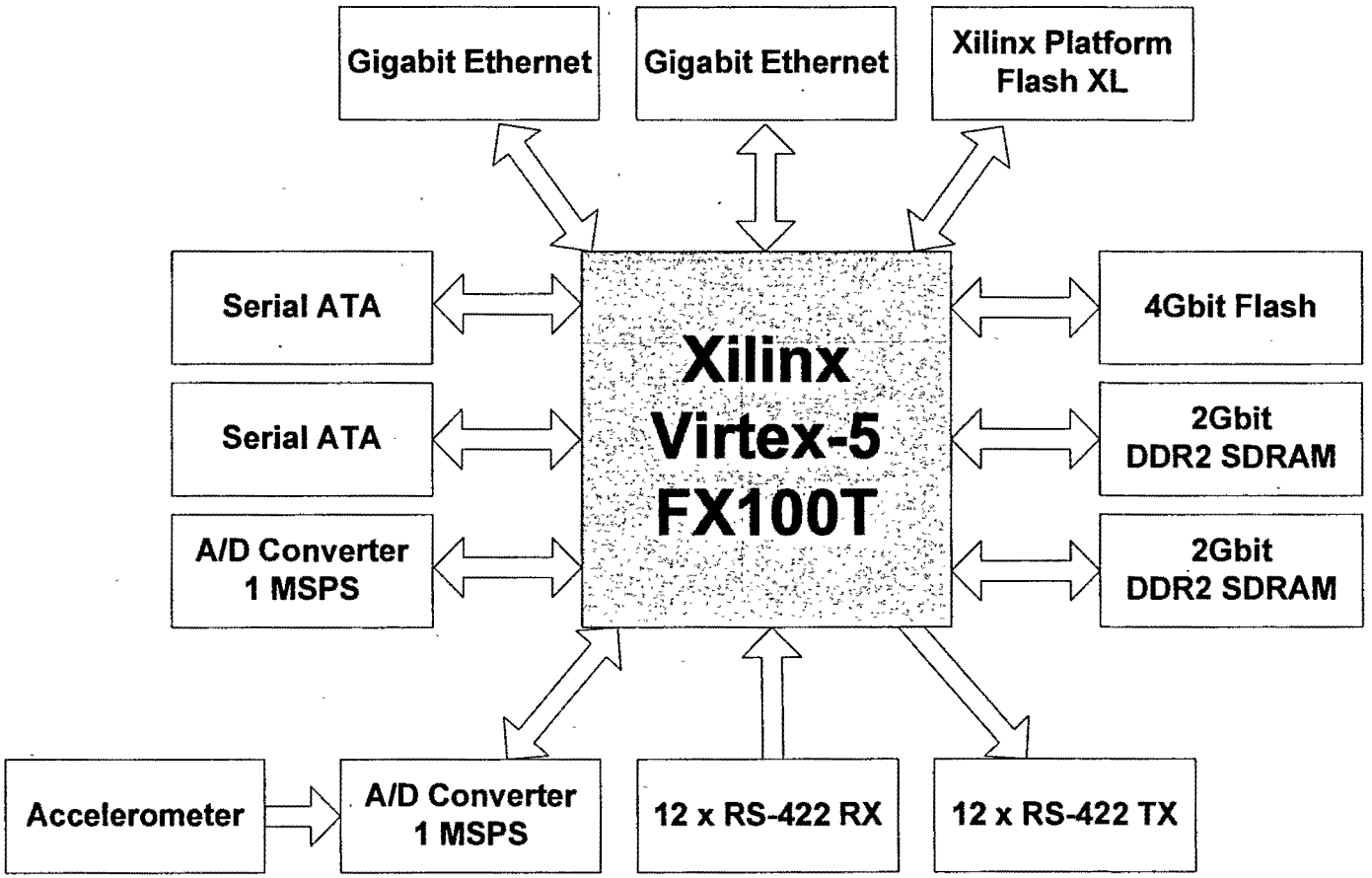
- Enjoy the Space Shuttle launch!!

- Conduct ops and analyze radiation data
- Improve RHBS algorithms and incorporate OS
- Collaboration with industry partners and universities
- Upload improved FPGA/SW designs

SpaceCube 1.5 Overview

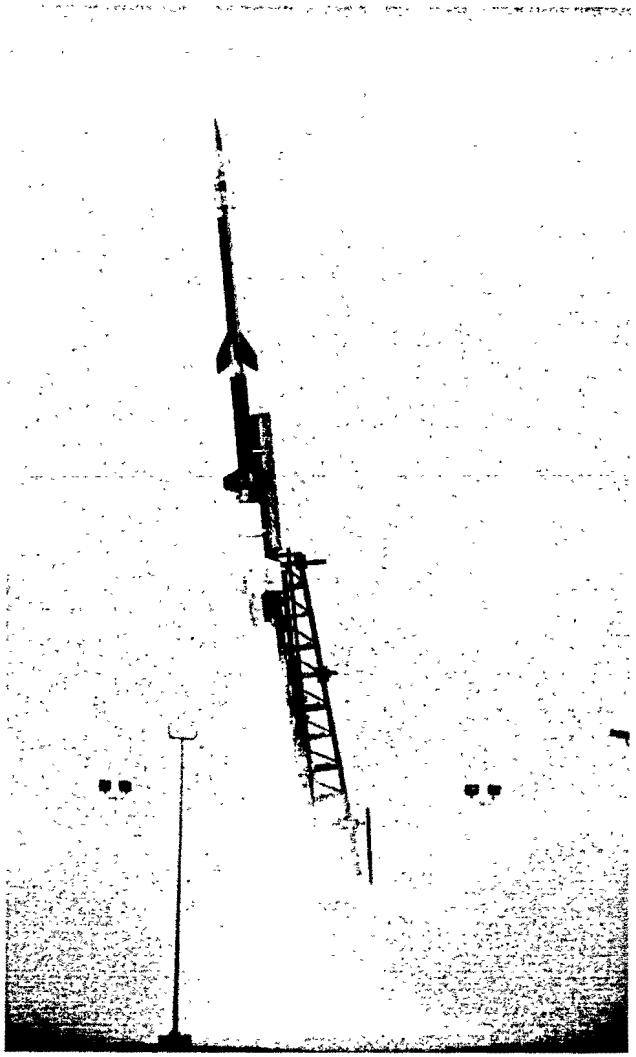
- SpaceCube 1.5 Processor Card
  - DoD **O**perationally **R**esponsive **S**pace (ORS) payload funding
  - COTS components
    - Targets small-scale missions such as sounding rockets
    - Short-duration flights
  - Features inherited from SpaceCube 1.0
    - 4" x 4" Form-Factor
    - Stackable Architecture
    - Legacy flight interfaces (RS-422/LVDS)
    - Power card compatibility
  - Bridge to SpaceCube 2.0
    - Transition to Xilinx Virtex-5 FPGA / PowerPC 440
    - "Plug and Play" Gigabit interfaces (SATA, Ethernet)
    - High-speed DDR2 SDRAM memories

SpaceCube 1.5: Processor Card

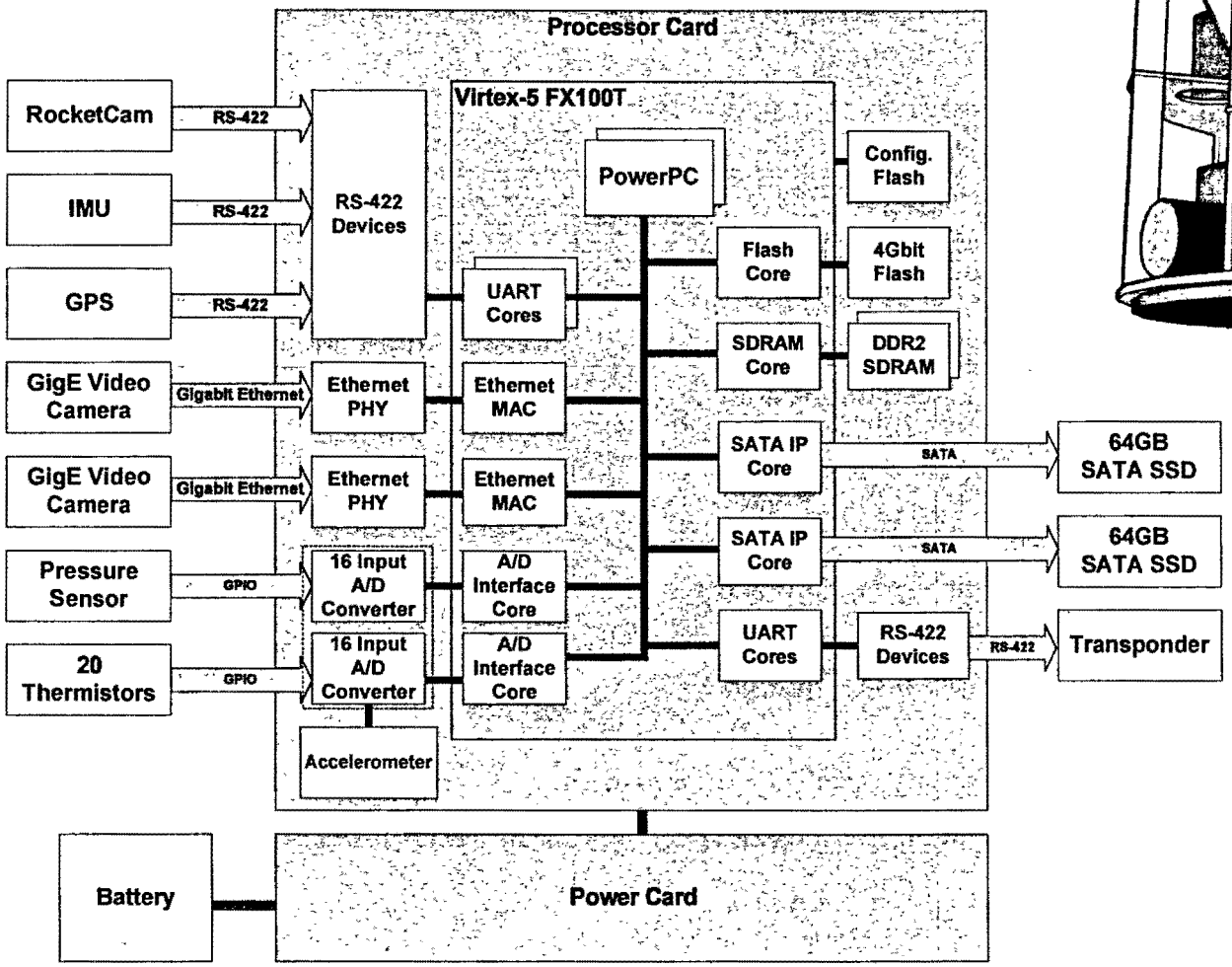


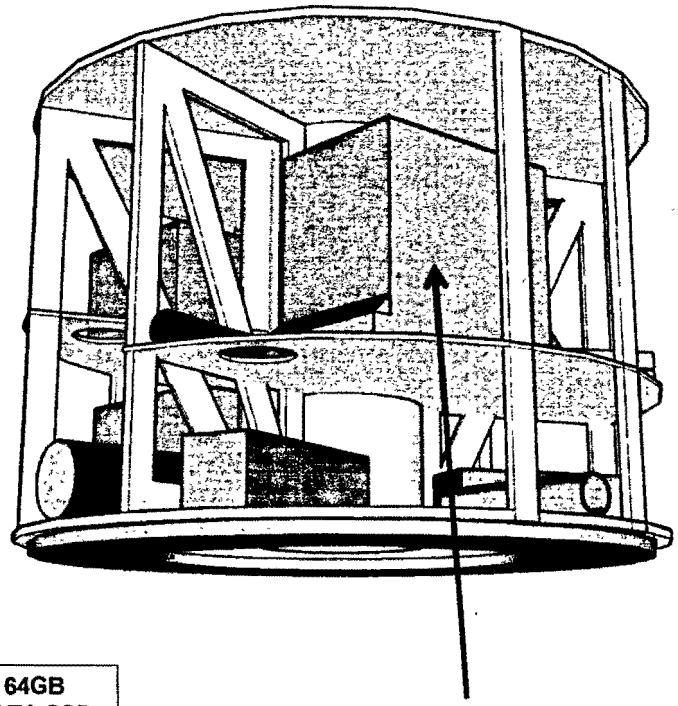
SpaceCube 1.5: SMART/ORS

- **Small Rocket/Spacecraft Technologies (SMART)**
  - Joint program between NASA and ORS
- Objectives
  - Develop faster, leaner, and more efficient approach to space flight
  - Maturation of miniaturized avionics for small launch vehicles, flight safety, and spacecraft applications
  - Reconfigurable payload structure for accommodating various subsystems
  - Demonstration of technologies applicable to future rocket balloon flights
- Series of sounding rocket flights
  - **First launch: Summer 2010** on a Terrier Improved-Orion sounding rocket
- Micro-satellite platform with **SpaceCube 1.5** as payload avionics
  - Ingest data from
    - RocketCam
    - 2 x GigE Industrial Cameras
    - Inertial Measurement Unit (IMU)
    - GPS
    - Sensors (pressure, thermal, acceleration)
  - Cameras validate interfaces and document flight and deployment of parachute
  - Record data telemetry on two commercial SATA Solid State Drives (SSD)
  - Downlink reduced telemetry through transponder (10Mb/s)



SMART System



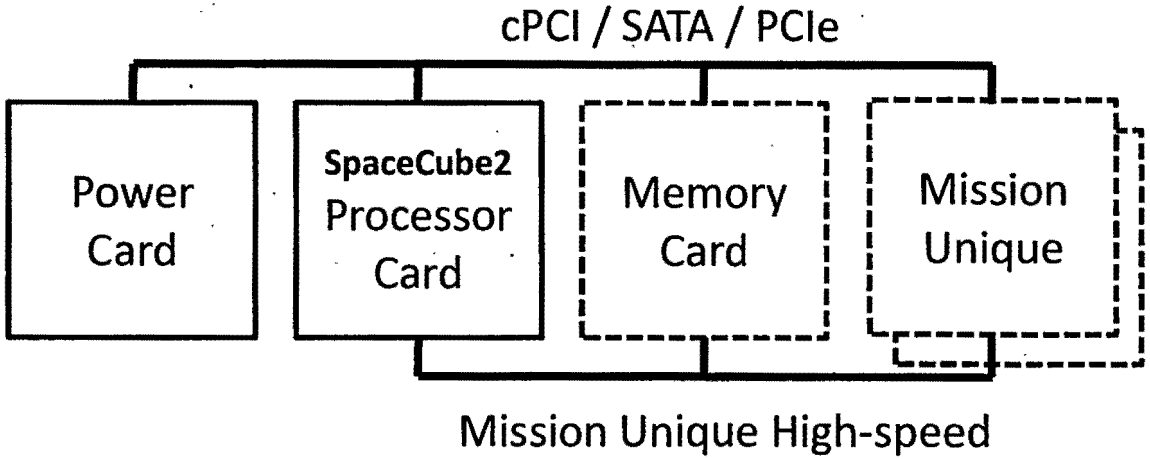


SpaceCube 1.5
in sounding rocket payload

SpaceCube 1.5: Status & Future Work

- Challenges:
  - Small Form Factor requires careful device selection and constrains I/O resources
  - Finding SATA solution (chose SATA IP Core)
- Improvements:
  - Compact/Rugged gigabit connectors capable of meeting **ALL** SATA specifications
- Status:
  - Completing schematic phase, initiating layout phase
  - FPGA/Software implementation of key interfaces proceeding on development boards

SpaceCube 2.0 Overview

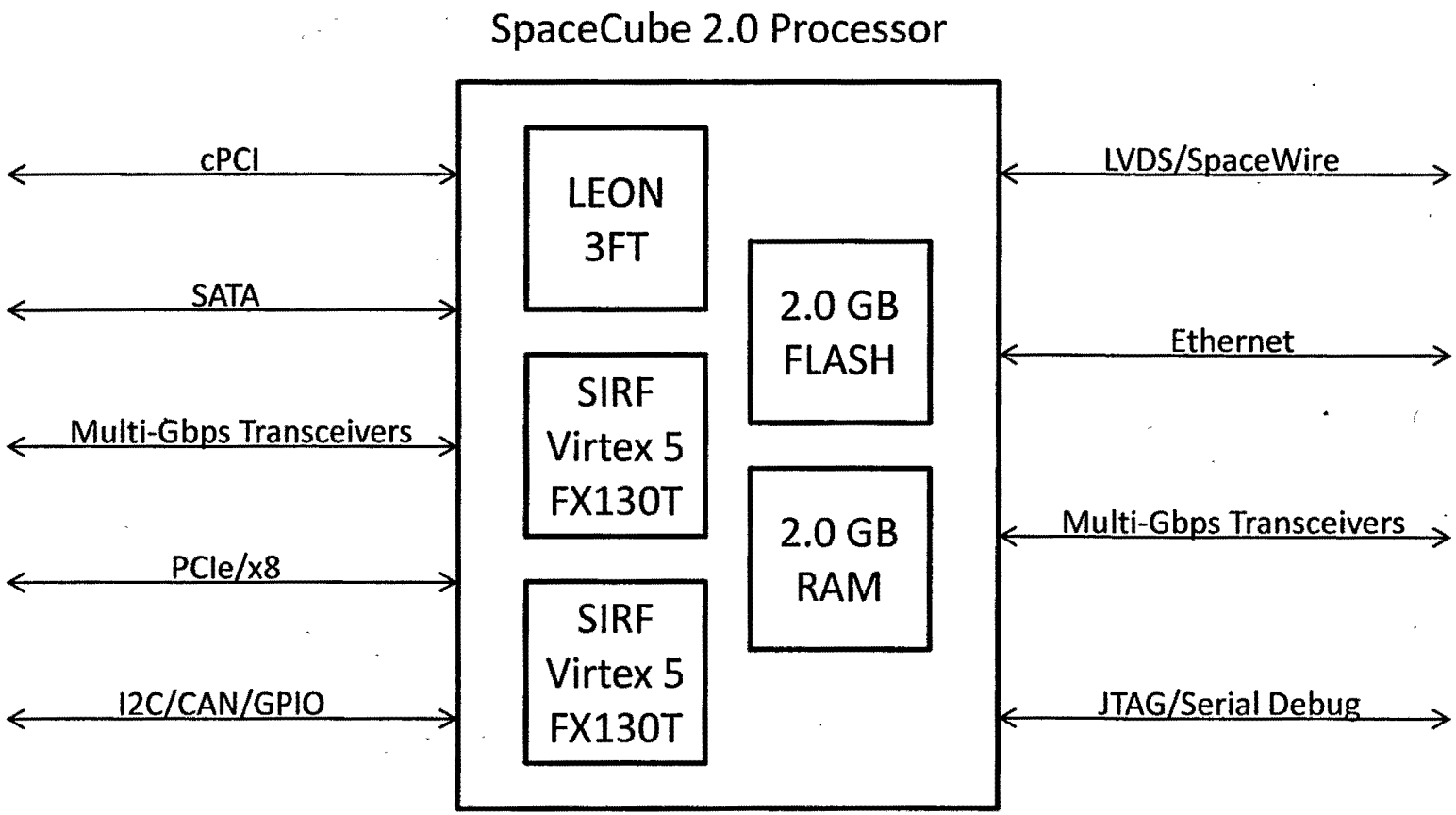


Flight Processor Comparison

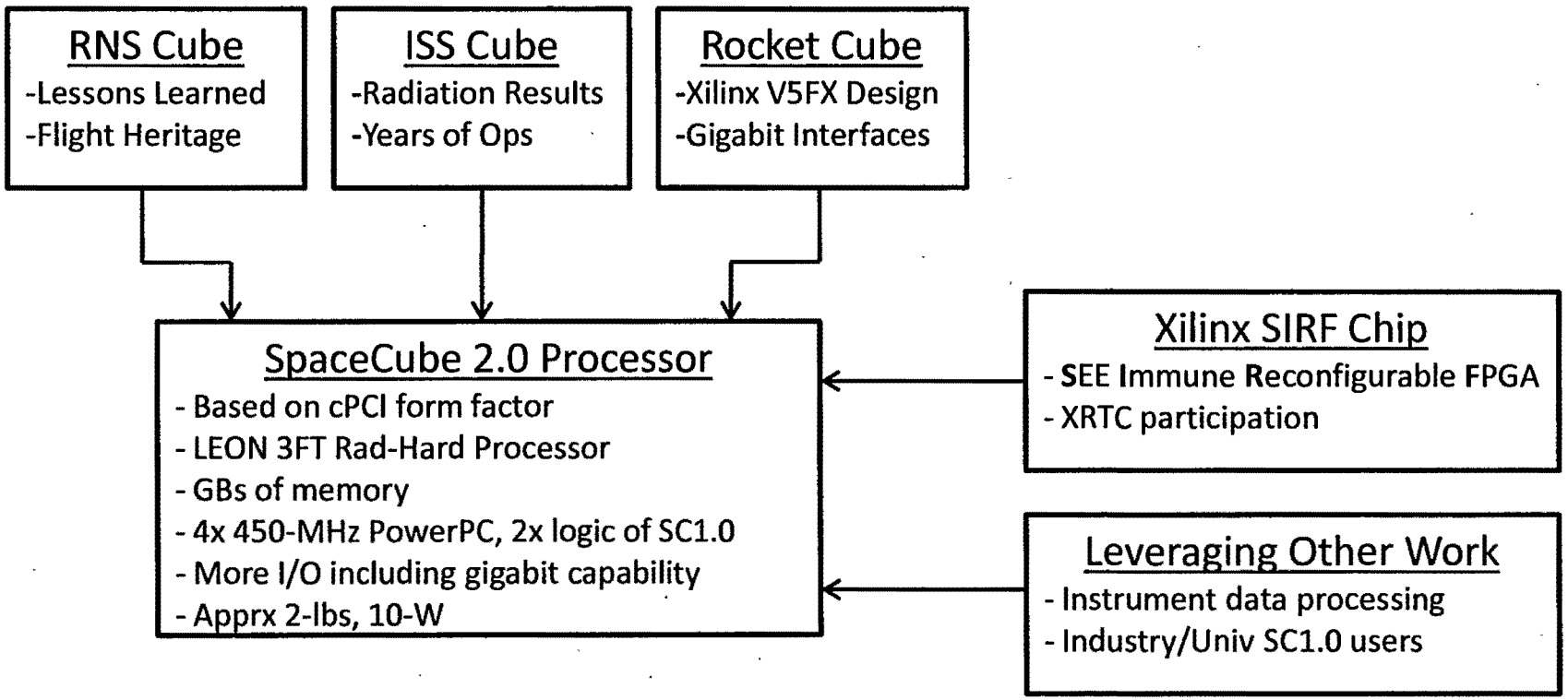
	MIPS	Cost	Power	MIPS/W
MIL-STD-1750A	3	-	15W	0.2
RAD6000	35	$250K	10-20W	2.33[1]
RAD750	< 500	$200K	10-20W	30[2]
SpaceCube 1.0	3000	$60K	5-15W	400[3]
SpaceCube 2.0	5000	$75K	10-20W	500[4]

Notes:
1 – typical, 35 MIPS at 15 watts
2 – typical, 450 MIPS at 15 watts
3 – 3000 MIPS at 7.5 watts (measured)
4 – 5000 MIPS at 10 watts (calculated)

SpaceCube 2.0 Processor Interfaces



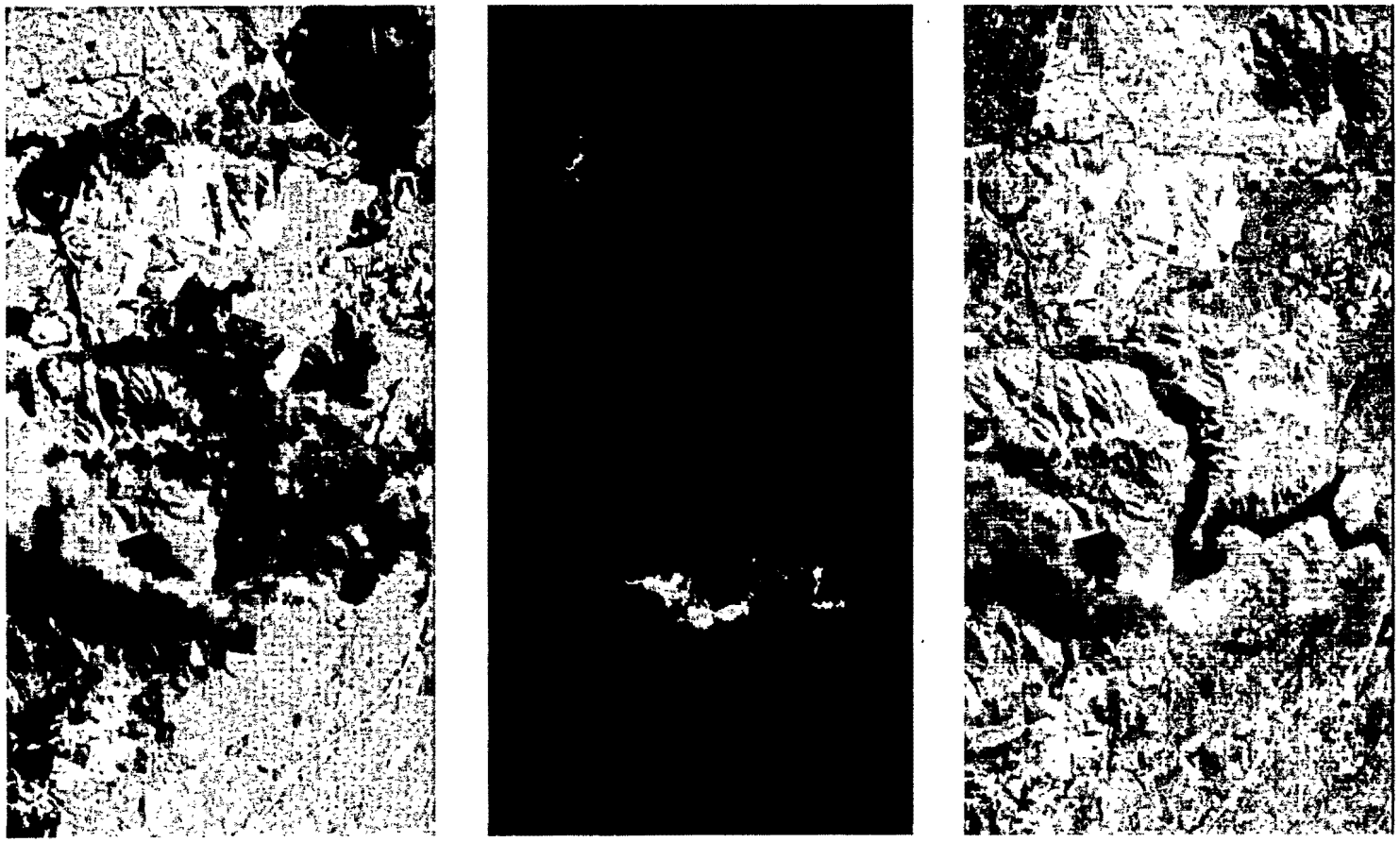
SpaceCube 2.0 Development Paths



Main Goals:

- Retain processing power of SpaceCube 1.0
- Add gigabit interfaces
- Improving overall reliability

SpaceCube On-Board Data Processing



On-Board HyperSpectral Data Processing IRAD --- Left: California Wildfire Scene, Center: On-Board Wildfire Detection and Temperature Characterization, Right: On-Board Product Generation for Direct Downlink to Emergency Services Personnel

Acronyms

- CDH: Command and Data Handling
- ELC: Express Logistics Carrier
- ESTO: Earth Science Technology Office
- FPGA: Field Programmable Gate Array
- IRAD: Internal Research and Design
- ISS: International Space Station
- MISSE: Materials ISS Experiment
- NRL: Naval Research Laboratory
- ORS: Operationally Responsive Space
- OS: Operating System
- PCI: Peripheral Component Interconnect
- PPC: PowerPC
- RHBS: Radiation-Hardened By Software
- RNS: Relative Navigation Sensors
- SATA: Serial Advanced Technology Attachment
- SEE: Single Event Effect
- TMR: Triple Module Redundancy