SEU Analysis of Complex Circuits Implemented in Actel RTAX-S FPGA Devices

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Place, Route, and Gate Utilization are Stored in the FPGA Configuration

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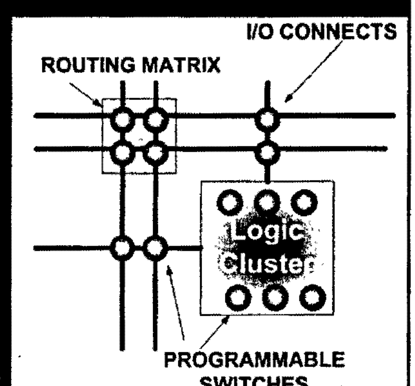
Configuration Defines:

- *Functionality (logic cluster)*
- *Connectivity (routes)*
- *Placement*



Configuration Switch Types:

- *Antifuse: One time Programmable (OTP)*
- *SRAM: Reprogrammable (RP)*
- *Flash: Reprogrammable (RP)*

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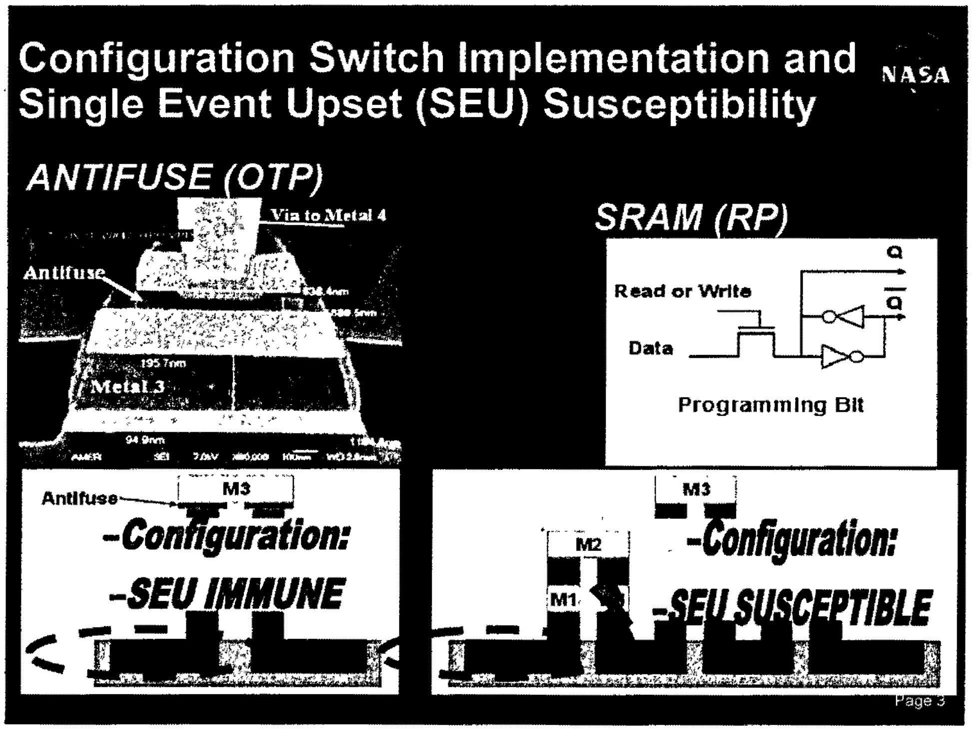

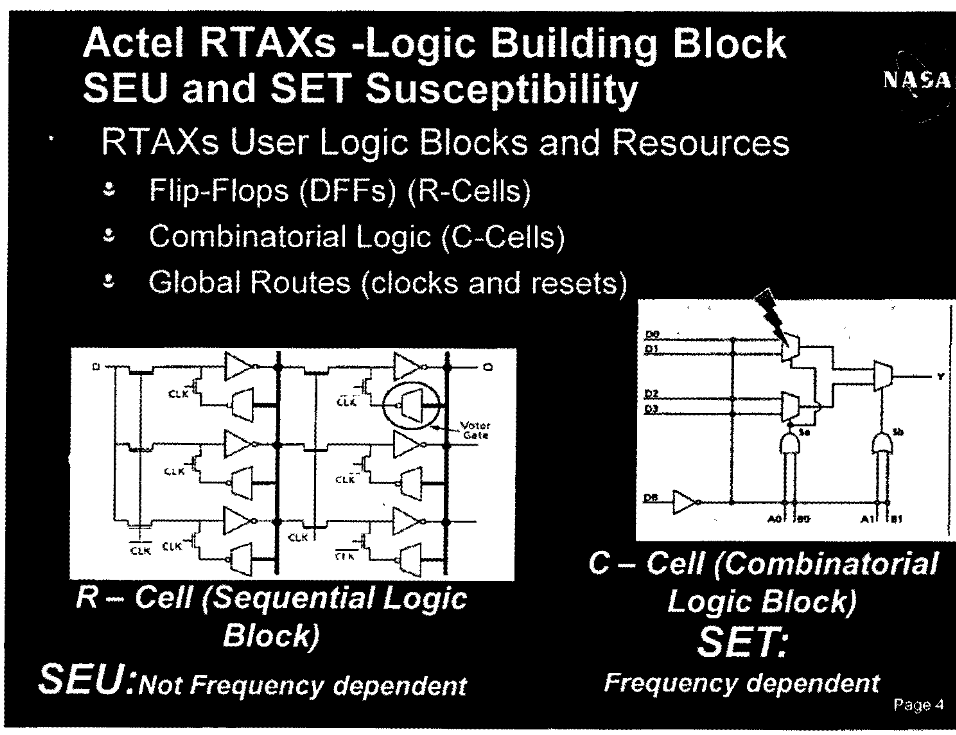

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Actel RTAXs Susceptibility and Mitigation

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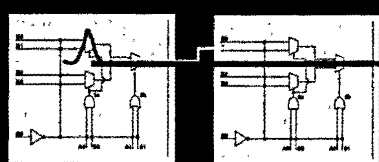
Design Specific SEE upset rate

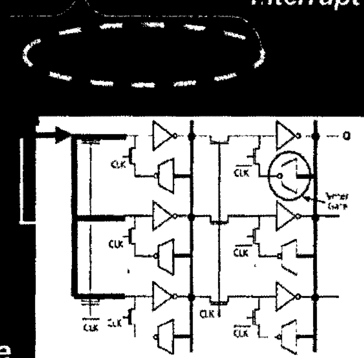
Configuration SEE upset rate

Functional logic SEE upset rate

Single Event functional Interrupt



Combinatorial logic cells



Triple DFFs lower P_{DFFSEU} but can not mitigate $P(fs)_{SET \rightarrow SEU}$ (upset rate in Frequency Dependent)

DFF

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FPGA Design Under Test Development

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- Repeatability ... increase statistics

Traditional FPGA Testing

- Stress and expose building blocks
- Divide and conquer...Determine separate error cross sections that correspond to specific:
  - Frequencies
  - Designs and Building blocks (when applicable)
- Fault Isolation...Create designs that will facilitate error differentiation

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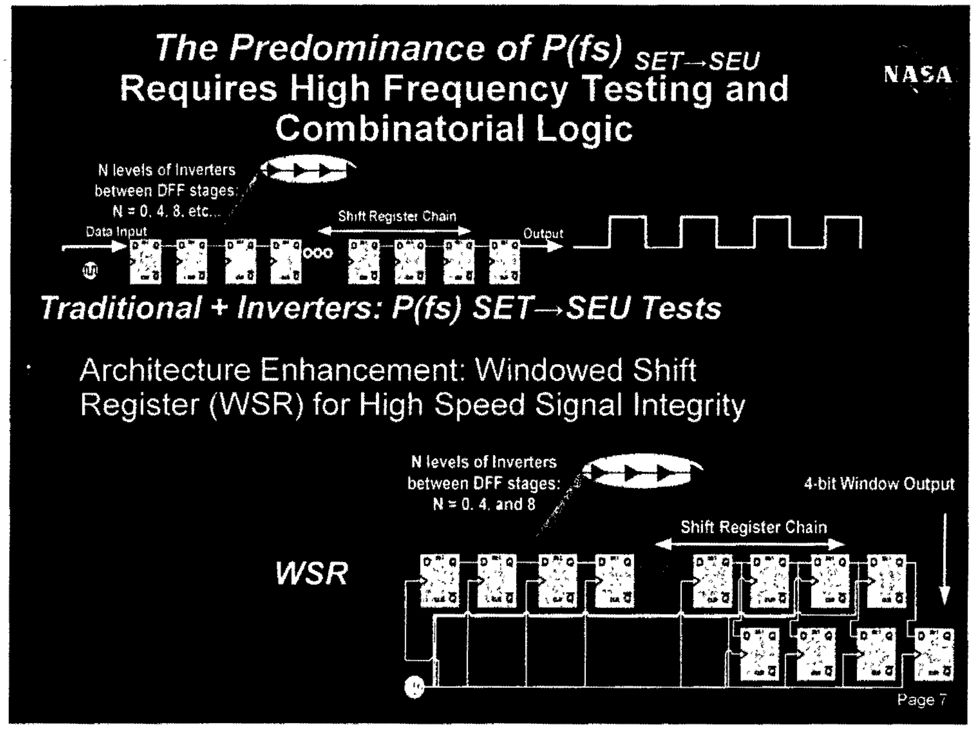
The Predominance of P(fs) SET→SEU
Requires High Frequency Testing and
Combinatorial Logic
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N levels of Inverters
between DFF stages:
N = 0, 4, 8, etc...
Data Input
Shift Register Chain
Output
Traditional + Inverters: P(fs) SET→SEU Tests
Architecture Enhancement: Windowed Shift Register (WSR) for High Speed Signal Integrity
N levels of Inverters
between DFF stages:
N = 0, 4, and 8
4-bit Window Output
Shift Register Chain
WSR
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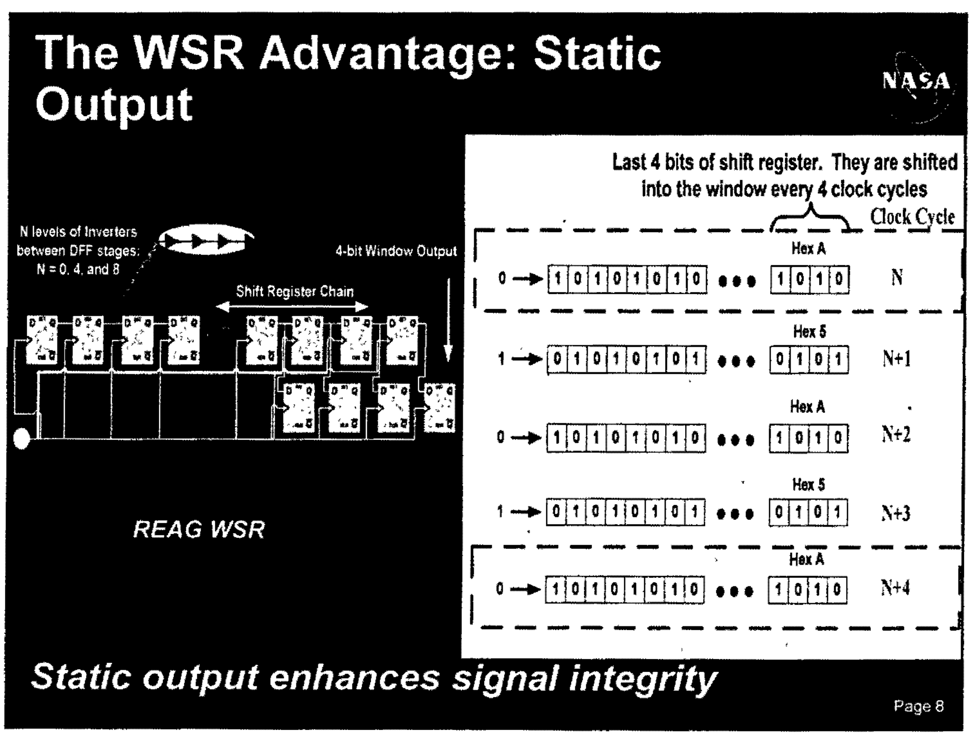
The WSR Advantage: Static Output
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N levels of Inverters
between DFF stages:
N = 0, 4, and 8
4-bit Window Output
Shift Register Chain
REAG WSR
Last 4 bits of shift register. They are shifted into the window every 4 clock cycles
Clock Cycle
Hex A
0 → 1 0 1 0 1 0 1 0 ••• 1 0 1 0 N
Hex 5
1 → 0 1 0 1 0 1 0 1 ••• 0 1 0 1 N+1
Hex A
0 → 1 0 1 0 1 0 1 0 ••• 1 0 1 0 N+2
Hex 5
1 → 0 1 0 1 0 1 0 1 ••• 0 1 0 1 N+3
Hex A
0 → 1 0 1 0 1 0 1 0 ••• 1 0 1 0 N+4
Static output enhances signal integrity
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Highlights/Accomplishments: REAG WSR SEE Results

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- Error rates are significantly dependent on Threshold LET(LET_{th})
- Choice of design impacted LET_{th} … number of C-Cells between DFFs
- Choice of data pattern and frequency of operation impacted LET_{th} (>2 orders of magnitude)

	Low Frequency	Increased Frequency
LET_{th} MeV*cm²/mg	$LET_{th} > 37$	$8 < LET_{th} < 30$
Bit Error Rate (errors/bit-day)	$dE_{bit}/dt \approx 1\times10^{-10}$	$1\times10^{-10} < dE_{bit}/dt < 5\times10^{-8}$

If Frequency or data pattern were not varied during testing, then an incorrect LET_{th} and dE_{bit}/dt would had been calculated

Considerations when Developing a Complex Design under Test Architecture

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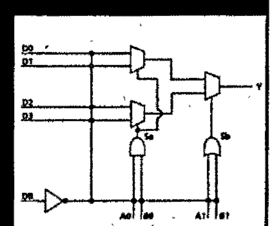

- Are inverters efficient test structures?
- Want to investigate something more realistic than a shift register
  - It should have the characteristics of a complex design with:
    - fan-out and fan-in > 1
    - contains a mixture of sequential and combinatorial logic.
  - The circuit should be replicated to increase statistics.
  - Its state space can be traversed within relatively short time periods such that all states are equally likely to be subject to particle strikes during radiation testing.

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Counters Meet Requirements

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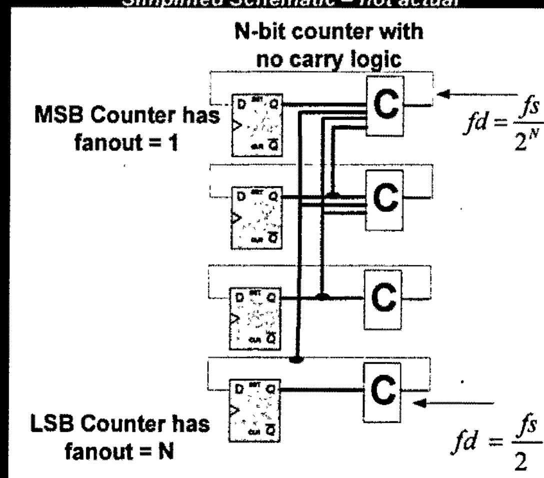
- Has characteristics of a complex design with:
  - fan-out and fan-in > 1
  - contains a mixture of sequential and combinatorial logic.
- Variety of data pattern frequencies (f_d)
- State space Traversal = $2^N/f_s$

Simplified Schematic – not actual



fd: data pattern frequency
fs = system frequency

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Highlights/Accomplishments:
Texas A&M Heavy Ion Results Counters versus WSRs

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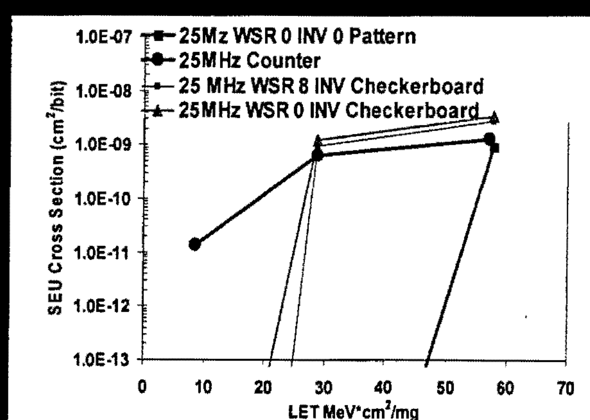

*25MHz Counter LETth is lower than 25MHz WSR but similar to 100MHz CB WSRs (also has a LET_{th} = 8.6MeV*cm²/mg)*

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Summary

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- Because configuration, global routes, and configuration is hardened in the RTAXs device, $P_{SET \rightarrow SEU}$ becomes the most significant source of upsets in radiation environments
- The ratio of combinatorial logic delay to clock frequency within a data path will drive $P_{SET \rightarrow SEU}$.
- Hence, Choice of Architecture and frequency can significantly affect SEE cross section and bit error rate RTAXs characterization
- Counter Arrays were driven near their top speed while containing several combinatorial logic levels. Subsequently they produced the lowest LETth→Highest bit error rate versus the shift register designs

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Summary: REAG Evolution of FPGA Designs Under Test

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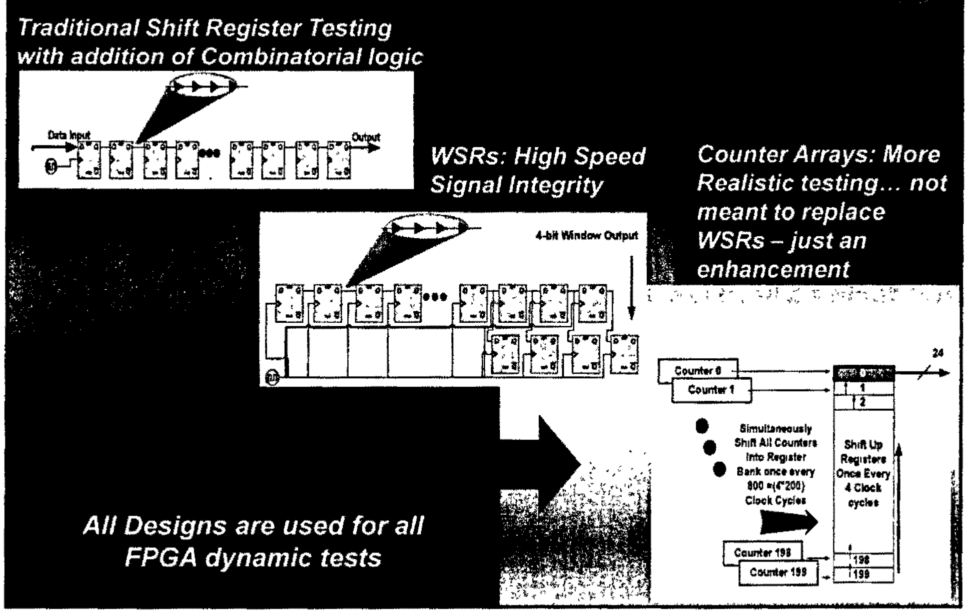

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