Complexity Management and Design Optimization Regarding a Variety of Triple Modular Redundancy Schemes through Automation

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Agenda

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- **Section I:** Single Event Effects in Digital Logic
- **Section II:** FPGA Basics – Architectural Differences
- **Section III:** Reducing System Error: Common Mitigation Techniques
  - Triple Modular Redundancy:
    - Block Triple Modular Redundancy (BTMR)
    - Local Triple Modular Redundancy (LTMR)
    - Global Triple Modular Redundancy (GTMR)
- **Section IV:** The Automation Process

To be presented by Melanie Berg at the Mid-Atlantic Region Local Users Group (MARLUG) Meeting at Applied Physics Lab, Laurel, Maryland, May 26, 2010.

Section I: Single Event Effects in Digital Logic

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Source of Faults: SEEs and Ionizing Particles

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- Single Event Effects (SEEs)
  - Terrestrial devices are susceptible to faults mostly due to:
    - **alpha particles**: from packaging and doping and
    - **Neutrons**: caused by Galactic Cosmic Ray (GCR) Interactions that enter into the earth's atmosphere.
  - Devices expected to operate at higher altitude (Aerospace and Military) are more prone to upsets caused by:
    - **Heavy ions**: direct ionization
    - **Protons**: secondary effects

Energy emitted from an atom or nucleus in the form of waves or particles

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Device Penetration of Heavy Ions and Linear Energy Transfer (LET)

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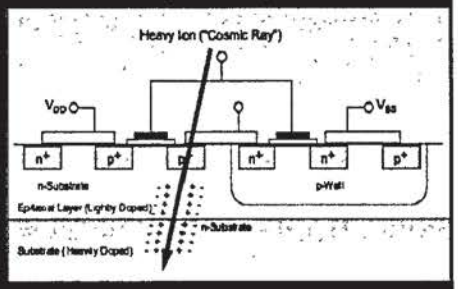
- LET characterizes the deposition of charged particles
- Based on Average energy loss per unit path length (stopping power)
- Mass is used to normalize LET to the target material



Average energy deposited per unit path length

$$\frac{MeV}{mg/cm^2}$$

Units

Density of target material

LET vs. Error Cross Section Graph

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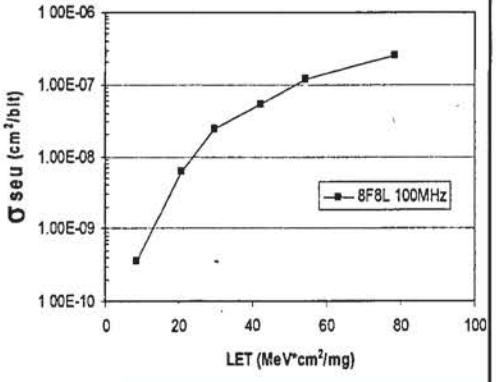
Error Cross Sections are calculated per LET value in order to characterize the number of potential faults and error rates in the space environment

Terminology:

- Flux: Particles/(sec-cm^2)
- Fluence: Particles/cm^2
- Error cross section(σ): #errors normalized by fluence
- Error cross section is calculated at several LET values (particle spectrum)

LET vs. σ:

$$\sigma_{seu} = \frac{\#errors}{fluence}$$



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Single Event Faults and Common Terminology

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- Single Event Latch Up (**SEL**): Device latches in high current state
- Single Event Burnout (**SEB**): Device draws high current and burns out
- Single Event Gate Rupture: (**SEGR**): Gate destroyed typically in power MOSFETs
- **Single Event Transient** (SET): current spike due to ionization. Dissipates through bulk
- **Single Event Upset** (SEU): transient is caught by a memory element
- **Single Event Functional Interrupt** (SEFI) - upset disrupts function

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Radiation Induced Fault Generation

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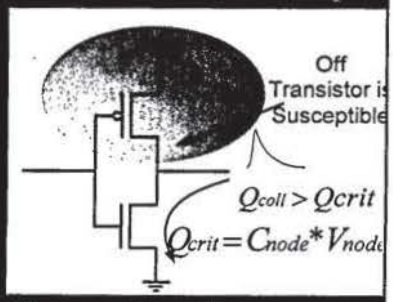
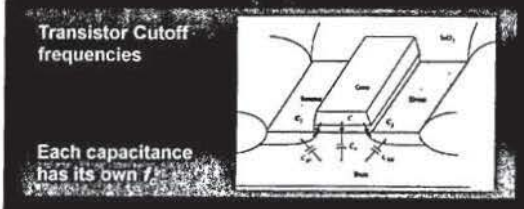
- (SET)s can develop in combinatorial logic
- SETs can vary in pulse width (T_{pulse}) and amplitude.



- Geometry of Transistors
- Loading of Transistors
- Length of Routes
- Switching Rates



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Single Event Effects (SEEs) and IC System Error

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- **SEUs or SETs can occur in:**
  - Combinatorial Logic (including global routes)
  - Sequential Logic
  - Memory Cells
- Depending on the Device and the design, each fault type will:
  - Have a probability of occurrence
  - Either have a significant or insignificant contribution to system error

Every Device has different Error Responses… We must understand the differences and design appropriately

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Section II: FPGA Basics – Architectural Differences

Configuration… Only FPGAs

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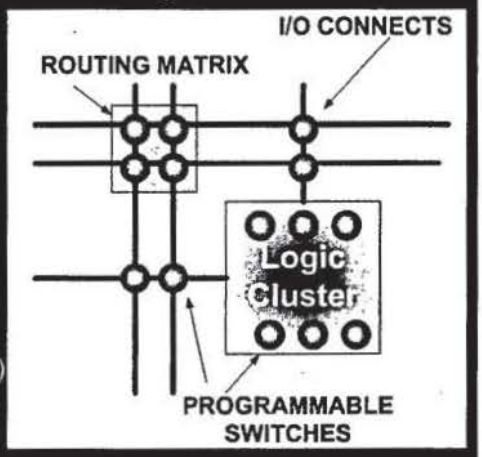
HDL → **FPGA MAPPING** → **Configuration**

- **Configuration Defines:** Arrangement of pre-existing logic via programmable switches
  - Functionality (logic cluster)
  - Connectivity (routes)
- Programming Switch Types:
  - **Antifuse:** One time Programmable (OTP)
  - **SRAM:** Reprogrammable (RP)
  - **Flash:** Reprogrammable (RP)



Combinatorial Logic Blocks and Potential Upsets… SETs in ASICs and Anti-fuse FPGAs

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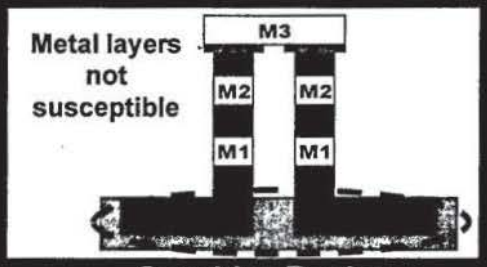
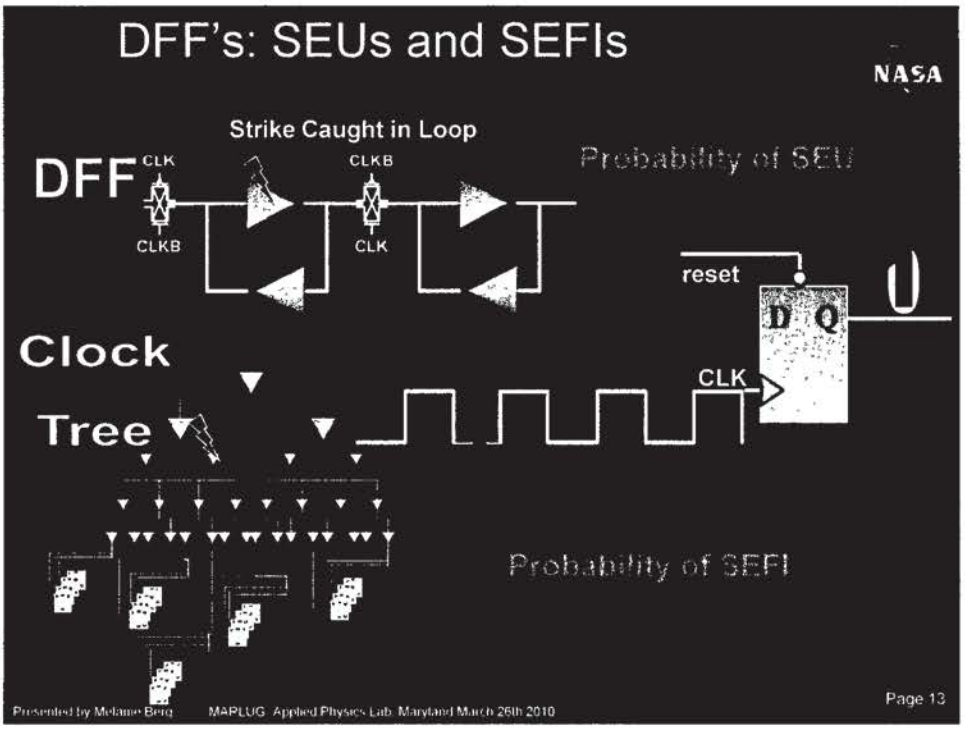


Sensitive Region

Glitch = Transient


DFF's: SEUs and SEFIs
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Strike Caught in Loop
DFF
CLK
CLKB
CLKB
CLK
Probability of SEU
reset
D Q
U
CLK
Clock
Tree
Probability of SEFI
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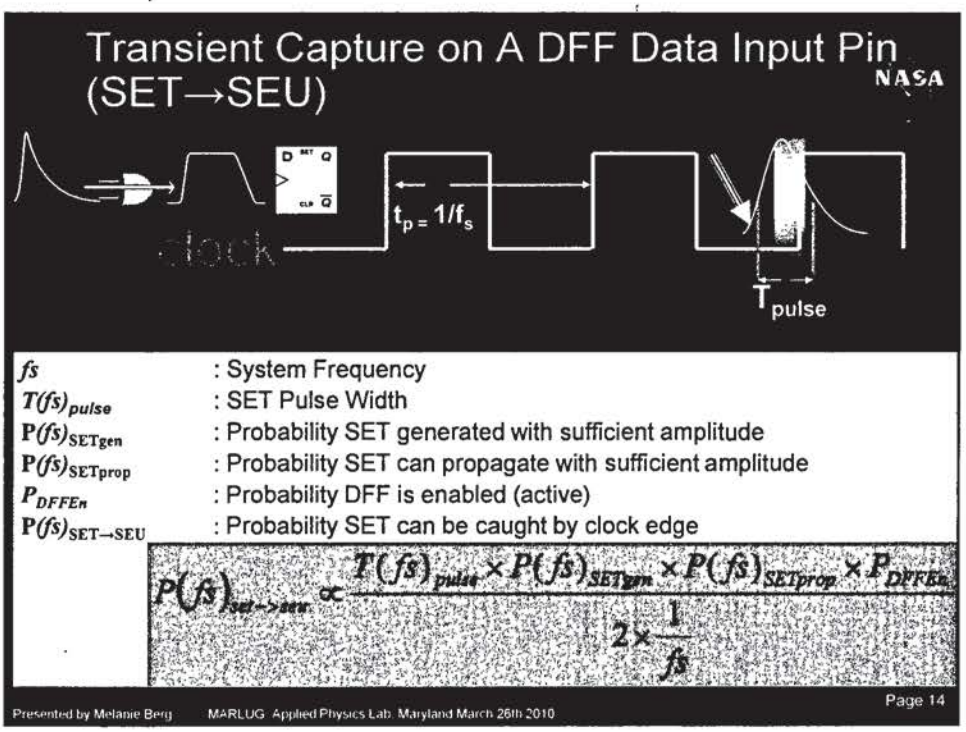
Transient Capture on A DFF Data Input Pin (SET→SEU)
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D SET Q
CLR Q
clock
$t_p = 1/f_s$
T_{pulse}
fs : System Frequency
$T(fs)_{pulse}$: SET Pulse Width
$P(fs)_{SETgen}$: Probability SET generated with sufficient amplitude
$P(fs)_{SETprop}$: Probability SET can propagate with sufficient amplitude
P_{DFFEn} : Probability DFF is enabled (active)
$P(fs)_{SET\rightarrow SEU}$: Probability SET can be caught by clock edge
$P(fs)_{set->seu} \propto \frac{T(fs)_{pulse} \times P(fs)_{SETgen} \times P(fs)_{SETprop} \times P_{DFFEn}}{2 \times \frac{1}{fs}}$
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Summary: Most Significant Factors of System Error Probability $P(fs)_{error}$

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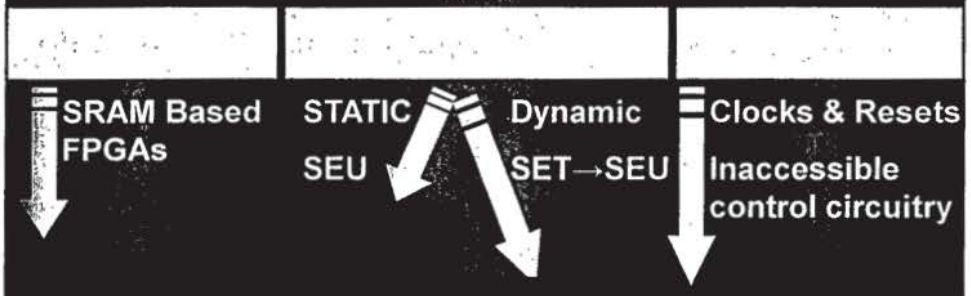

Antifuse FPGA Devices

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- Currently the most widely employed FPGA Devices within space applications
- Configuration is hardened due to fuse based technology (Metal to Metal)
- Localized (@ DFF node) Mitigation (TMR or DICE) is employed
- Clock and Reset lines are hardened

ACTEL RTAX-S Architecture Basics

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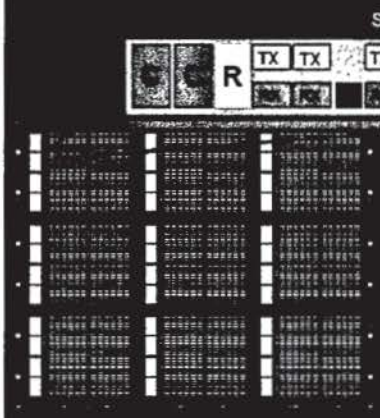

Super Cluster:
- **Combinatorial Cells: C CELLS**
- **DFF Cells: R Cells**

Source: RTAX-S/SL RadTolerant FPGAs 2009 Actel.com

ACTEL RTAX-S Combinatorial and Sequential Logic

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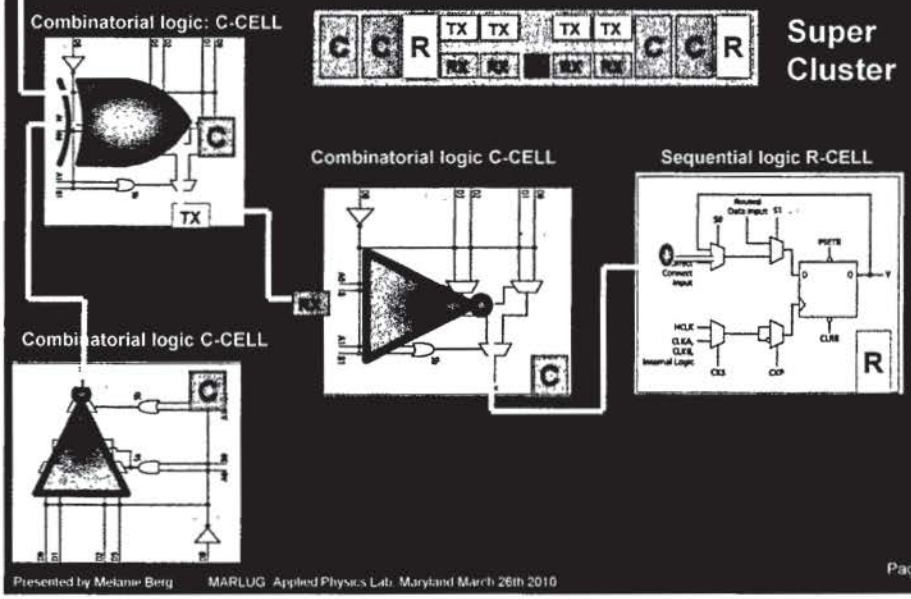

General Xilinx Virtex 4 FPGA Architecture: SRAM Based Configuration

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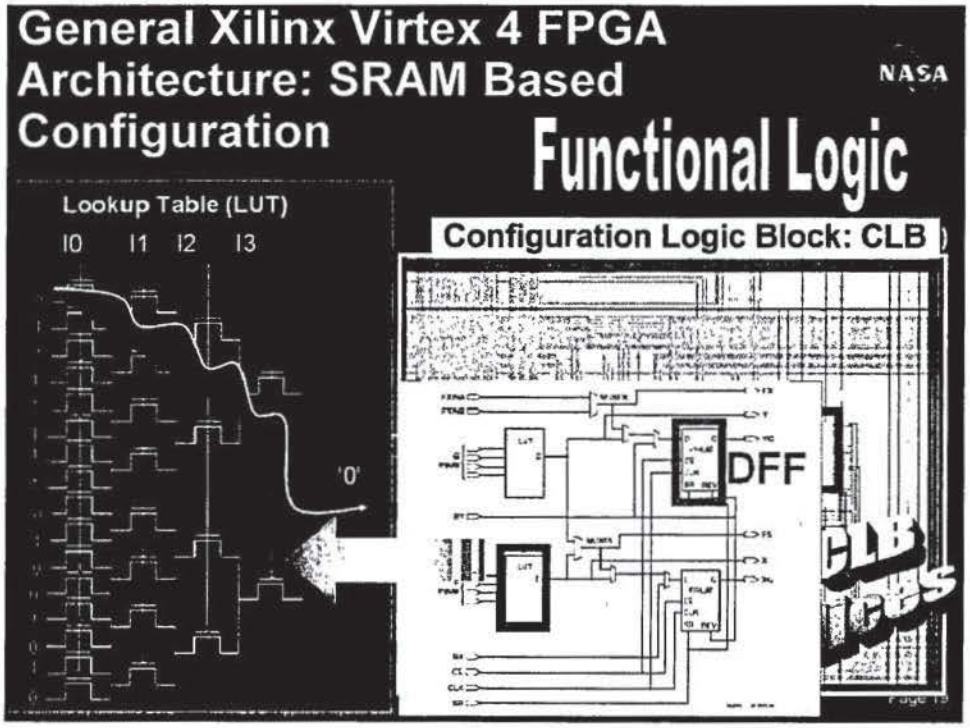

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Section III: Reducing System Error: Common Mitigation Techniques

- Triple Modular Redundancy:
  - Block Triple Modular Redundancy (BTMR)
  - Local Triple Modular Redundancy (LTMR)
  - Global Triple Modular Redundancy (GTMR)
  - Distributed Triple Modular Redundancy (DTMR)

Mitigation

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- Error Correction or Error avoidance
- Mitigation can be:
  - **Embedded**: built into the device library cells
    - User does not verify the mitigation – manufacturer does
  - **User inserted**: part of the actual design process
    - User must verify mitigation… Complexity is a RISK!!!!!!!!
- Mitigation should reduce error…
  - Generally through redundancy
  - Incorrect implementation can increase error

Want to reduce as many terms as possible:

Example: TMR Mitigation Schemes will use Majority Voting

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I0	I1	I2	Majority Voter
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Best 2 out of 3

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Reducing System Error: Common Mitigation Techniques

- Triple Modular Redundancy:
  - Block Triple Modular Redundancy (BTMR)
  -
  -
  -

BTMR

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- Need Feedback to Correct
- Generally can not apply internal correction from voted outputs
- Errors can accumulate – not an effective technique

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Reducing System Error: Common Mitigation Techniques

- Triple Modular Redundancy:
  -
  - Local Triple Modular Redundancy (LTMR)
  -
  -

Local Triple Modular Redundancy (LTMR):

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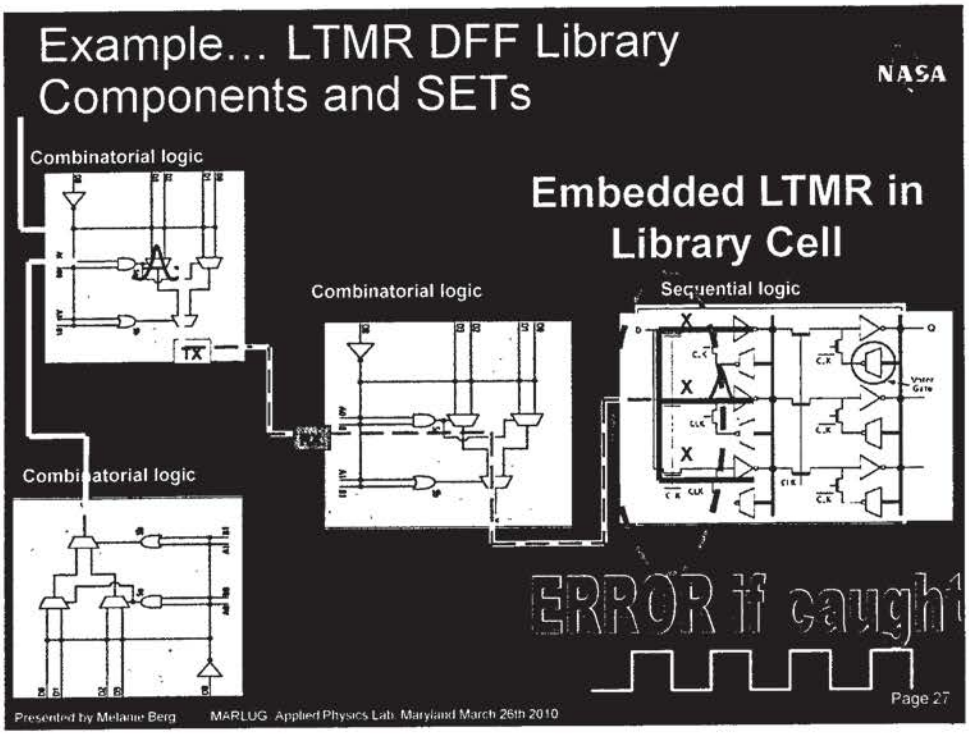
- Triple Each DFF + Vote+ Feedback Correct at DFF
- Unprotected:
  - Clocks and Resets… SEFI
  - Transients (SET->SEU)
  - Internal/hidden device logic: SEFI


Example... LTMR DFF Library Components and SETs
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Combinatorial logic
Embedded LTMR in Library Cell
Combinatorial logic
Sequential logic
TX
Combinatorial logic
ERROR if caught
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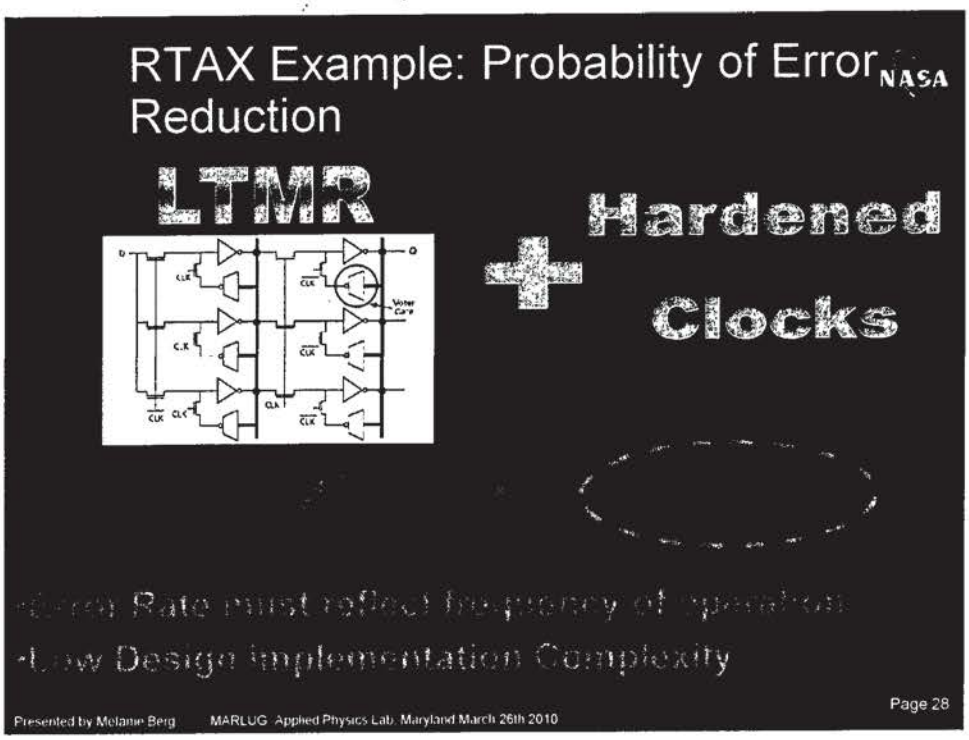
RTAX Example: Probability of Error Reduction
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LTMR
Hardened Clocks
Low Design Implementation Complexity
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Example…Upper-Bound Error Prediction for LTMR + hardened Global Routes RHBD

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- Given…15MHz to 120MHz: Dynamic Error Bit Rate

$P(fs)_{SET \rightarrow SEU}$:

Source: NASA Goddard

Upper-Bound Error Prediction Actel RHBD Anti-fuse FPGA

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With embedded LTMR Mitigation + Hardened Clocks

50,000 DFFs

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Reducing System Error: Common Mitigation Techniques

- Triple Modular Redundancy:
  -
  -
  - Global Triple Modular Redundancy (GTMR)
  -

Global Triple Modular Redundancy (GTMR): Largest Area → Complexity

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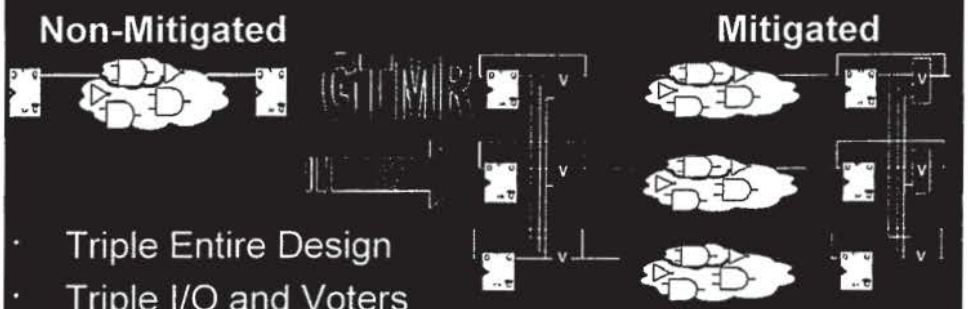

- Triple Entire Design
- Triple I/O and Voters
- Unprotected – hidden device logic SEFIs
- Can not be an embedded strategy: Complex to verify

GTMR Proves To be A Great Mitigation Strategy... BUT...

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- Triplicating a design and its global routes takes up a lot of power and area
- Not part of the provided and well tested/characterized library elements
- Generally performed after synthesis by a tool– not part of RTL
- Difficult to verify
- Additional complications with Clock Skew and domain crossings
- Can be implemented in an ASIC... but is not considered as a contemporary methodology

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Reducing System Error: Common Mitigation Techniques

- **Triple Modular Redundancy:**
  -
  -
  -
  - **Distributed Triple Modular Redundancy (DTMR)**

DTMR

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- Looks a lot like GTMR only difference is that the Global routes and I/O are not triplicated
- Small reduction in area vs. GTMR
- Small reduction in power vs. GTMR
- Can be slightly slower than GTMR because all circuitry share the same clock

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Section IV: The Automation Process

Automation through Synthesis

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- Mentor Graphics and Synplicity provide TMR insertion
- It is up to the designer to understand which type of TMR to implement based on the target FPGA and the target space environment

FPGA	LTMR	DTMR	GTMR
Antifuse			
SRAM			
Flash			

General Recommendation
Not Recommended but may be a solution for some situations
Will not be a good solution

Automation Process

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VHDL

Select Mitigation

Synthesis

Review Synthesis Output

Gate Level Simulations

Summary

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- SEEs will affect FPGAs in space radiation environments
- TMR has been the most effective SEE mitigation technique
- There are many types of TMR:
  - BTMR
  - LTMR
  - DTMR
  - GTMR
- Vendors have integrated different TMR schemes into their synthesis package
- The designer must be aware of the target FPGA and its SEE sensitivity before using any automated approach
- After TMR insertion, a rigorous review and simulation process must be performed