NEPP Electronic Technology Workshop
June 22-24, 2010

National Aeronautics and Space Administration

Ultra-Scaled CMOS Radiation Performance

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Intro

- Ultra-scaled CMOS includes commercial foundry capabilities at and below the 90 nm technology node
- Some evaluations take place using standard products, others are focused on test characterization vehicles (memories, logic/latch chains, etc.)
- NEPP focus is two-fold:
  - Conduct early radiation evaluations to ascertain viability for future NASA missions – leverage commercial technology development
  - Uncover gaps in current testing methodologies and mechanism comprehension – early risk mitigation

To be presented by Jonathan A. Pellish at the NASA Electronic Parts and Packaging (NEPP) Program Electronic Technology Workshop, NASA-GFSC, Greenbelt, MD, June 22-24, 2010 and published on http://nepp.nasa.gov.

Intro

- **Large source of collaboration with external partners:**
  - **Cypress Semiconductor**
  - **IBM Corporation**
  - **Intel Corporation**
  - **Texas Instruments**
  - **STMicroelectronics**
  - **Naval Research Laboratory**
  - **Sandia National Laboratories**
  - **Vanderbilt University**
  - **The Georgia Institute of Technology**

Scaled CMOS

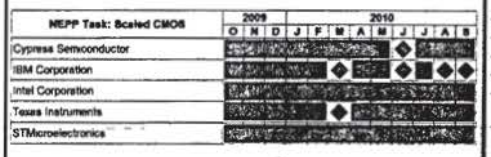
Description:

- Continue task to evaluate scaled CMOS technologies (< 100 nm) from Cypress Semiconductor, IBM, Intel, Texas Instruments, and STMicroelectonics using state-of-the-art test vehicles and products, and
- Determine inherent single-event effects (SEE) tolerance of Trusted Access Program Office (TAPO) product flows, and
- Identify challenges for future SEE hardening efforts
- Investigate new SEE failure mechanisms and effects, and
- Provide data to NASA/DTRA modeling programs.
- Testing covers both destructive and non-destructive SEE using heavy ion and protons
- Recent emphasis has been on low-energy proton soft errors induced by direct ionization

FY10 Plans:

- Cypress: evaluate heavy ion data from 65 nm quad data rate SRAM; conduct heavy ion and possible pulsed laser evaluation of 90 nm non-volatile SRAM.
- IBM: continue analysis of FY09 45 nm SOI SRAM data to assess role of proton direct ionization soft errors (both single and multi-bit); extend accelerated ground tests to 45 nm SOI latches; employ cold laser ablation and XeF_2 to yield advanced flip-chip sample preparation for low-energy protons and pulsed laser testing; extend studies to 32 nm SOI when available.
- Intel: continue evaluation of test articles as available
- TI: continue comparison of 65 and 45 nm data; support Vanderbilt efforts to gather SEL and exotic particle SEU data; support modeling efforts.
- STMicro: develop test set for 65 nm test characterization vehicle.

Schedule:



- All tasks are currently ongoing
- Diamonds indicate completed or scheduled tests

Deliverables:

- Quarterly status reports to NEPP/DTRA
- Test reports
- Updates to lessons learned
- Presentations at leading technical conferences
- Publications in refereed journals

Goals

- Cypress Semiconductor
  - Complete design of 90 nm CMOS non-volatile SRAM test sets
  - Collect initial SEE data sets – heavy ion and pulsed laser
- IBM Corporation
  - Gather first heavy ion and proton data sets on 45 nm SOI latches
  - Analyze low-energy proton and alpha particle data for latches and SRAM
- Texas Instruments
  - Continue investigation of layout dependence on heavy ion SEL in 45 nm CMOS
  - Support additional accelerated tests to aid modeling efforts

Goals

- Intel Corporation
  - Work with vendor to develop and perform radiation tests for 32 nm CMOS technology
- STMicroelectronics
  - Develop test set for 65 nm CMOS test vehicle
  - Identify appropriate tests for provided hardware

Expected Impact to Community

- Encouragement for early-adoption of advanced technologies
  - Technology development and non-recurring engineering leverage
- Identification of new failure mechanisms
  - Risk reduction
  - Refinement of advanced test methodologies
- Support existing and foster new relationships with industry
  - Maintains a proactive (not reactive) stance for the radiation community

Status/Schedule

- Cypress Semiconductor
  - Completed data analysis of 90 nm, 4 Mbit asynchronous SRAM (FY09 TAMU data)
  - Completed initial heavy ion test of 4 Mbit non-volatile SRAM (FY10 LBNL data)
- IBM Corporation
  - Completed 45 nm SOI latch test set design
  - Completed initial 45 nm SOI latch heavy ion test (FY10 TAMU)
  - Completed initial 45 nm SOI proton test (FY10 IUCF)
  - Completed follow-up heavy ion testing of 45 nm SOI latches, including RHBD variant (FY10 LBNL)
- Texas Instruments
  - Completed initial heavy ion SEL analysis (FY09 TAMU & LBNL) on 45 nm CMOS
  - Completed support of initial tests at TRIUMF (FY10) on 45 nm CMOS

Status/Schedule

- **Intel Corporation**
  - **Continuing discussions with Intel to gain access to 32 nm hardware**
  - **Radiation testing looks likely for FY10Q4**
- **STMicroelectronics**
  - **Completed initial conversation with Albert Ouellet and Philippe Roche regarding transfer of 65 nm CMOS hardware from STMicro foundry**

FY10 Publications

Single-Event Upsets and Multiple-Bit Upsets on a 45 nm SOI SRAM

David F. Heidel, *Senior Member, IEEE*, Paul W. Marshall, *Member, IEEE*, Jonathan A. Pellish, *Member, IEEE*, Kenneth P. Rodbell, *Senior Member, IEEE*, Kenneth A. LaBel, *Member, IEEE*, James R. Schwank, *Fellow, IEEE*, Steven E. Rauch, *Senior Member, IEEE*, Mark C. Hakey, Melanie D. Berg, *Member, IEEE*, Carlos M. Castaneda, *Member, IEEE*, Paul E. Dodd, *Senior Member, IEEE*, Mark R. Friendlich, Anthony D. Phan, Christina M. Seidleck, Marty R. Shaneyfelt, *Fellow, IEEE*, and Michael A. Xapsos, *Senior Member, IEEE*

Impact of Low-Energy Proton Induced Upsets on Test Methods and Rate Predictions

Brian D. Sierawski, *Member, IEEE*, Jonathan A. Pellish, *Member, IEEE*, Robert A. Reed, *Senior Member, IEEE*, Ronald D. Schrimpf, *Fellow, IEEE*, Kevin M. Warren, *Member, IEEE*, Robert A. Weller, *Senior Member, IEEE*, Marcus H. Mendenhall, *Member, IEEE*, Jeffrey D. Black, *Member, IEEE*, Alan D. Tipton, *Member, IEEE*, Michael A. Xapsos, *Member, IEEE*, Robert C. Baumann, *Member, IEEE*, Xiaowei Deng, *Member, IEEE*, Michael J. Campola, *Member, IEEE*, Mark R. Friendlich, Hak S. Kim, Anthony M. Phan, and Christina M. Seidleck

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 56, NO. 6, DECEMBER 2009

FY10 Publications

Heavy Ion Testing with Iron at 1 GeV/amu

Jonathan A. Pellish, *Member, IEEE*, Michael A. Xapsos, *Senior Member, IEEE*, Kenneth A LaBel, *Member, IEEE*, Paul W. Marshall, *Member, IEEE*, David F. Heidel, *Senior Member, IEEE*, Kenneth P. Rodbell, *Senior Member, IEEE*, Mark C. Hakey, Paul E. Dodd, *Senior Member, IEEE*, Marty R. Shaneyfelt, *Fellow, IEEE*, James R. Schwank, *Fellow, IEEE*, Robert C. Baumann, *Member, IEEE*, Xiaowei Deng, *Member, IEEE*, Andrew Marshall, *Member, IEEE*, Brian D. Sierawski, *Member, IEEE*, Jeffrey D. Black, *Member, IEEE*, Robert A. Reed, *Senior Member, IEEE*, Ronald D. Schrimpf, *Fellow, IEEE*, Hak S. Kim, *Member, IEEE*, Melanie D. Berg, *Member, IEEE*, Michael J. Campola, *Member, IEEE*, Mark R. Friendlich, Christopher E. Perez, *Member, IEEE*, Anthony M. Phan, and Christina M. Seidleck

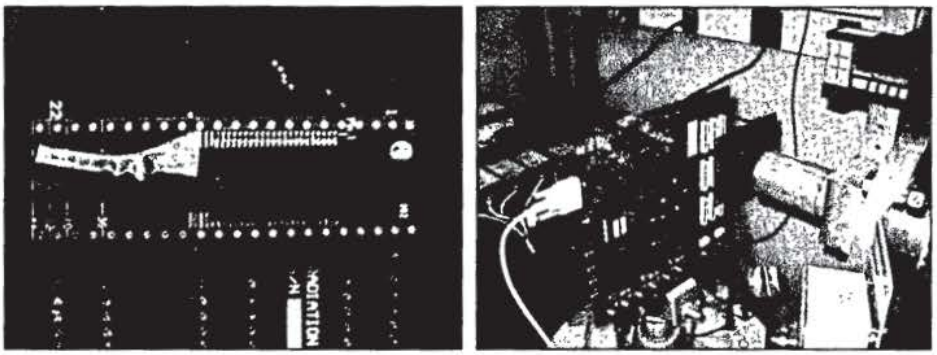
Submitted for publication in
IEEE Transactions on Nuclear Science

FY10 Presentations

- **J. A. Pellish, *et al.*, "Practicality of Evaluating Soft Errors in Commercial sub-90 nm CMOS for Space Applications," presented at the 2010 IEEE Int. Reliability Physics Symp., Anaheim, CA.**
- **J. A. Pellish, *et al.*, "Impact of Spacecraft Shielding on Direct Ionization Soft Error Rates," to be presented at the 2010 IEEE Nuclear Space Radiation Effects Conf., Denver, CO.**
- **N. A. Dodds, *et al.*, "Impact of Spacecraft Shielding on Direct Ionization Soft Error Rates," to be presented at the 2010 IEEE Nuclear Space Radiation Effects Conf., Denver, CO.**

Technical Highlights

90 nm Cypress CMOS

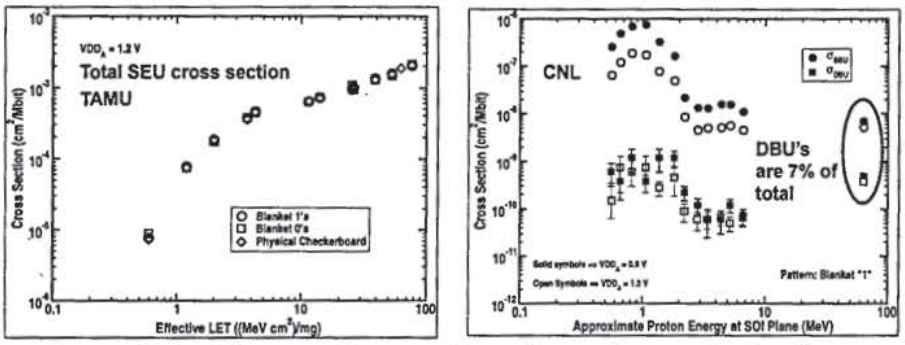


90 nm CMOS non-volatile SRAM

- Heavy ion testing at LBNL
- Good flow of data and information between Cypress and GSFC
- Data analysis shared between GSFC and Cypress

Technical Highlights

45 nm IBM SOI CMOS SRAM



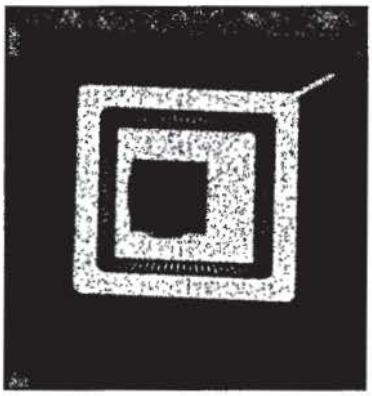
- Completed heavy ion and proton characterization
- Developed procedure to analyze multi-bit upset
- Showed that 45 nm is similar to 65 nm in total SEU cross section – multi-bit cross section is higher

D. F. Heidel et al., *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, Dec. 2009.

Technical Highlights

45 nm IBM SOI CMOS Latches

- Five latch chains of varying length
- Three of the five chains are SEE-hardened designs, including stacked and DICE variants
- Irradiation will be topside, through the back end of line
- Test will be able to reuse 65 nm IBM SOI SRAM test board

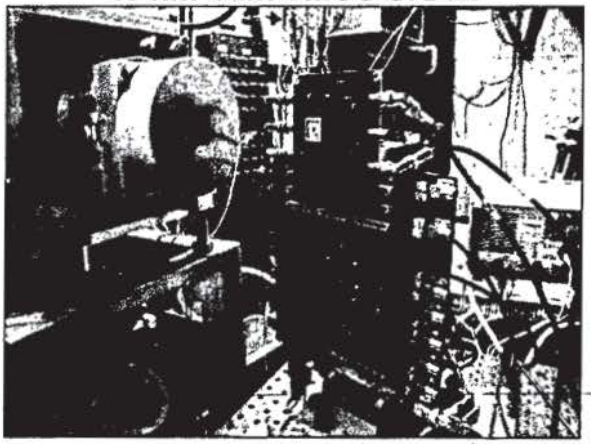


84-pin wire bond package

Technical Highlights

45 nm Texas Instruments CMOS

45 nm bulk CMOS SRAM



UC Davis CNL proton testing at 63 and 6.5 MeV – 23 June 2009

Plans (FY10/FY11)

- Cypress Semiconductor
  - Continue analysis of 65 nm QDR SRAM data (FY10Q3-Q4)
  - Begin analysis of 90 nm non-volatile SRAM data (FY10Q3-Q4)
  - Continue dialog with Cypress to obtain new hardware (FY10Q3-Q4, FY11)
- IBM Corporation
  - Perform low-energy proton and ^{4}He tests at UC Davis (FY10Q3)
  - Perform additional heavy ion tests at TAMU (FY10Q4)
  - Continue SRAM and latch data analysis (FY10Q3-Q4, FY11)
- Intel Corporation
  - Obtain 32 nm hardware and begin development of test sets for TID, dose rate, and proton evaluation (FY10Q3-Q4)
  - Perform radiation testing (FY10Q3-Q4, FY11)

Plans (FY10/FY11)

- STMicroelectronics
  - Obtain 65 nm CMOS test characterization vehicle (FY10Q3-Q4)
  - Begin identification of test sites and development of test sets for TID and SEE evaluation (FY10Q3-Q4)
  - Perform radiation tests (FY10Q4, FY11)
- Texas Instruments
  - Continue analysis of TAMU and LBNL SEL data (FY10Q3-Q4)
  - Support additional testing and modeling efforts as necessary (FY10Q3-Q4, FY11)