Generic Avionics Backplane using Quadraxial Insert Connectors

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Goals

- Reduce costs of avionics system development
 - Through significant reduction of NRE and
 - Through standardization of avionic <u>internal</u> electrical interfaces and mechanical interfaces
- For electrical interfaces by adopting:
 - serial communications interface
 - single voltage power distribution
 - minimal set of commonly used signals
 - Interconnection through a star architecture
 - Common card HUB
 - User card NODE
- For mechanical interfaces by adopting:
 - modular and variable length slot mechanical enclosure concept using card frames (slices) where
 - each Printed Wiring Board (PWB) includes its own portion of the mechanical chassis

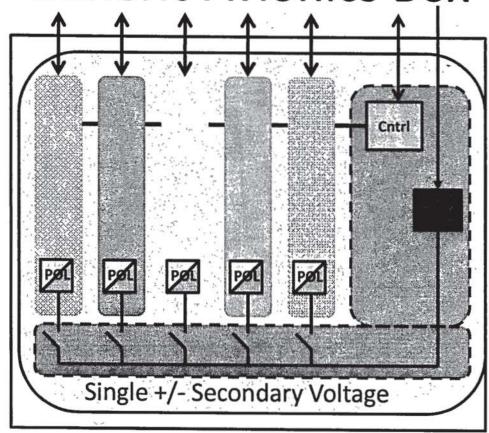
Benefits

- NASA builds a board; ESA or JAXA builds a board; and industry supplies boards that can all connect together to form a subsystem
- Increased data throughput on subsystem level
 - Asynchronous data flows
 - Concurrent data flows
- Lower mass and volume over parallel bus design
- 100% EMI shielded
- No strict requirements for mechanical enclosure design
 - Card frames are standalone mechanical designs
 - Not constrained by distances between boards (board height)
 - Easy mechanical tolerance constraints for harness interconnects
- Support multiple redundancy schemes Single String, Dual Redundant or Cross-Strapped Redundant

Major System Requirements

- High speed communication links
 - Compatibility with high speed (gigabit) serial protocol
- Power distribution
- Reliability
 - Card-to-card isolation
 - Support Redundancy schemes
- Ease of implementation
- Ease of expansion
 - Up to 5 NODE cards in same chassis (6 or 7 cards total including HUB card(s))
 - Front panel expansion possible







= DC/DC Power Converter



= Electronics enclosure



= Linear

Or Switching



= Functional partition



Primary Power



= Common slice

Secondary Power







Subsystem slice

= Vehicle Control Data Network

= Internal Data Network

Typically Used Backplane Signals

- Signals list derived from experience over many missions:
 - Data
 - Power
 - Clock
 - Telemetry
 - Handshaking/ Auxiliary

Traditional Approach

Electrical

- Custom and/or Euro Card form factor (typically 6U or 3U)
- Parallel Printed Wiring Board backplane (typically PCI)
- Some custom signals added to PCI signal set

Mechanical

Custom Enclosure design with card faceplate integrated with card

Proposed System Description Peer-to-Peer Network

Data

- Full-duplex SERDES communications signaling up to 4 GHz
- AC coupled
- e.g., SpaceWire; SpaceFibre; PCI Express, compatible

Power

- Switched power distribution from HUB
- Hot-pluggable card system
- Up to 3 Amps per NODE (after derating)

Clock

- Individually distributed from HUB
- Flexibility for NODE to eliminate on-card oscillator
- Zero frequency drift
- Superior events synchronization

Dedicated analog telemetry

- Temperature telemetry (1 thermistor per NODE card)
- Ability to eliminate the analog Data Acquisition System (DAS) for each card
 - Only multiplexer for analog signals required

Handshaking/ Auxiliary

- System configuration indicates presence and activity of NODE card
- Master/ Slave indicates which HUB is prime and which is redundant

Proposed System Highlights

Ease of implementation

- 1 large connector per CPU (HUB) card
- 1 small connector per load (NODE) card

System reliability

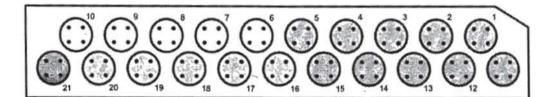
- Single string, or
- Dual redundancy, or
- Cross-redundancy
- Double processing/comm rate when 2 Hub cards are plugged in

System expandability

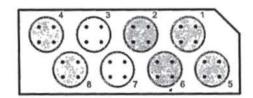
- Can control Dual/Cross redundant subsystems

Suggested Functional Arrangement

HUB Connector

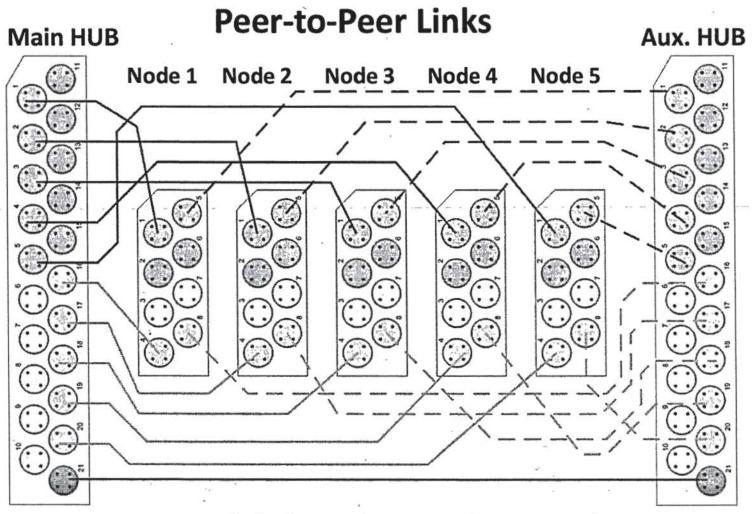


NODE Connector



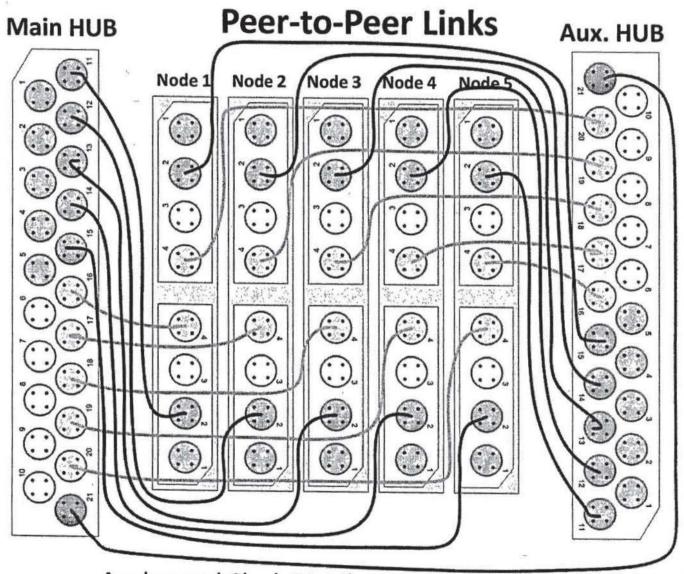
- Analog Telemetry (Node → Hub)
- Power Distribution (Hub → Node)
- Clock Distribution (Hub → Node)
- Node Communication (Hub ↔ Node)
- Cross Communication (Hub ↔ Hub)

Suggested Bus Architecture #1 HUB Connectors are Same Orientation

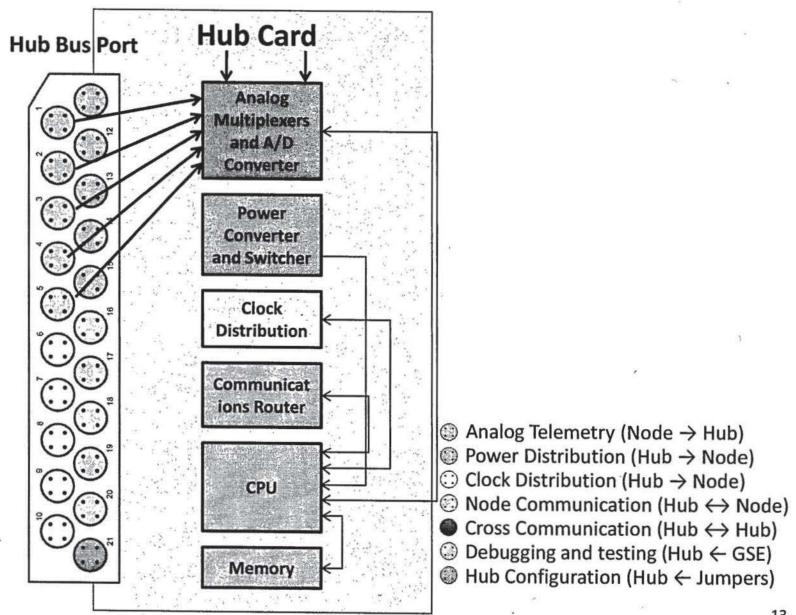


Power and Clock Distribution Links are not Shown

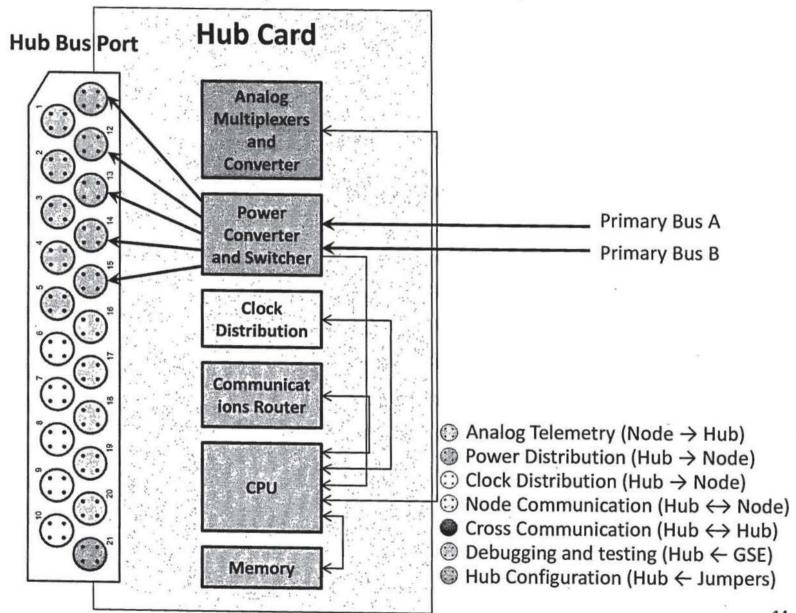
Suggested Bus Architecture #2 HUB Connectors are Reversed Orientation



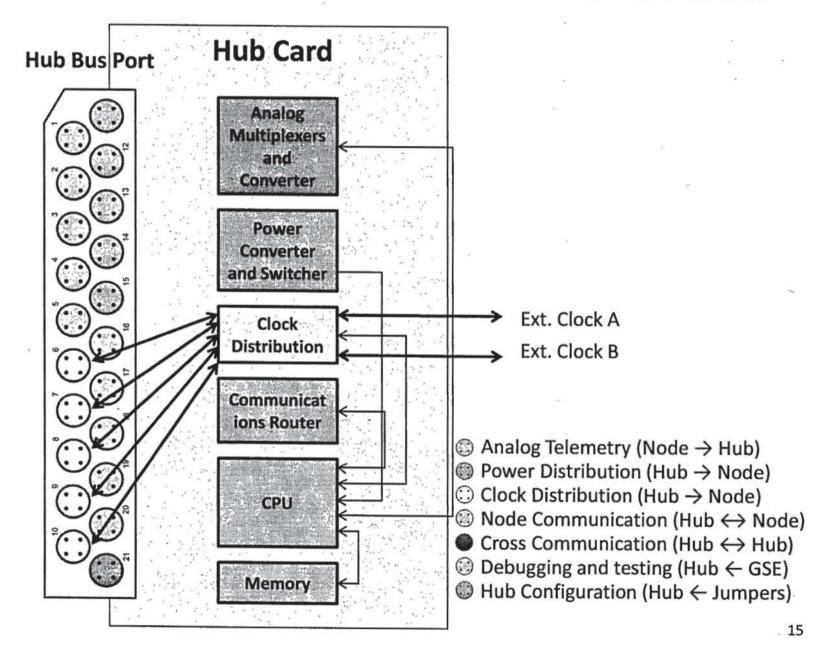
Hub Architecture: Analog Telemetry



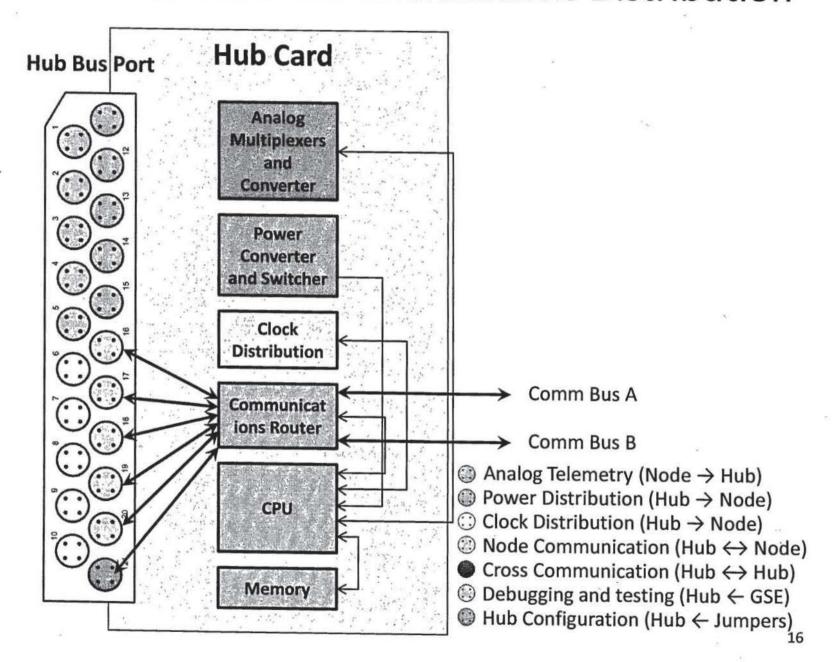
Hub Architecture: Power Distribution



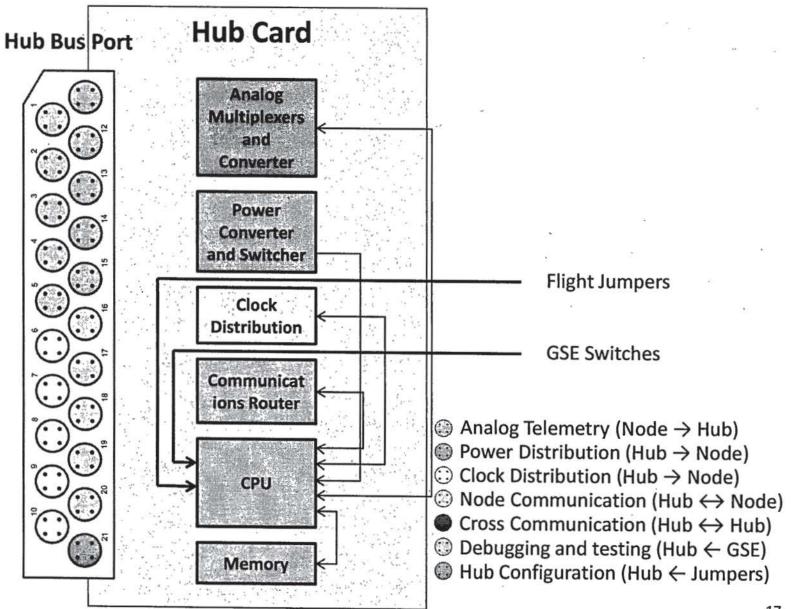
Hub Architecture: Clock Distribution



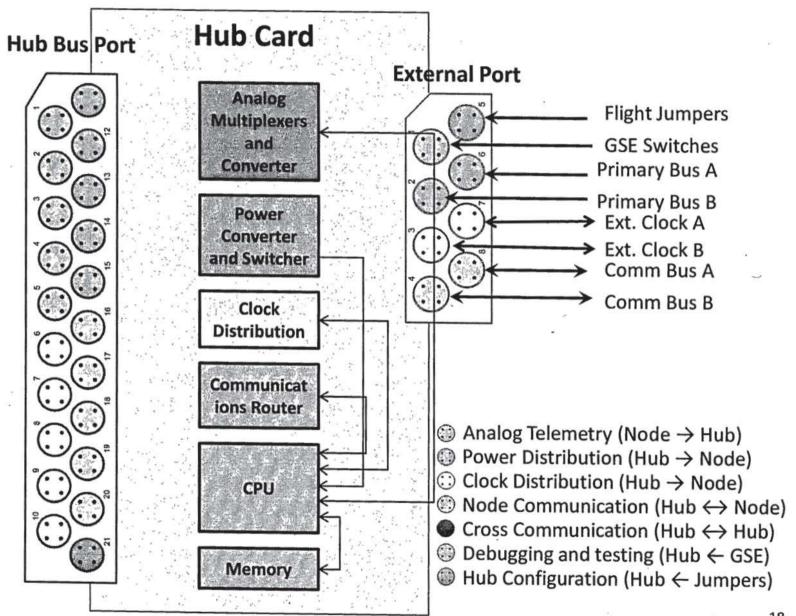
Hub Architecture: Communications Distribution



Hub Architecture: Test and Configuration

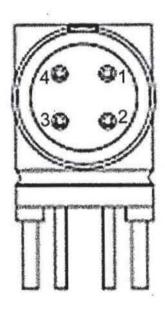


Hub Architecture: Proposed External Port



Connector Inserts Assignments

Group	Pin	Hub Bus Conn	Node Bus Conn	Hub Ext. Conn	Notes
	1	TX+	RX+	TX+	
Node	2	RX+	TX+	RX+	Diagonal pins provide 100Ω impedance
Communication	3	TX-	RX-	TX-	
	4	RX-	TX-	RX-	
Geoss	2	77 4		1 (m) 3 4 (m) (m) (m) 4 (m)	Pragonal pins provide 1000 Impedance
Communication					
	187			不识性是为《数	
	1	Clk_out+	∌. Clk_in+	Clk_out+	1 M. C. Barrell
Sync Distribution	2.	Reset_out	Reset_in "."	Clk_in+	Reset sync all Nodes; Ready tells Hub if Node is active or there is an error condition there
	3	. Clk_out-	Clk_in-	- Clk_out-	
	4	Ready_in	Ready_out*	Clk_in-	
	1	Switched Power (+15V)	Switched Power (+15V)	Prime+28V	1.5A after derating per each pin; total of up to 3A per insert
Power	2	Digital GND	Digital GND	Prime Return	
Distribution	3	Digital GND	Digital GND	Prime Return	
	4	Switched Power (+15V)	Switched Pawer (+15V)	Prime+28V	
	1	Analog_in	Analog_out	A T	Thermistor is required for each Node; Analog signal is optional for Node. Sense tells Hub if Node is plugged
Analog	2	Analog GND	Analog GND		
Telemetry	3	Thermistor_in	Thermistor_out		
	4	Sense_in	Sense_out		
Debugging and Testing	1	学学的一种数学等	14000000000000000000000000000000000000	Pushbutton Reset	Signals are used for Hub/System debugging only; active "low"
	2	第二次第二次第一次	40.10g · \$7.848 (Digital GND	
	3	数195724至2000	1111	EPROM Write Enable	
	4	The second		Watchdog Disable	
	1		151117-10-1	Hub A/B Select	Short on Hub A/B selects between Prime and Auxiliary Hubs; Clock configuration selects which clock runs the Hub; internal or one of
Hub	2			Digital GND	
Configuration	3.			Clock Configuration 1	
	4		1	Clock Configuration 2	externals (for complete sync)

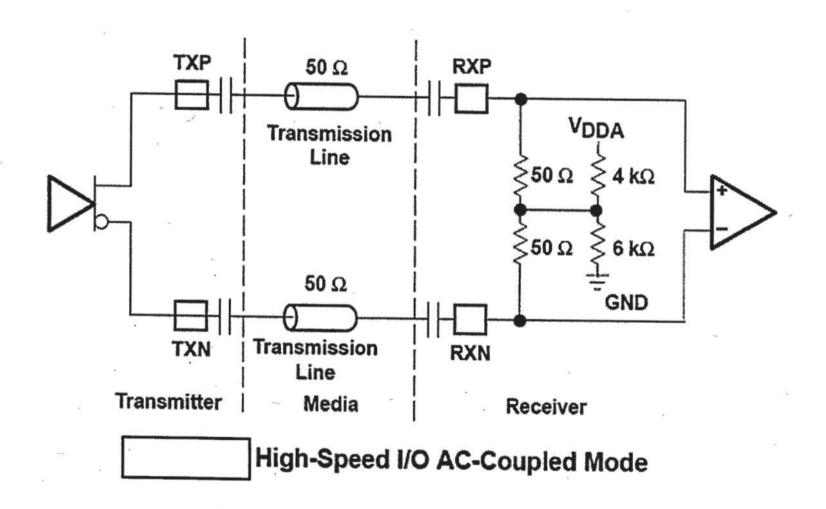


Shield on each Quadrax insert is for EMI/EMC only

Overall Comparison Chart

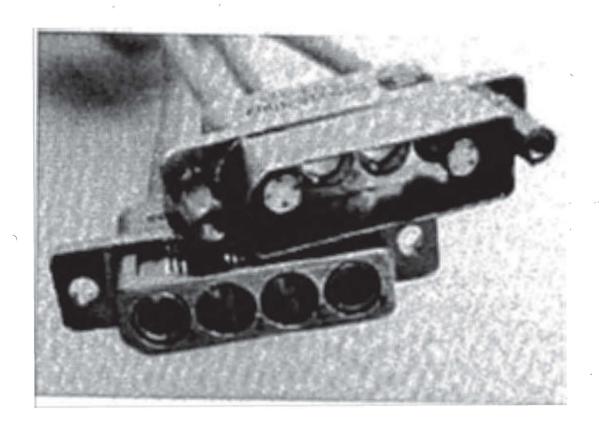
Function	Traditional	Suggested	
Data Interface	Parallel	Serial	
Data Exchange	Half-duplex	Full-duplex	
Data Exchange Method	Synchronous	Asynchronous	
Impedance Matching	Mis-matched	Matched	
Bus Utilization	Single flow	Multiple flows	
Redundancy	None	Full, Cross	
Power Distribution	Multiple low voltages	Single 15V	
Bus Current	High to very high	Low to very low	
Common Mode Voltage	Low	High	
Card Isolation	Complex	Simple	
Hot Plugable	Not possible	Possible ·	
Clock Distribution	System wide & matched	Events Sync	
System Telemetry	Not Specified	Standardized	
Telemetry Type	Not Specified	Digital and Analog	
EM Interference	Leaking	Shielded	
Outgassing	Possible	None	
Connector Pins	Several hundreds	16 per Node + Case	
Bus Interconnect	РСВ	PCB or harness	
Mechanical	3Ú or 6U	3U or 6U	
Insertion Force	Medium	Low	
Mating	Blind mate	Blind mate	
Scoop proof	Yes	Yes	
Inter-card Distance	20-25mm	up to 500mm	

Communications Link Interconnection



Suggested Connector Family

Rugged D-Sub minuature from Sabritec Inc.



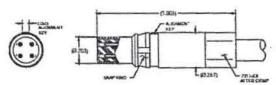
Connector Insert's Parameters

Quadrax insert

	Electrical Specifications	
Dielectric Withstanding Voltage	250 VDC max	
Insulation Resistance	5,000 Mega-Ohms min. @ 100 VDC	
Contact Current Rating	3.0 Amps max.	
Data Rates	>1 Gbits/sec	
Differential Pair Cable Impedance	150 Ohm ± 15 Ohm 100 Ohm ± 10 Ohms	
Signal to Shield Cable Impedance	75 Ohm ± 10 Ohm 50 Ohm ± 7 Ohms	
	Material & Finishes	
Shell & Inner Contacts	Brass per ASTM-B16, alloy UNS C36000 or BeCu per ASTM-B196, alloy UNS C17200, C17300 303 CRES per ASTM-A582 Gold plate per MIL-DTL-45204, Type II, Class 1	
Insulators	PTFE per ASTM-D1710 or ULTERM 1000	
Gasket/Seal	Silicone Rubber per A-A-59588	

Inserts Types

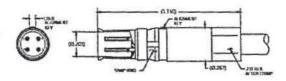
Size 9 Quadrax Pin Contact 100 Ohm



Part Number		Cable
019235-8000	Differential Quad	540-1183-000

For use in P/N: 012800-3002 thru 3006

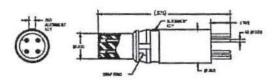
Size 9 Quadrax Socket Contact 100 Ohm



Part Number	Cable Type	Cable
019135-6000	Differential Quad	540-1183-000

For use in P/N: 012700-2002 thru 2006

Size 9 Quadrax Pin Contact PCB Mount 100 Ohm

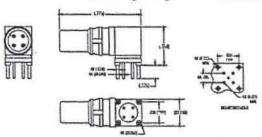




P/N: 019217-2006

For use in P/N: 012800-3002 thru 3006

Size 9 Right Angle PC Tail Quadrax Contact 100 Ohm



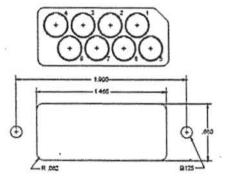
P/N: 019217-1001

For use in P/N: 012800-1000 thru 1001

Suggested Connector Configurations

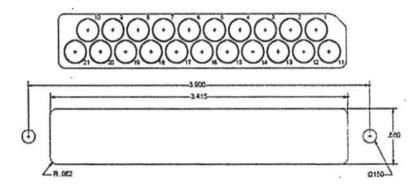
Node Card

Shell Size 3 Arrangement 3-8 8 # 9 Quad/Twinax Contacts



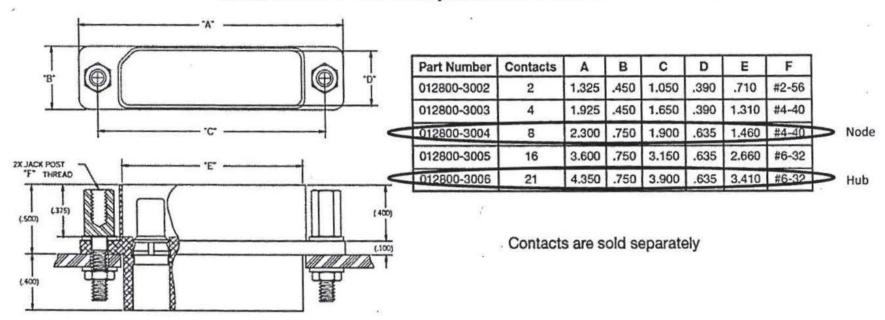
Hub Card

Shell Size 5 Arrangement 5-21 21 # 9 Quad/Twinax Contacts



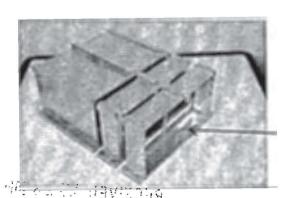
Connector Dimensions

Quad/Twinax D-Sub Receptacle Cable Mount



Conclusion & Forward Work

- Signal list and connector selection presented here are intended to be a starting point for discussions and comments
- Electrical interface is the first priority for agreement
 - architectural approach
 - number of NODE cards in an assembly
 - connector type
 - style
 - signal list
 - pin assignment
- The mechanical concept is secondary but questions to address are:
 - Harness interconnect versus Printed Wiring Board (PWB)
 - Card frame versus single enclosure mechanical design



Card Frame

Please send comments to: Glenn.P.Rakow@nasa.gov