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Packaging Technology for Dielectric-Coating-Less Heavy Ion Radiation Testing of High-Voltage (HV) Electronic Parts

Andrew Woodworth
Glenn Research Center, Cleveland, Ohio

Liangyu Chen
Ohio Aerospace Institute, Brook Park, Ohio

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National Aeronautics and
Space Administration

Glenn Research Center
Cleveland, Ohio 44135

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Andrew Woodworth
National Aeronautics and Space Administration
Glenn Research Center
Cleveland, Ohio 44315

Liangyu Chen
Ohio Aerospace Institute
Brook Park, Ohio 44142

Summary

Testing high-voltage (HV) electronic parts (>300 V) for single event effects (SEE) caused by cosmic rays in the space environment, consisting of energetic heavy ions, and neutron radiation in the upper atmosphere is a crucial step towards using these parts in spacecraft and aircraft. Due to the nature of cosmic radiation and neutrons, electronic parts are tested for SEEs without any packaging and/or shielding over the top of the device. In the case of commercial HV parts, the top of the packaging is etched off and then a thin dielectric coating is placed over the part in order to avoid electrical arcing in between the device surface and wire bonds and other components. Even though the effects of the thin dielectric layer on SEE testing can be accounted for, the dielectric layer significantly hinders post-testing failure analysis. Replicating the test capability of state-of-the-art (SOA) packaging, while eliminating the need for post radiation test processing of the die surface (that obscures failure analysis), is the goal. To that end, a new packaging concept for HV parts has been developed that requires no dielectric coating over the part. Testing of prototype packages used with Schottky diodes (rated at 1200 V) has shown no electrical arcing during testing and the leakage currents during reverse bias testing are within the manufacturer's specifications.

Introduction

Testing electronic parts for susceptibility to single event effects (SEE) that are triggered by cosmic radiation (energetic heavy ions) in space or neutrons in the upper atmosphere is a critical step towards using an electronic part in spacecraft and aircraft applications (Refs. 1 and 2). Packaging is essential to the operation of these devices and all microelectronic devices require some sort of packaging in order to interface with other circuitry. In the case of vertically integrated high-voltage (HV) Schottky diodes, contact must be made to the anode (top surface of the device) and cathode (back side of the device). Therefore, packaging must hold the diode in place (diode size is ~3 by 3 by 0.3 mm) and provide electrical current paths to both the cathode and anode. Cathode attachment is usually done with a conductive epoxy to secure the cathode to a copper backplane that extends from the device and gives ample space for large wires to be bonded (providing a current path). For the anode, wires are bonded to the anode surface and then to an interconnect pad that allows for larger wires to be attached (providing a current path). In order to prevent electrical arcing from the anode bonded wires to the backplane, a high breakdown dielectric material is always present.

Testing protocol (Ref. 3) requires the power device die to be unshielded; this is achieved by deencapsulating commercial parts from selected areas of their packaging, which leaves the bare die and wire bonds exposed. However, this process also weakens the dielectric strength of the packaging and for HV parts (rated for >300 V), arcing occurs between the backplane wire and/or die. Therefore, current SEE testing methods call for a thin (~1 mil/0.025 mm) of a dielectric film (e.g., parylene) to be deposited on the surface of the die. Figure 1(a) shows a depackaged Schottky diode with a parylene coating. Visible

in the image is the anode surface of the diode along with wires bonded to the anode surface. The backplane and the anode wires make the connection to the larger leads on the right-hand side of the image that are used to connect to other electronic components. The black plastic dielectric material that is used to encapsulate the diode is also visible surrounding the diode in Figure 1(a) (Ref. 4). While the effects of the dielectric coating on the SEE testing can be quantified and accounted for in the analysis of results, the process of removing the coating complicates identification and inspection of failure points. Black dielectric packaging left on the surface from the depackaging process, visible in Figure 1(b), complicates identifying points of failure. Dielectric coatings placed on the surface blur features during optical microscopic inspection as can be seen when comparing Figure 1(b) and (c) (before and after dielectric coating) and completely blocks surface features to analysis by scanning electron microscopy (SEM) and many other types of surface analysis. There are packaging schemes that can be used to package bare die (electronic parts with no packaging) without the presence of the black plastic dielectric, but those schemes still require some sort of dielectric coating to prevent arcing. In order to remove the coating, chemical and mechanical processes need to be used. These coating removal processes are likely to alter the surface features and obscure the failure analysis.

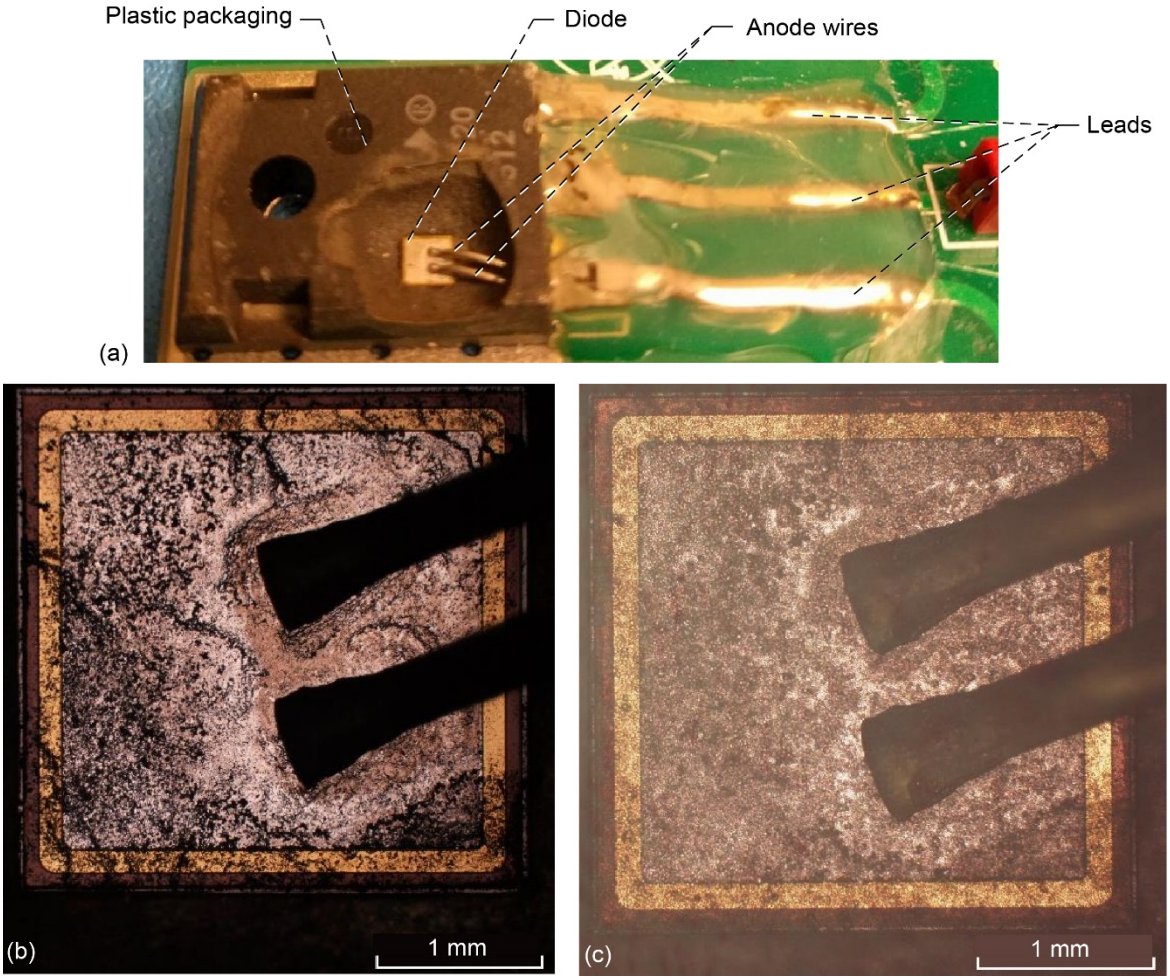

Figure 1.—Depackaged Schottky diode and diodes and bonded wires. (a) Schottky diode with a dielectric (parylene) coating showing leads, anode wires, diode, and plastic packaging. Depackaging was done using fuming acid, and the etch area is clearly visible around the diode. (b) Diode and bonded wires after depackaging with acid. (c) Diode from part (b) after dielectric (parylene) coating.

Therefore, a packaging scheme that does not require a dielectric coating, while replicating the state-of-the-art (SOA) decapsulated and parylene-coated packaging test's capability, would be of great use in failure analysis of HV electronic parts. While the description in this section has been focused on vertically integrated Schottky diodes, the design method and challenge applies equally to vertical PIN diodes and vertical field effect transistors (FETs) such as metal oxide semiconductor field effect transistors (MOSFETs), junction field effect transistors (JFETs), and bipolar junction transistors (BJTs). This paper addresses this packaging challenge.

Technical

This section describes packaging schemes for a bare die designed using direct bonded copper (DBC) on a ceramic polycrystalline alumina substrate for reliability and failure mechanism study of power diodes under high reverse bias voltage, high forward current, and radiation without a dielectric coating layer. The ceramic polycrystalline alumina provides excellent electrical insulation resistivity, suitable to be used as a packaging substrate for SiC power diodes that operate under very high reverse bias >1000 V. Alumina also has very good thermal stability of its electrical properties in the elevated temperature range in which SiC power diodes can function (~250 °C). The DBC layer can be as thick as 0.4 mm and the DBC substrate provides very good thermal conductivity; it is suitable for packaging high-power devices (Ref. 5).

Two substrate designs have been generated using DBC on alumina substrates for device testing as shown in Figure 2 and Figure 3. The design in Figure 2 is for vertical diodes, and the design shown in Figure 3 is for vertical FET tests. These packages are designed to provide sufficient electrical insulation under the 1,100 Vdc maximum reverse bias so dc breakdown will not occur either through the substrate material or ambient air. The design of the substrates also accommodates the electrical leads, two for diodes (Figure 2) and three for FETs (Figure 3), on the same side of the substrate with spaces. These spaces are consistent with those of the existing printed circuit board used by Lauenstein et al. (Ref. 4) for radiation testing. As shown in Figure 2(b) and (c) and Figure 3(c) and (d), the copper pads designated for wire bonding are partially electroplated with 3-mil-thick aluminum film necessary for optimal bond strength for sonic press bonding of thick aluminum wires. Figure 2(c) shows a packaged SiC Schottky power diode.

The diode die is attached to the substrate using conductive epoxy, and 15-mil-diameter aluminum wire is sonic press wedge bonded to electrically connect the diode anode to the pad on the substrate. Both the relative position of the diode die attached on the substrate and the curved shape of aluminum wire are designed to have sufficient airgap (C2) to prevent breakdown under the possible maximum bias of the diode, as shown in Figure 2(d). Figure 2(d) also shows the sufficient substrate gap (C1) of the substrate preventing breakdown.

Figure 4 shows the I-V curves of the packaged diodes under forward and reverse biases without passivation coating of the diode. The measured I-V data of packaged SiC Schottky diodes are in the range of the data of unpackaged diodes provided by the manufacturer (Ref. 6), indicating sufficient electrical insulation as well as breakdown threshold under the reverse bias of the diode provided by the DBC substrate and the packaging geometry design.

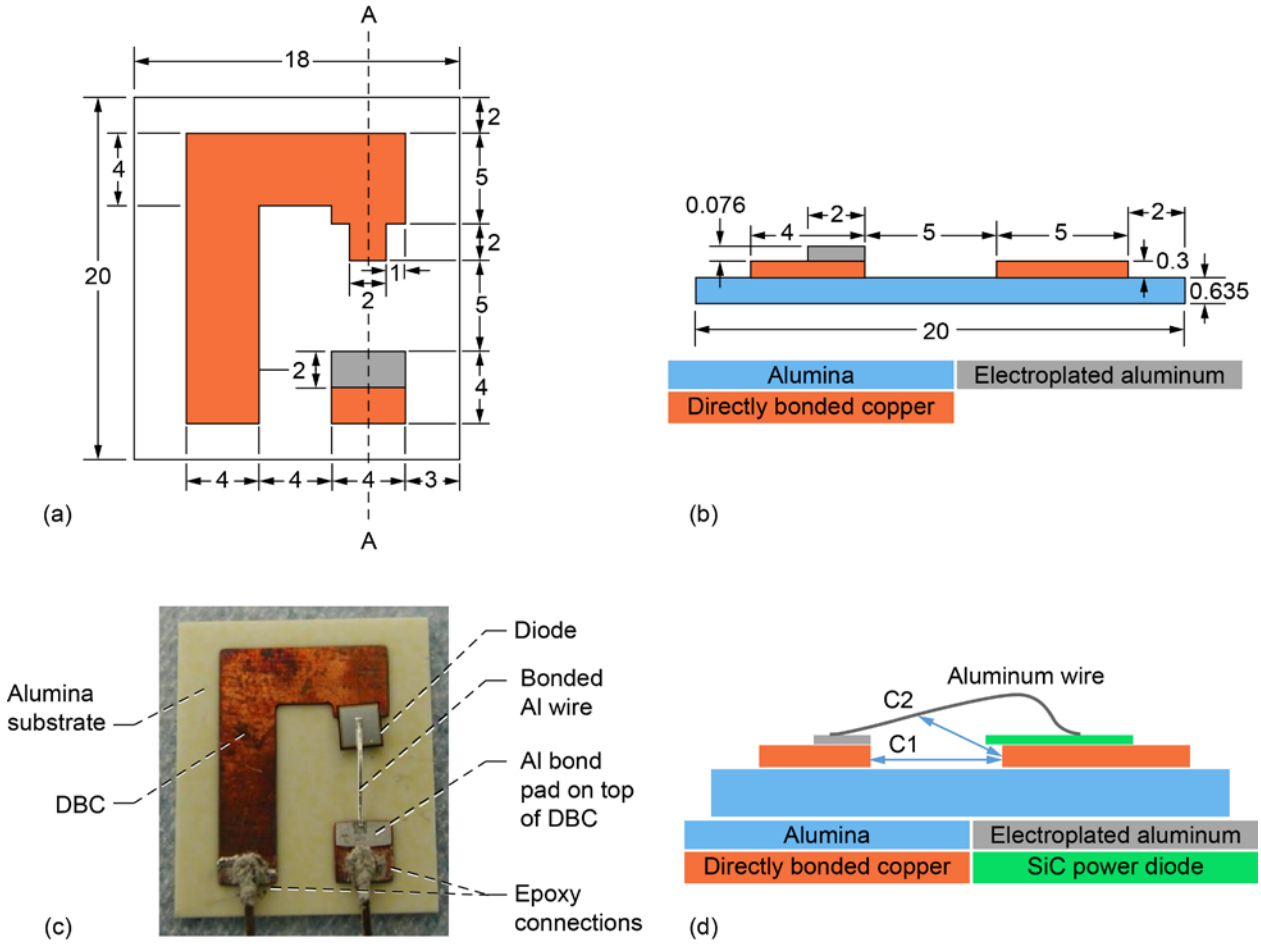

Figure 2.—Diode package using 0.3-mm-thick direct bonded copper (DBC) on a ceramic polycrystalline alumina substrate with 0.075-mm aluminum (Al) film electroplated on the copper. (a) Plan view schematic of the package: shadowed red area is a copper pattern and the gray area is aluminum. Dimensions are in mm and proportional. (b) Cross section at Line A; dimensions are not proportional. (c) Packaged power diode. (d) Critical distances and positioning of the SiC diode preventing air breakdown.

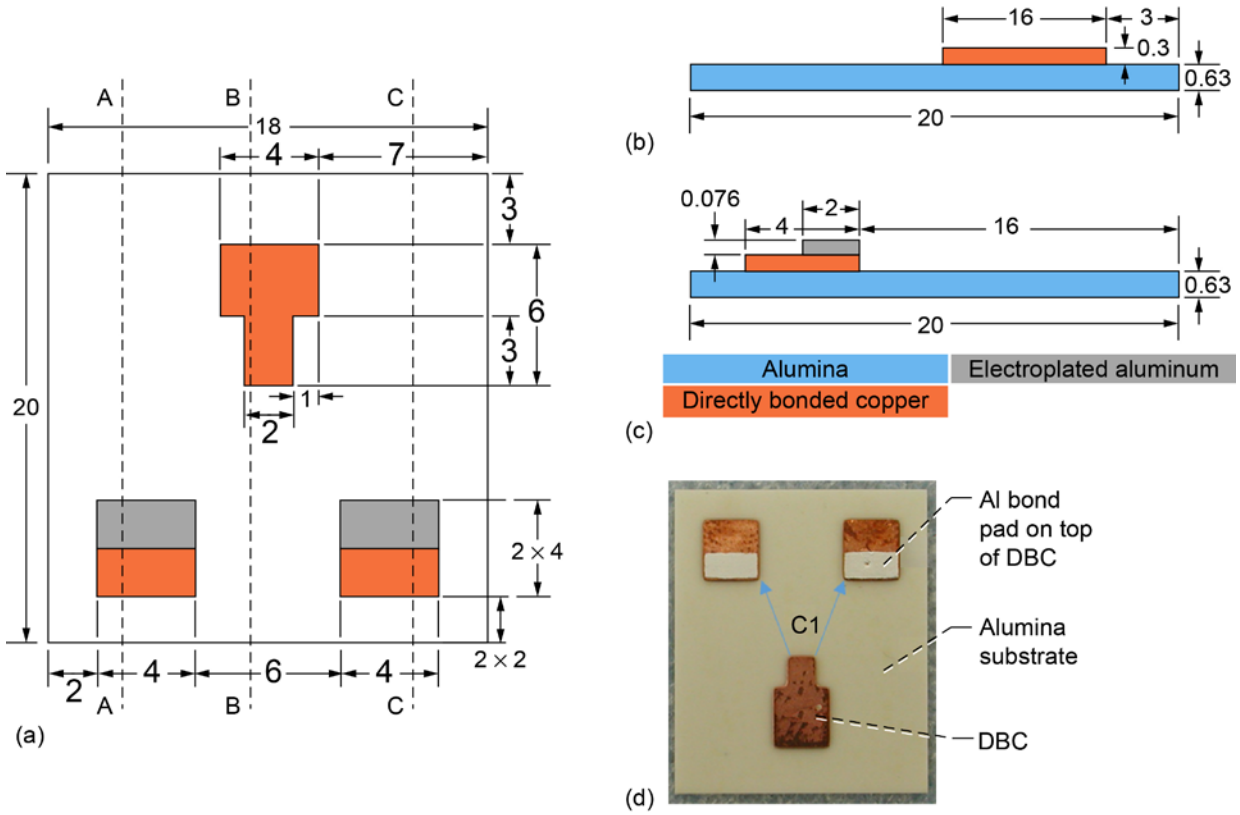

Figure 3.—Package for vertical field effect transistors (FETs) using 0.30-mm-thick direct bonded copper (DBC) on a ceramic polycrystalline alumina substrate with 0.075-mm-thick aluminum (Al) film. (a) Plan view schematic of the package: shadowed red area is copper pattern and the gray area is aluminum. Dimensions are in mm and proportional. (b) Line B cross-section schematic. (c) Lines A and C cross-section schematic; dimensions are not proportional. (d) Substrate showing the distance C1 preventing breakdown. Note that the geometry and spacing of the device to bond pads used for the vertical diodes is also necessary for the FETs (Figure 2(d)).

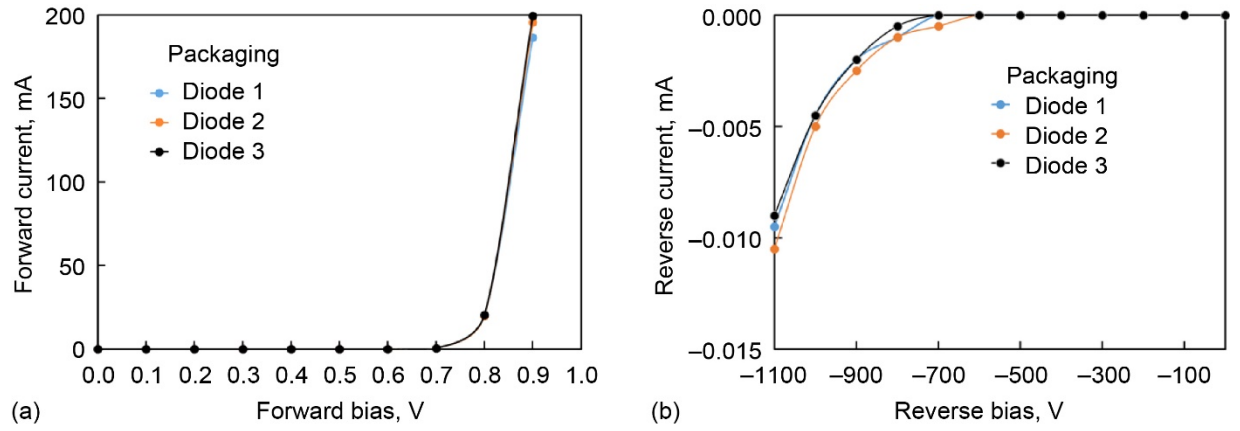

Figure 4.—Forward (a) and reverse bias (b) testing data of a Cree SiC power diode rated for 1200 V mounted on the diode package. No arcing is observed and the leakage current is within the diode manufacturer specifications at 1100 Vdc (the upper limit of the source measure unit).

Conclusions

Specially designed packages were generated to enable packaging of power devices for reliability tests under radiation environments and high electrical reverse bias without dielectric coating for the first time for vertical power diodes and vertical field effect transistors (FETs). The combination of control of the die-attach and wire-bond geometries are key elements of this technology. SiC Schottky diodes have been successfully packaged and electrically tested using the vertical-diode packaging, without dielectric coating, indicating that the design goal has been achieved. The bare device surface is immediately available (not obstructed by a dielectric requiring post processing of the surface) for direct post-testing failure analysis using microscopic analysis tools such as optical microscopy, focused ion beam (FIB) milling, and scanning electron microscopy (SEM). Direct access of an unaltered, obscured, or covered surface also makes possible the application of scanning probe microscopy techniques (e.g., atomic force microscopy, scanning tunneling microscopy, tunneling atomic forces microscopy, etc.) and/or other techniques that require similar access. Replicating the test capability of state-of-the-art (SOA) packaging, while eliminating the need for post-radiation test processing of the die surface that obscures failure analysis, is the goal of this technology. Understanding the points of failure will be important for manufacturers to develop single event effect (SEE) tolerant high-voltage (HV) devices for a variety of applications. While the use of these packages is for a niche application, they will be a useful tool for future power part development. The results of the radiation tests of SiC power devices enabled by this technology will also provide useful information in developing guidelines for use of HV power electronics in future applications in space.

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