Inclusion of Body Bias Effect in SPICE Modeling of 4H-SiC Integrated Circuit Resistors

Philip G. Neudeck

NASA Glenn Research Center, 21000 Brookpark Road, M.S. 77-1, Cleveland, OH 44135 USA

Neudeck@nasa.gov

Keywords: Integrated Circuit, High Temperature, 4H-SiC, SPICE, Resistor, Body Bias Effect

Abstract. The DC electrical behavior of n-type 4H-SiC resistors used for realizing 500 °C durable integrated circuits (ICs) is studied as a function of substrate bias and temperature. Improved fidelity electrical simulation is described using SPICE NMOS model to simulate resistor substrate body bias effect that is absent from the SPICE semiconductor resistor model.

Introduction

As progressively complex 4H-SiC junction field effect transistor (JFET) integrated circuits (ICs) have reproducibly demonstrated operation for thousands of hours at T > 460 °C, interest in usefully fielding these uniquely durable chips in harsh environment missions has grown [1-3]. Regardless of the circuit complexity, these ICs are made from on-chip interconnection of just two fundamental device types: (1) n-channel 4H-SiC JFETs and (2) n-channel 4H-SiC resistors. In order to maximize availability and ease of use for prospective circuit designers, JFET and resistor models compatible with baseline-version SPICE circuit modeling software have been developed and compared with experimental device measurements [4,5]. The JFET models have included non-negligible substrate body bias effect by employing the baseline SPICE n-channel MOSFET (i.e., NMOS) electrical model. However, the baseline-version SPICE semiconductor resistor R model, which is the basis for the 4H-SiC resistor model approximation reported in [4], makes no provision for substrate body bias effect. This report examines body bias effect measured in 4H-SiC IC resistors and describes the use of NMOS-based models for more accurately simulating DC resistor behavior in baseline-version SPICE.

Experiment

Fig. 1 schematically illustrates the simplified cross-section of a 4H-SiC IC resistor, in which signal current flows through the non-depleted portion of the n-doped channel layer between topside resistor contacts on opposite ends. Resistor body bias effect arises from the junction-bias-dependent extent of n-channel depletion imposed by the substrate-channel pn junction. Even though p-epilayer doping is light to minimize the amount of n-channel depletion, the varying channel-to-substrate biases across circuits (as large as the supply voltage spread, ~ 50V [1-4]) is sufficient to impact resistor electrical characteristics. Fig. 1 also shows a topside n-channel depletion region likely to arise from non-optimized SiO_2 fixed and interface state charge.

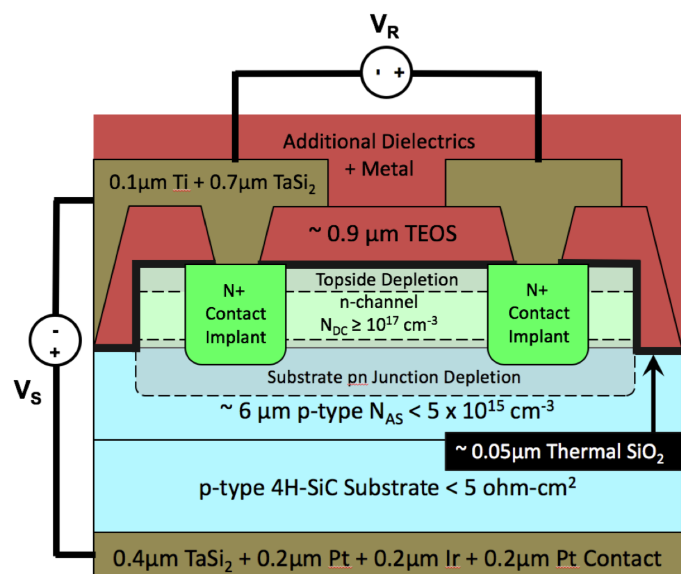


Fig. 1. Simplified 4H-SiC IC resistor cross-section with depletion regions that affect n-channel resistance.

Procedures. The IC fabrication used to realize the studied resistors is described elsewhere [1,2], except that Ti was used for the ohmic contact. DC current-voltage (I-V)

measurements were conducted on high-temperature packaged chips [6] using computer-controlled source-measure units.

Resistor Characteristics. Consistent with results reported in [4], negligible dependence of resistor values on wafer position was observed during 25 °C prober mapping of the wafer prior to dicing. Figure 2 shows measured (dashed lines) at 27 °C and 500 °C for a 480 μm x 6 μm resistor (80-squares, laid out as four series connected 20-square resistors) that exemplifies the major observed resistor behaviors. Linear resistor model simulations are shown as solid lines in Fig. 2. The body bias effect is clearly evident in the measured I-V characteristics (dashed green) that show slight resistance increase as increasingly negative substrate bias V_S depletes the n-side of the substrate-channel pn junction. The I-V characteristics bend down consistent with the fact that bias across the substrate-channel pn junction increases approaching the anode end of the resistor where positive I-V measurement bias V_R is applied. These modest changes in I-V behavior arising from body bias effect are not accounted for in the baseline SPICE semiconductor resistor I-V model (solid green) that is completely linear and ignores body bias between the n-channel and p-epilayer/substrate. As can be seen in Fig. 2, the significant discrepancy between measured resistor I-V data and the linear SPICE semiconductor resistor model grows larger with increasing V_R and $|V_S|$.

Extraction of differential resistance $R_{Diff} = dV_R/dI_R$ (Fig. 2, light blue) quantifies change in device resistance as the anode measurement voltage V_R is swept. If there were ideal contacts, no body effect and no self-heating, the three measured (dashed blue) curves plotted in each part of Fig. 2 would instead fall on a single horizontal (e.g., solid blue) line. While measured data for $V_R < 15$ V is somewhat compromised by slightly rectifying contacts at 27 °C, the differential resistance of the SiC n-channel is dominant for $V_R > 15$ V and/or for T = 500 °C.

To elucidate if device self-heating under bias contributes significantly to I-V bend down as V_R increases, Fig. 3 re-plots 500 °C R_{Diff} data (which exhibits more I-V bending than 27 °C data) as a function of applied anode-to-substrate voltage ($V_{RAS} = V_R - V_S$). The nearly exact overlap of Fig. 3 graph data measured under various combinations of V_R and V_S demonstrates that R_{Diff} data is predominantly a function of V_{RAS}. If resistor self-heating significantly impacted measured I-V characteristics, R_{Diff} values measured at low resistor power (e.g., $V_R = 1$ V) would have been smaller than R_{Diff} values measured at higher power (e.g., $V_R = 40$ V) for the same V_{RAS}.

In Fig. 4, resistor I-Vs of all devices from this wafer that were packaged and tested to 500 °C are plotted with measured current normalized to 1-square layout dimension (I_{RNorm}) for $V_S = 0$ V. Despite disparities in resistor layout dimensions and wafer location, the normalized currents all exhibit nearly the same magnitude of bending and fall within 20% of the average for each temperature. The resistor plotted with the thickest (dark blue) dashed line of Fig. 4 is representative since it falls in the middle of both I-V data sets, and is actually the same resistor whose data is shown in Figs. 2 and 3.

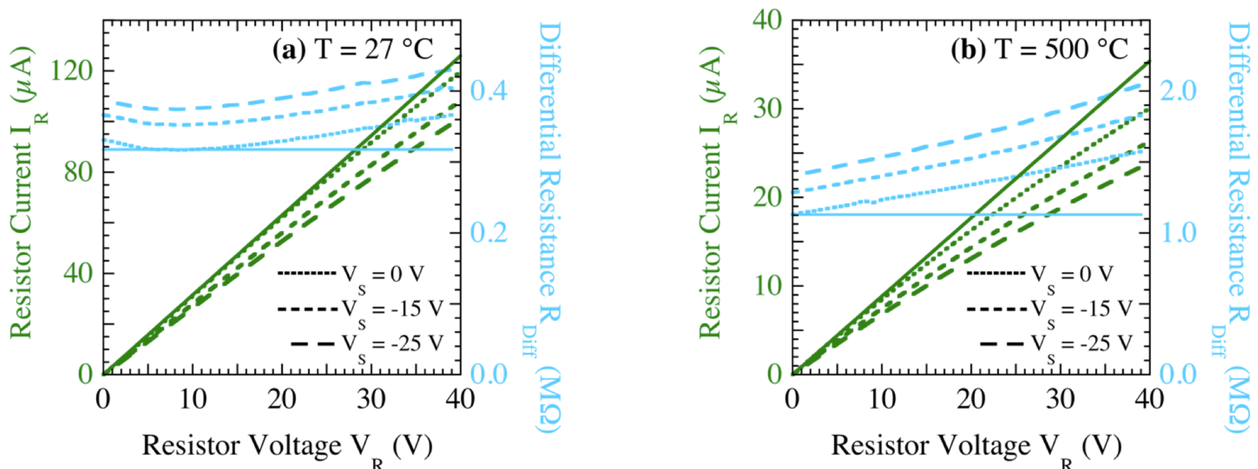


Fig. 2. Comparisons of DC measured 80-square resistor electrical characteristics (dashed lines) with linear resistor model simulations (solid lines) at V_S of 0 V, -15 V, and -25V at (a) 27 °C and (b) 500 °C. The difference between linear model and measured is significant, and grows larger with increasing V_R and $|V_S|$.

SPICE Models. Refs. [4,5] describes the modeling of SiC IC JFETs using the baseline SPICE NMOS LEVEL=1 model. While Fig. 1 depicts a resistor cross-section, it can also be considered a long-channel JFET with the electrically biased p-epilayer/substrate serving as the gate terminal. The magnitude of negative substrate voltage V_S required to completely deplete the n-channel is large since $N_{AS} << N_{DC}$, so the JFET operates in the linear region as a substrate-bias controlled resistor. A resistor with body effect can therefore be modeled in baseline SPICE as a long-channel, large threshold voltage NMOS transistor, wherein substrate bias V_S is applied to (i.e., becomes) the gate terminal of the NMOS device instance.

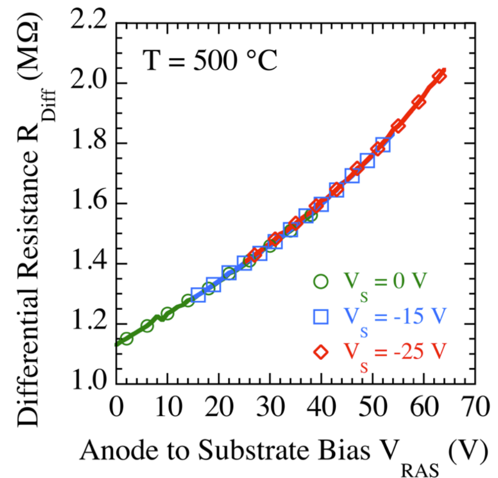


Fig. 3. Differential resistance R_{Diff} plotted vs. anode to substrate bias V_{RAS} that indicates I-V bending is not due to self-heating (see text).

The SPICE NMOS LEVEL=1 parameters for modeling IC resistors as MOSFETs with body bias effect can theoretically be calculated from the device structure. However, such calculations for VTO and KP NMOS parameters require quantitative knowledge of the oxide/interface charge that produces the topside depletion (Fig. 1). Alternatively, VTO and KP parameters can be extracted from measured resistor I-V data. The low drain-bias NMOS parameter extraction procedure described in Ref. [7] was employed to extract VTO and KP from Fig. 2 I-V data. Other SPICE NMOS LEVEL=1 parameters that are not a function of oxide/interface charge were calculated from standard depletion approximation formulas [5].

Fig. 5 compares SPICE simulated resistor I-Vs with the representative (Fig. 2) resistor's $V_S = 0$ V and $V_S = -25$ V measured I-V's at 27 °C and 500 °C. The SPICE NMOS modeled I-Vs (dashed green) provide far better match to measured (dashed light blue) compared to the linear SPICE R model (solid blue), especially for $V_S \approx -25$ V substrate bias conditions employed in 1000+ hour 500 °C integrated circuit demonstrations to date [1-4].

Text input listings for the Fig. 5 SPICE NMOS model I-V simulations are given below each plot. These examples illustrate correct SPICE practices for modeling IC resistors with body effect as NMOS devices. For the MOSFET device instance that is the "resistor" in the SPICE deck (e.g., "MSICRES"), *it is important to make SPICE node connections in the following manner:* The gate and bulk terminals should always be wired to the IC substrate bias (e.g., example node "2"), while the source and drain serve as the resistor contacts. The L and W parameters of the device instance

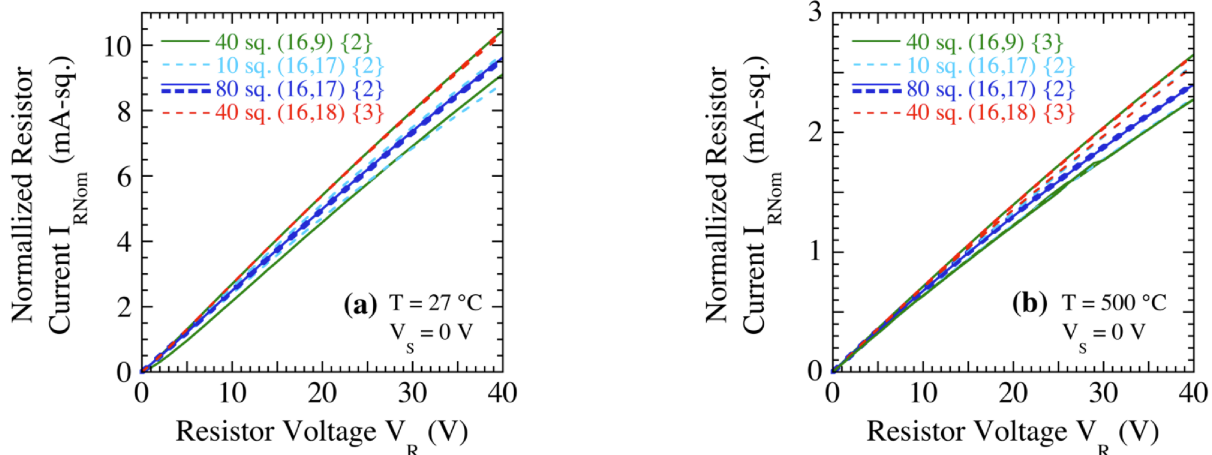
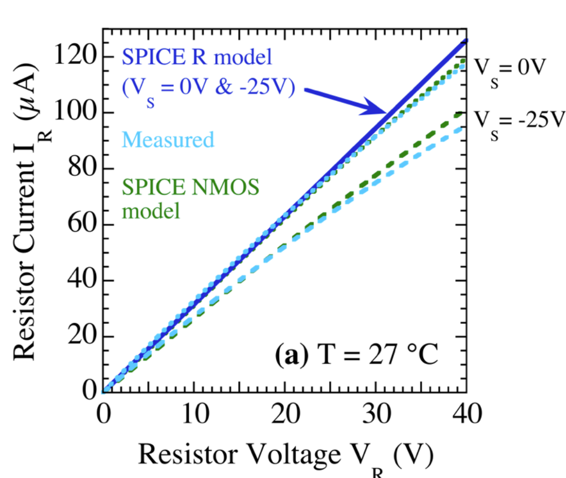
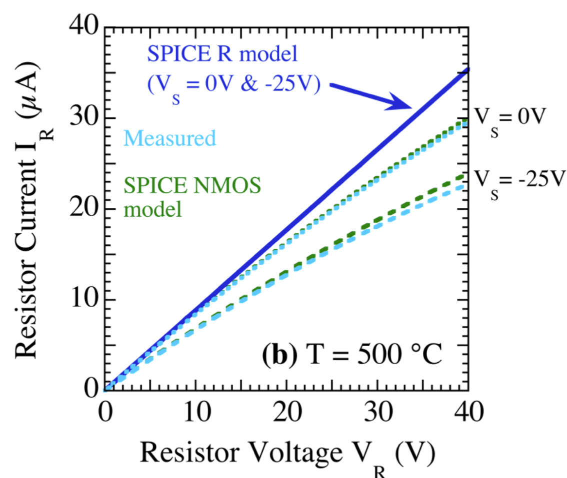


Fig. 4. Dimensionally normallized (a) 27 °C and (b) 500 °C I-Vs from all resistors that were high-temperature packaged from the same wafer. The thickest dashed line (dark blue) is from the same 80 square resistor as plotted in Figs. 2 & 3. Wafer die location coordinates are in parenthesis, and numbers in braces disclose how many resistors of each kind are plotted.




```
*NASA Glenn SiC IC Resistor I-V Simulation 27C
V1 1 0
V2 2 0
MSICRES 1 2 0 2 sicresfet L=4.8E-4 W=6.0E-6
.MODEL sicresfet NMOS LEVEL=1 VTO=-155 KP=1.773E-6
CJ=6.856E-5 PB=2.87 RSH=0.0 PHI=1.435 GAMMA=0.0 JS=0.0
.DC v1 0 40.0 1.0 v2 0 -25.0 -25.0
.PRINT v(1) mag(i(v1))
.END
```




```
*NASA Glenn SiC IC Resistor I-V Simulation 500C
V1 1 0
V2 2 0
MSICRES 1 2 0 2 sicresfet L=4.8E-4 W=6.0E-6
.MODEL sicresfet NMOS LEVEL=1 VTO=-128 KP=5.474E-7
CJ=8.822E-5 PB=1.99 RSH=0.0 PHI=0.998 GAMMA=0.0 JS=0.0
.DC v1 0 40.0 1.0 v2 0 -25.0 -25.0
.PRINT v(1) mag(i(v1))
.END
```

Fig. 5. I-V comparison of linear R SPICE resistor model (solid dark blue) and NMOS SPICE body-effect resistor model (dashed green) with measured data (dashed light blue) for a 480μm x 6μm resistor at (a) 27°C and (b) 500 °C.

should match the physical resistor length and width layout dimensions (in meters). Since the body bias effect in this approach is handled by the voltage on the NMOS gate terminal (not the NMOS bulk terminal), the GAMMA parameter is always set to zero.

Studies comparing use of the linear R resistor model with use of NMOS resistor model in SPICE simulation of 25 °C to 500 °C digital and analog circuits will be reported in future communications.

Conclusion. For improved accuracy circuit design and modeling of 4H-SiC JFET ICs using SPICE, the NMOS resistor modeling approach described in this report should supercede/replace the standard linear SPICE R resistor model reported in [4] that ignores the body bias.

Acknowledgements. D. Spry, L. Chen, G. Beheim, N. Prokop, M. Krasowski, K. Moses, J. Gonzalez, M. Mrdenovich, R. Buttler, R. Meredith, D. Lukco, C. Chang, G. Hunter, G. Ponchak, L. Matus. Work funded jointly by NASA Aeronautics (Transformative Tools and Technologies project) and Science Mission (Planetary Instrument Concepts for the Advancement of Solar System Observations project) Directorates.

References

[1] D.J. Spry, et al., IEEE Electron Device Lett. **37** (2016) 625-628.
[2] D.J. Spry, et al., Proc. IMAPS Int. High Temperature Electronics Conf. (2016) 249-256.
[3] P.G. Neudeck et al., AIP Advances **6** (2016) 125119.
[4] P.G. Neudeck, et al., Proc. IMAPS Int. High Temperature Electronics Conf. (2016) 263-271. Available https://sic.grc.nasa.gov/files/HiTEC2016-SPICEPaperV6.pdf
[5] P.G. Neudeck, D.J. Spry, L. Chen, Materials Science Forum **828** (2016) pp. 903-907.
[6] L. Chen, et al., Proc. IMAPS Int. High Temperature Electronics Conf. (2016) 66-72.
[7] E. Profumo, MOS Parameter Measurements, in: P. Antognetti, G. Massobrio (Eds.), Semiconductor Device Modeling with SPICE, McGraw-Hill, New York, 1987, pp. 231-234.