National Aeronautics and Space Administration

New Developments in Field Programmable Gate Array (FPGA) Single Event Upsets (SEUs) and Fail-Safe Strategies

Melanie Berg, MEI Technologies in support of NASA/GSFC

Different Aspects of Mitigation: Things to Think about during Presentation

- Detection:
  - Watchdog (state or logic monitoring)
  - Checking ...Decoding
  - Action
- Masking
  - Not letting an error propagate to other logic
  - Redundancy or checking
  - Turn off faulty path
- Correction
  - Error state (memory) is changed
  - Need feedback

To be presented by Melanie Berg at the Revolutionary Electronics in Space (ReSpace) / Military and Aerospace Programmable Logic Devices (MAPLD) 2011 Conference, Albuquerque, NM, August 22-25, 2011, and to be published on nepp.nasa.gov website.

Mitigation Concerns

- Are you reducing error rate?
  - Strategy may NOT reduce error rate but reduce system error (Masking)
  - Be careful not all FPGAs have the same Single Event Upset (SEU) error signatures
  - Poorly selected/implemented Mitigation scheme may increase upset rate instead of decrease
- Accumulation versus Multiple Bit Upsets (MBUs) may need to be handled differently
- Tradeoffs: Is your scheme buying you anything?
  - May reduce system error rate at a high cost (area, power, complexity, cost)
  - STOP.... Requirements may not need Mitigation
  - If you can't validate that it meets requirements – then you can't fly it

How Safe is Your Design?

- Understand the SEU error mode specifics?
- Are there lock-up conditions in my design?
- Does your strategy protect the entire critical path?
- Is the synthesized design fail-safe?
- Did you mitigate where you expected to mitigate?
- Can your watch-dog catch failure?
- Will your recovery scheme work?
- What are the limitations of your verification strategy?

The list goes on... Based on error signatures of the target FPGA, the designer must keep all points in mind at all stages of the design

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Agenda

- Section I: Single Event Effects (SEEs) in Digital Logic
- Section II: Application of the NASA Goddard Radiation Effects and Analysis Group (REAG) FPGA SEU Model
- Section III: Reducing System Error: Common Mitigation Techniques

Break

- Section IV: When Your Mitigation Fails
- Section V: Xilinx V4 and Mitigation
- Section VI: Fail-Safe Strategies

Agenda (First Half)

- Section I: SEEs in Digital Logic
- Section II: Application of the NASA Goddard Radiation REAG FPGA SEU Model
- Section III: Reducing System Error: Common Mitigation Techniques

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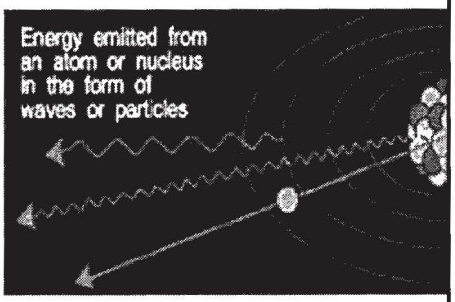
Van Allen Radiation Belts Have Varying Particle Spectra

Van Allen Radiation Belts: Illustrated by Aerospace Corp.

Source of Faults: SEEs and Ionizing Particles

- Terrestrial devices are susceptible to faults mostly due to:
  - Alpha particles: from packaging and doping and
  - Neutrons: caused by Galactic Cosmic Ray (GCR) interactions that enter into the earth's atmosphere.



- Devices expected to operate at higher altitude (Aerospace and Military) are more prone to upsets caused by:
  - Heavy ions: direct ionization
  - Protons: secondary effects

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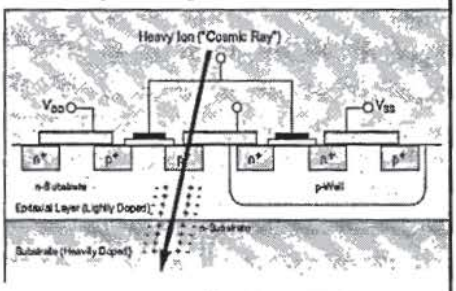
Device Penetration of Heavy Ions and Linear Energy Transfer (LET)

- LET characterizes the deposition of charged particles
- Based on Average energy loss per unit path length (stopping power)
- Mass is used to normalize LET to the target material



$$LET = \frac{1}{\rho}\frac{dE}{dx} \; ; \; MeV\frac{cm^2}{mg}$$

Average energy deposited per unit path length

Density of target material

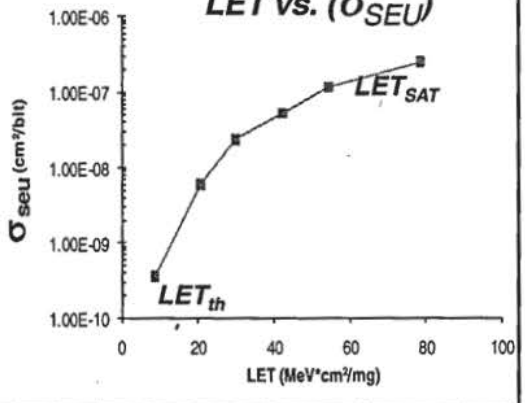
Units

LET vs. SEU Error Cross Section (σ_{SEU})

Terminology:

- Flux: Particles/(sec-cm^2)
- Fluence: Particles/cm^2
- The σ_{SEU} is calculated at several LET values (particle spectrum)
  - LET Threshold (LET_{th}) is the point where errors are first observed (on-set)
  - LET Saturation (LET_{SAT}) is the point where errors stop statistically increasing with LET

$$\sigma_{seu} = \frac{\#errors}{fluence}$$



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Single Event Faults and Common Terminology

- Single Event Latch Up (SEL): Device latches in high current state
- Single Event Burnout (SEB): Device draws high current and burns out
- Single Event Gate Rupture: (SEGR): Gate destroyed typically in power MOSFETs
- Single Event Transient (SET): current spike due to ionization. Dissipates through bulk
- Single Event Upset (SEU): transient is caught by a memory element
- Single Event Functional Interrupt (SEFI) - upset disrupts function

Single Event Effects (SEEs) and FPGA System Error

- FPGA SEUs or SETs can occur in:
  - Configuration
  - Combinatorial Logic (including global routes or control)
  - Sequential Logic
  - Memory Cells

Every Device has different Error Responses – We must understand the differences and design appropriately

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Agenda (First Half)

- Section I: Single Event Effects in Digital Logic
- **Section II: Application of the NASA Goddard REAG FPGA SEU Model**
  - Configuration σ_{SEU} ($P_{configuration}$)
  - Functional Data Path σ_{SEU} ($P_{functionalLogic}$)
  - Microsemi (Actel) ProASIC3 Example
- Section III: Reducing System Error: Common Mitigation Techniques

The NASA Goddard REAG FPGA SEU Model : Top Down Approach

Top Level Model has 3 major categories of σ_{SEU}:

$$P(fs)_{error} \propto P_{Configurat\ ion} + P(fs)_{functional\ Logic} + P_{SEFI}$$

Design σ_{SEU} — Configuration σ_{SEU} — Functional logic σ_{SEU} — SEFI σ_{SEU}

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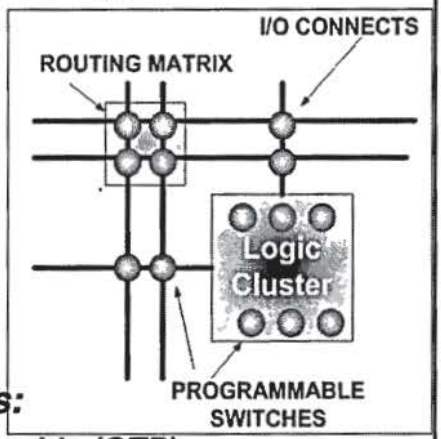
$$P(fs)_{error} \propto P_{Configurat\ ion} + P(fs)_{functional\ Logic} + P_{SEFI}$$

Configuration SEU Cross Sections

Place, Route, and Gate Utilization are Stored in the FPGA Configuration

- ***Configuration Defines:*** ***Arrangement of pre-existing logic via programmable switches***
  - ***Functionality (logic cluster)***
  - ***Connectivity (routes)***
  - ***Placement***
- ***Programming Switch Types:***
  - ***Antifuse: One time Programmable (OTP)***
  - ***SRAM: Reprogrammable (RP)***
  - ***Flash: Reprogrammable (RP)***



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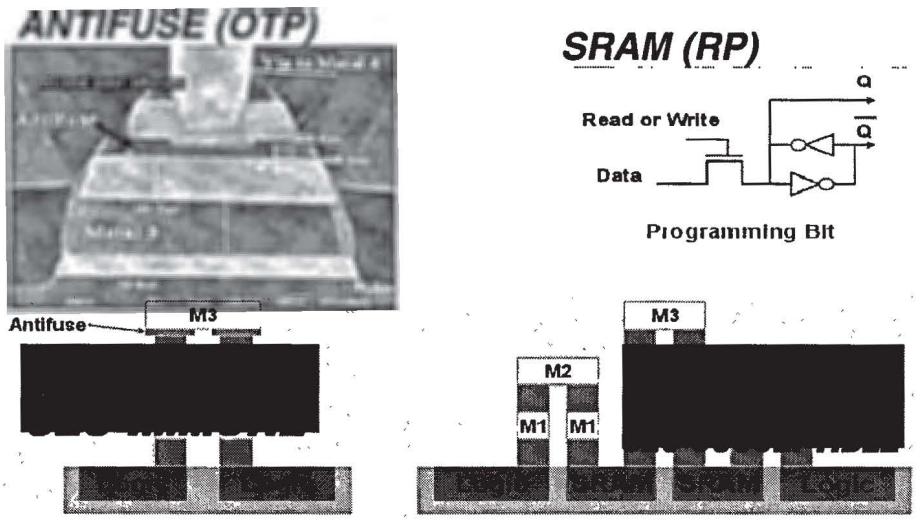
Programmable Switch Implementation and SEU Susceptibility



Configuration SEU Test Results and the REAG FPGA SEU Model

Configuration	REAG Model
Antifuse	$P(fs)_{error} \propto P_{functionalLogic}(fs) + P_{SEFI}$
SRAM (non-mitigated)	$P(fs)_{error} \propto P_{Configuration}$
Flash	$P(fs)_{error} \propto P_{functionalLogic}(fs) + P_{SEFI}$
Hardened SRAM	$P(fs)_{error} \propto P_{Configuration} + P_{functionalLogic}(fs) + P_{SEFI}$

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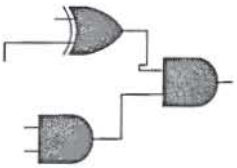
$$P(fs)_{error} \propto P_{Configurat\ ion} + P(fs)_{functional\ Logic} + P_{SEFI}$$

Functional Data Path SEU Cross Sections

Concepts of Synchronous Design

Synchronous Design Basic Building Blocks: Combinatorial Logic and Flip-Flops (DFF's)

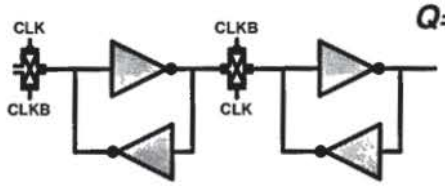


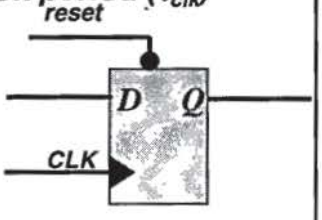
Combinatorial Logic: Output is a function of the inputs after some delay(τ_{dly})

Output=f(input,τ_{dly})

DFF: Captures data input at clock edge and is a function of the clock period (τ_{clk})

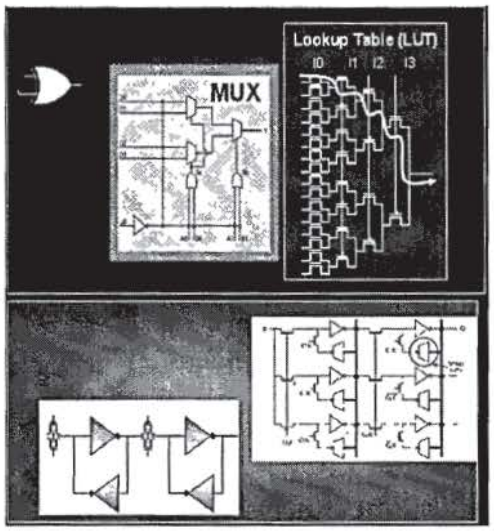
Q=f(D,τ_{clk})





Component Libraries: Basic Designer Building Blocks

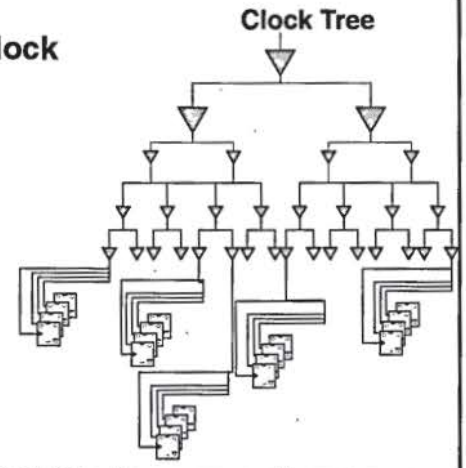
- Combinatorial logic blocks
  - ❑ Vary in complexity
  - ❑ Vary in I/O
- Sequential Memory blocks (Flip-flops or DFFs)
  - ❑ Uses global Clocks
  - ❑ Uses global Resets
  - ❑ May have mitigation



DFF's in a Synchronous Design

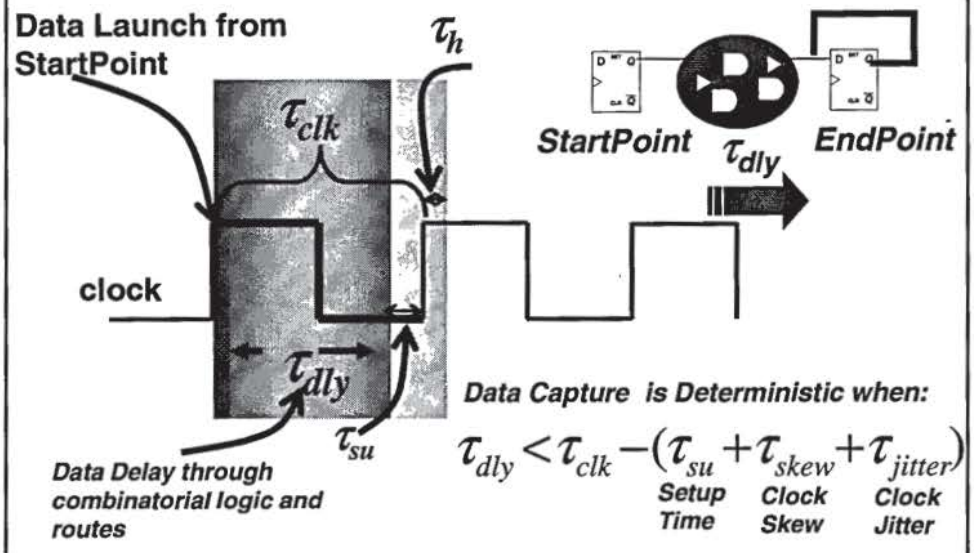
- All DFFs are connected to a clock
- Clock period: τ_{clk}
- Clock frequency: f_s

$$\tau_{clk} = \frac{1}{fs}$$



DFFs are BOUNDARY POINTs in a synchronous design

Deterministic Data Capture...Adhering to Setup (τ_{su}) and Hold Time (τ_h) for a DFF

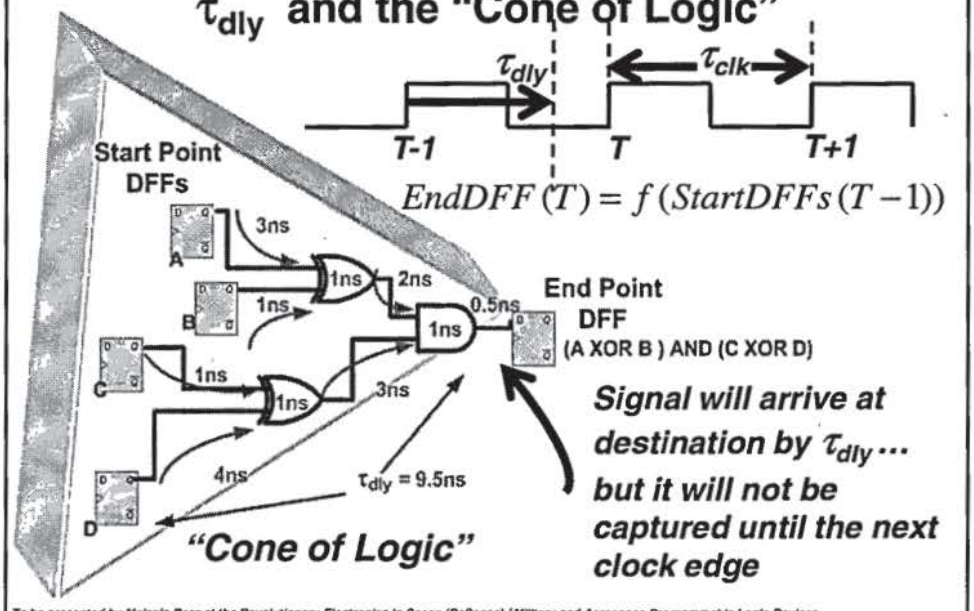


Data Capture is Deterministic when:

$$\tau_{dly} < \tau_{clk} - (\tau_{su} + \tau_{skew} + \tau_{jitter})$$

Setup Time | Clock Skew | Clock Jitter

StartPoint DFFs → EndPoint DFFs τ_{dly} and the "Cone of Logic"



$$EndDFF(T) = f(StartDFFs(T-1))$$

Signal will arrive at destination by τ_{dly}... but it will not be captured until the next clock edge

Synchronous Design Take Away Points

- Basic Blocks: DFFs and Combinatorial logic
- DFFs are boundary points
  - For each DFF (EndPoint) there is a backwards trace to start point DFFs
  - There is delay between StartPoint DFFs and endpoint DFFs
    - Combinatorial logic
    - Routes
- SEU analysis is based on utilized DFFs in a design because a functional data path upset is not an upset unless it is captured by a DFF

The question is... If an upset occurs will it reach and affect an endpoint DFF?

$$P(fs)_{error} \propto P_{Configurat\ ion} + P(fs)_{functional\ Logic} + P_{SEFI}$$

Functional Data Path SEU Cross Sections

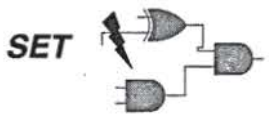
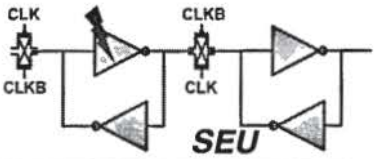
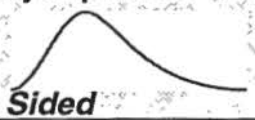
Configuration versus Data Path (Functional Logic) SEUs

- Configuration and Functional logic are separate logic
- Can be implemented with different technologies within one device
- Configuration is static and data paths are not. Requires a different test and analysis approach

This explains why there are separate categories of error:

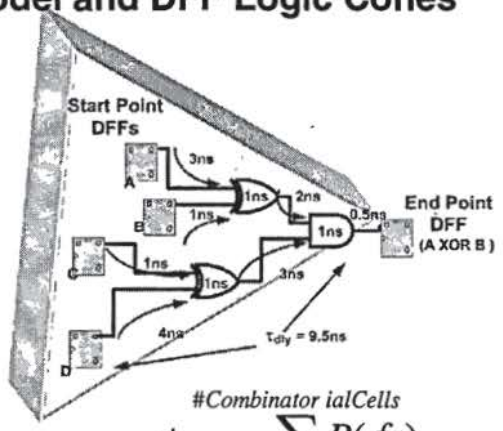
$$P_{configuration} \textbf{ vs. } P_{functionalLogic}$$

SEUs and SETs in a Data Path

Combinatorial	Sequential
Logic function generation (computation)	Captures and holds state of data input at rising edge of clock
	
SET: Glitch in the combinatorial logic: Capture is frequency dependent  Double Sided	SEU: State changes until next cycle of enabled input: Next state capture can be frequency dependent  Single Sided

Data Path Model and DFF Logic Cones

$P(fs)_{functional\ Logic}$



Evaluate for Each DFF

$$\exists_{DFF}\left(\sum_{j=1}^{\#StartPoint\ DFFs} P(fs)_{DFFSEU\rightarrow SEU(j)} + \sum_{i=1}^{\#Combinatorial\ Cells} P(fs)_{SET\rightarrow SEU(i)}\right)$$

StartPoint DFFs — Combinatorial logic

DFF_k Cone of Logic

$$P(fs)_{error} \propto P_{Configuration} + P(fs)_{functionalLogic} + P_{SEFI}$$

Functional Data Path SEU Cross Sections and Combinatorial Logic Effects (Capturing SETs)

$$P(fs)_{functional\ Logic} \propto P(fs)_{DFFSEU\rightarrow SEU} + P(fs)_{SET\rightarrow SEU}$$

SETs and a Synchronous System

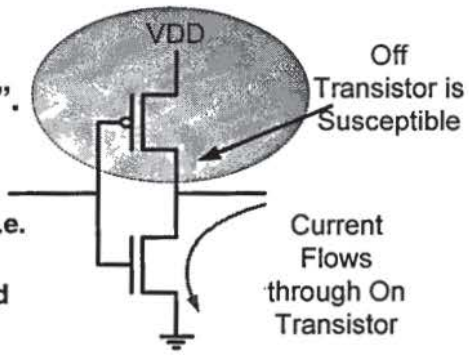
- Generation (P_{gen})
- Propagation (P_{prop})
- Logic Masking ($P_{logic.}$)
- Capture

All Components comprise:

$$P(fs)_{SET \rightarrow SEU}$$

SET Generation: P_{gen}

- SET generation occurs due to an "off" gate turning "on".
- SET has an amplitude and width (τ_{width}) based on:
  - Amount of collected charge (i.e. small LET →small SET)
  - The strength of the gate's load
  - The strength of its complimentary "ON" gate
  - The dissipation strength of the process.



Collected Charge Q_{coll} > *Critical Charge* $Qcrit$

$$Q_{crit} = C_{node} * V_{node}$$

Node Capacitance *Node Voltage*

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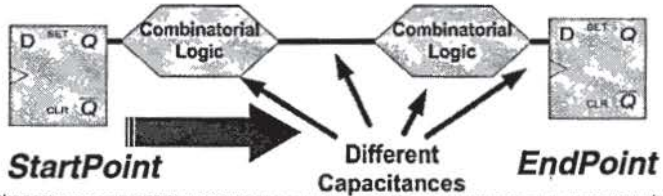
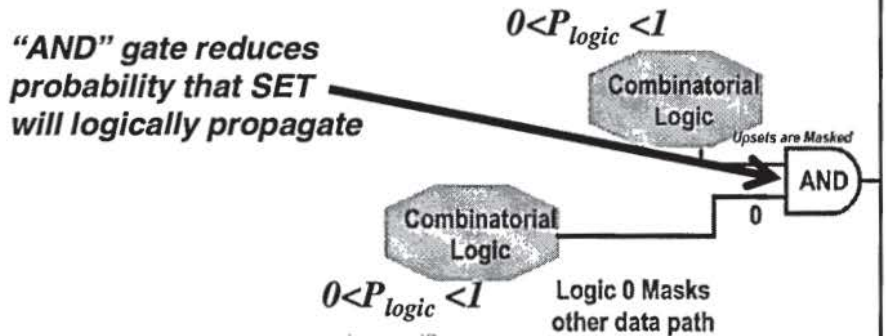
SET Propagation to an EndPoint DFF: P_{prop}

- In order for the data path SET to become an upset, it must propagate and be captured by its Endpoint DFF
- P_{prop} only pertains to electrical medium (capacitance of path… combinatorial logic and routing)
  - Capacitive SET amplitude reshaping
  - Capacitive SET width reshaping
- Small SETs or paths with high capacitance have low P_{prop}
- P_{prop} contributes to the non-linearity of $P(fs)_{SET \rightarrow SEU}$ because of the variation in path capacitance



SET Logic Masking: P_{logic}

- P_{logic}: *Probability that a SET can logically propagate through a cone of logic. Based on state of the combinatorial logic gates and their potential masking.*



Determining P_{logic} for a complex system can be very difficult

SET Capture at Destination DFF

The transient width (τ_{width}) will be a fraction of the clock period (τ_{clk}) for a synchronous design in a CMOS process.

$$P(\tau_{clk})_{SET \rightarrow SEU} \propto \frac{\tau_{width}}{\tau_{clk}}$$

$$P(fs)_{SET \rightarrow SEU} \propto \tau_{width} fs$$

Probability of capture is proportional to the width of the transient as seen from the destination DFF

Data Path Model and Combinatorial Logic SETs

$$\sum_{i=1}^{\#CombinatorialCells} P(fs)_{SET \rightarrow SEU(i)} \propto \sum_{i=1}^{\#CombinatorialCells} P_{gen(i)} P_{prop(i)} P_{logic(i)} \tau_{width(i)} fs$$

$$< \sum_{i=1}^{\#CombinatorialCells} P_{gen(i)} P_{prop(i)} \tau_{width(i)} fs$$

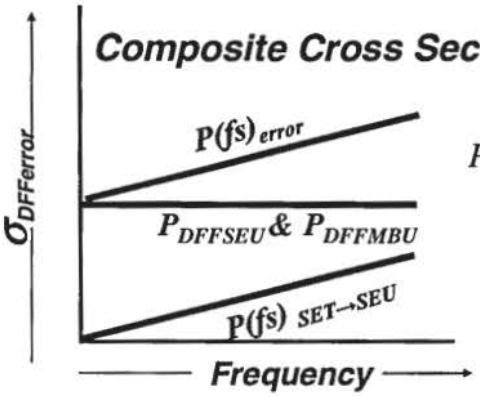
Upper Bound SET P_{logic}=1

$$P(fs)_{error} \propto P_{Configuration} + P(fs)_{functionalLogic} + P_{SEFI}$$

Functional Data Path SEU Cross Sections and DFF Effects (Capturing StartPoint SEUs)

$$P(fs)_{functional\,Logic} \propto P(fs)_{DFFSEU \rightarrow SEU} + P(fs)_{SET \rightarrow SEU}$$

Conventional Theory: System Upsets Have a Static Component+Dynamic Component



$$P(fs)_{error} = P_{DFFSEU} + P(fs)_{SET \rightarrow SEU}$$

Takes into account upsets from combinatorial logic in DFF data path and the DFF potential for flipping its state

Does not fully characterize DFF upsets as they pertain to a synchronous system

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StartPoint SEUs and a Synchronous System: New Stuff

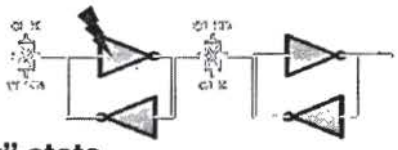
- Generation (P_{DFFSEU})
- P_{prop}=1 for hard state switch
- Logic Masking ($P_{logic.}$)
- Capture

All Components comprise:

$$P(fs)_{DFFSEU \rightarrow SEU}$$

Generation of DFF Upsets: P_{DFFSEU}

- Probability that a DFF will flip its state
- Can be a hard flip:
  - Will not change until the next clock cycle
  - Amplitude and width are not affected as with a SET
- Can be a metastable flip
  - No real defined state
  - Otherwise known as a "weak" state
  - Can cause oscillations in the data path



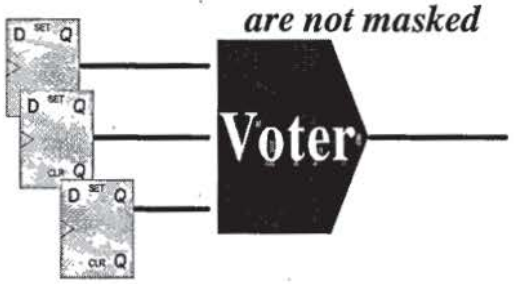
Generation P_{DFFSEU} versus Capture $P(fs)_{DFFSEU \rightarrow SEU}$

P_{DFFSEU}	$P(fs)_{DFFSEU \rightarrow SEU}$
Probability a StartPoint DFF becomes upset	Probability that the StartPoint upset is captured by the endpoint DFF
Occurs at some point in time within a clock period	Occurs at a clock edge (capture)
Not frequency dependent	Frequency dependent

Logic Masking DFFs... P_{logic}

- **Logic masking for DFF StartPoints is similar to logic masking of combinatorial logic.**
- **DFF logic masking is generally the point where Triple Modular Redundancy (TMR) is inserted**

$P_{logic}>0$ *for Voter... its upsets are not masked*



$P_{logic}=0$ *for DFFs... their upsets are masked*

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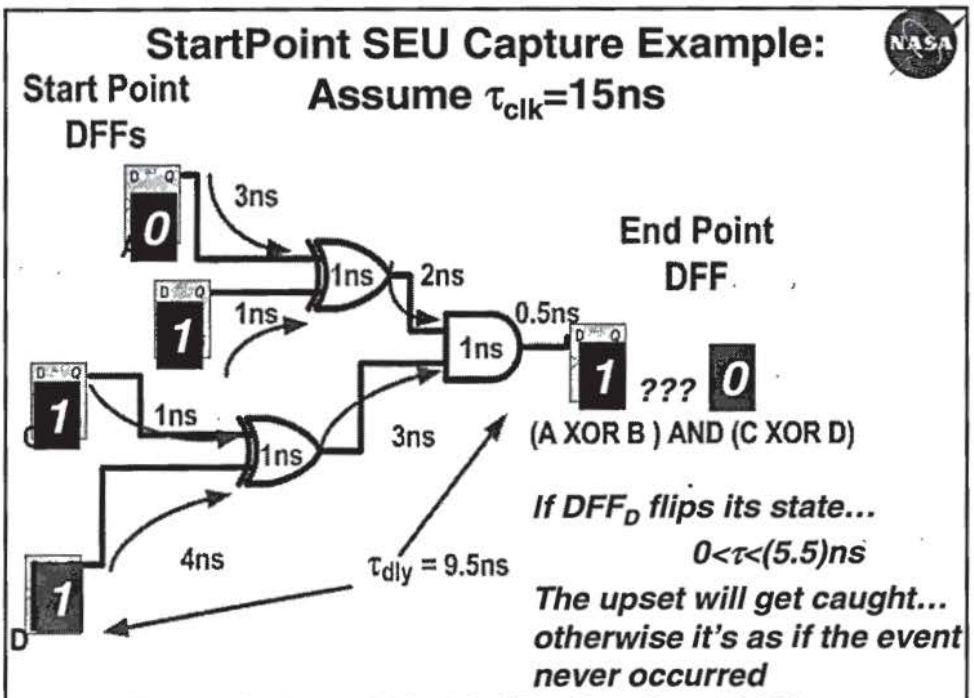
StartPoint SEU Capture Example:



Percentage of Clock Cycle for SEU Capture:

$$\tau < \tau_{clk} - \tau_{dly}$$

Upset is caught within this timeframe

$$\frac{\tau}{\tau_{clk}} < \frac{\tau_{clk} - \tau_{dly}}{\tau_{clk}} = 1 - \frac{\tau_{dly}}{\tau_{clk}}$$

Fraction of clock period for upset capture

$$\tau \ fs < 1 - \tau_{dly} \ fs$$

upset capture with respect to to frequency

Data Path Upsets and StartPoint DFFs

$$\sum_{j=1}^{\#StartPoint\ DFFs} P(fs)_{DFFSEU \rightarrow SEU(j)} \propto \sum_{j=1}^{\#StartPoint\ DFFs} P_{DFFSEU(j)} P_{\log ic(j)} (1-\tau_{dly(j)} fs)$$

$$< \sum_{j=1}^{\#StartPoint\ DFFs} P_{DFFSEU(j)} (1-\tau_{dly(j)} fs)$$

$$< \sum_{j=1}^{\#StartPoint\ DFFs} P_{DFFSEU(j)}$$

$P(fs)_{FunctionalLogic}$ Putting it all together:

$$P(fs)_{functionalLogic} \propto P(fs)_{DFFSEU \rightarrow SEU} + P(fs)_{SET \rightarrow SEU}$$

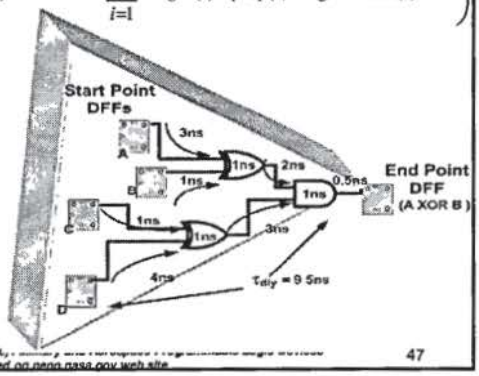
Data Path Upsets — ***StartPoint DFF SEU capture*** — ***Combinatorial Logic SET capture***

NASA REAG FPGA Data Path Functional Logic Susceptibility Model

$$P(fs)_{functionalLogic}$$

$$\exists_{DFF}\left(P(fs)_{DFFSEU \rightarrow SEU} + P(fs)_{SET \rightarrow SEU}\right)$$

$$\exists_{DFF}\left(\left(\sum_{j=1}^{\#StartPoint\,DFFs} P_{DFFSEU(j)}(1-\tau_{dly(j)}fs)P_{logic(j)}\right) + \sum_{i=1}^{\#CombinatorialCells}\left(P_{gen(i)}P_{prop(i)}P_{logic}\tau_{width(i)}fs\right)\right)$$



NASA REAG FPGA Upper Bound Susceptibility Model

$$\exists_{DFF}\left(\left(\sum_{j=1}^{\#StartPoint\,DFFs} P_{DFFSEU(j)}(1-\tau_{dly(j)}fs)P_{logic(j)}\right) + \sum_{i=1}^{\#CombinatorialCells}\left(P_{gen(i)}P_{prop(i)}P_{logic}\tau_{width(i)}fs\right)\right)$$

Upper-bound assumes P_{logic}=1 (no mitigation) and NO DFF frequency (fs) dependency

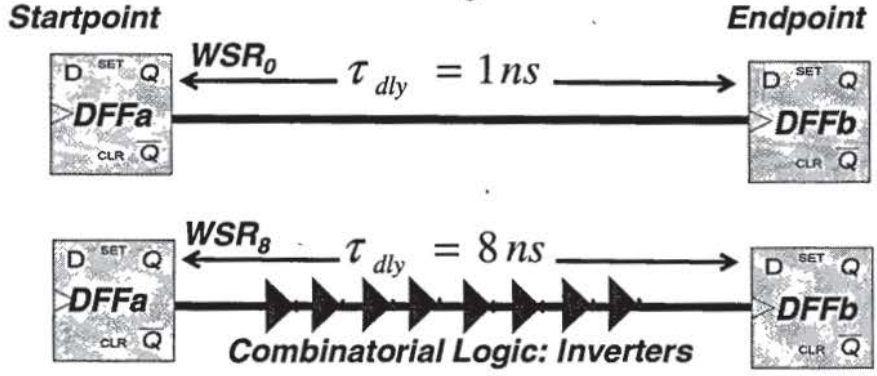
$$\exists_{DFF}\left(\sum_{j=1}^{\#StartPoint\,DFFs} P_{DFFSEU} + \sum_{i=1}^{\#CombinatorialCells}\left(P_{gen(i)}P_{prop(i)}\tau_{width(i)}fs\right)\right)$$

How DFF or Combinatorial Logic Dominance Affects σ_{SEU}

	$P(fs)_{DFFSEU \rightarrow SEU}$	$P(fs)_{SET \rightarrow SEU}$
Logic	DFF Capture	Combinatorial SET Capture
Capture percentage of clock period	$(1-\frac{\tau_{dly}}{\tau_{clk}}) = (1-\tau_{dly} fs)$	$\frac{\tau_{width}}{\tau_{clk}} = \tau_{width} \ fs$
Frequency Dependency	Increase Frequency decrease σ_{SEU}	Increase Frequency increase σ_{SEU}
Combinatorial Logic Effects	Increase Combinatorial logic increases τ_{dly} and decreases σ_{SEU}	Increase in combinatorial logic increases P_{gen} and increases σ_{SEU}

To be presented by Melanie Berg at the Revolutionary Electronics in Space (ReSpace) / Military and Aerospace Programmable Logic Devices (MAPLD) 2011 Conference, Albuquerque, NM, August 22-25, 2011, and to be published on nepp.nasa.gov web site. 49

Which String Would You Expect to Have a Higher SEU Cross Section? WSR_0 or WSR_8



You can't answer the question until you understand the relative σ_{SEU} contribution of DFFs to Combinatorial Logic... Is there Logic Mitigation?

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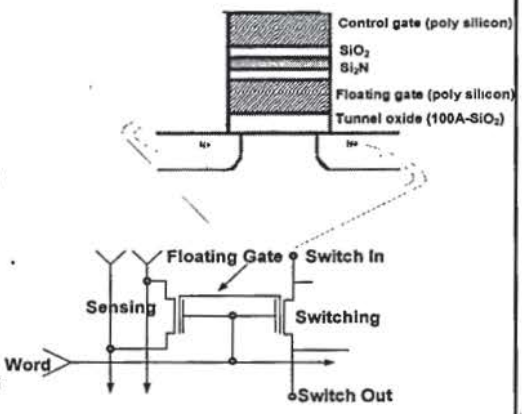
NASA REAG Models + Heavy Ion Data: ProASIC3

Background: Micro-Semi (Actel) ProASIC3 Flash Based FPGA

- Originally a commercial device
- Configuration is flash based and has proven to be almost immune to SEUs
- No embedded mitigation in device
- Evaluation of user mitigation insertion has been performed



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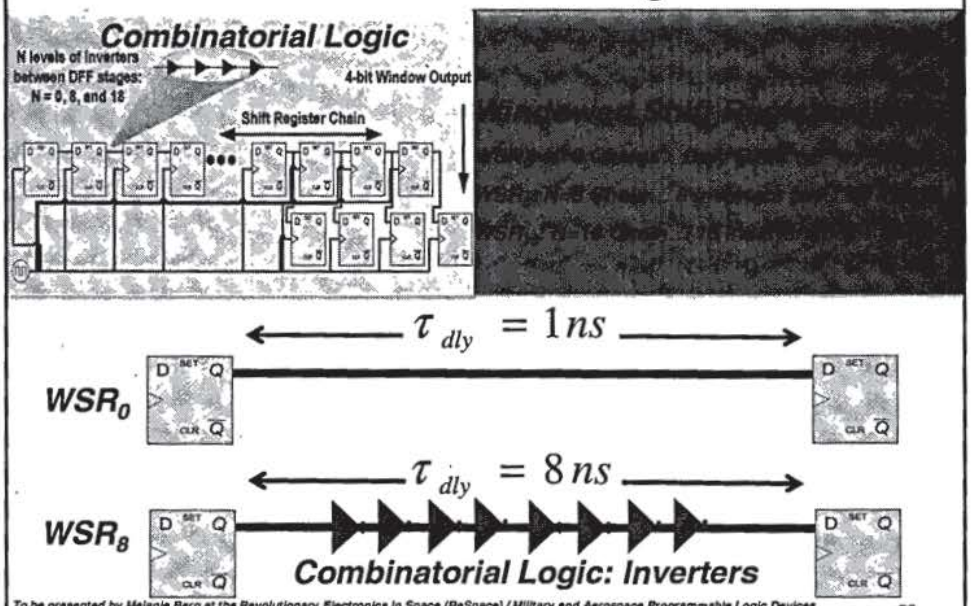
Testing Combinatorial Logic Contributions to SEU Cross-Sections: Shift Registers



Actel ProASIC3 Shift Register Study

- **Shift Register Functional Logic Designs Under Test:**
  - **Six WSR strings with various levels of combinatorial logic**

$$P(fs)_{error} \propto P_{Configuration} + P(fs)_{functionalLogic} + P_{SEFI}$$

$$\exists_{DFF}\left(P(fs)_{DFFSEU \rightarrow SEU} + \sum_{i=0}^{\#Inverters} P(fs)_{SET \rightarrow SEU\,(i)} \right)$$

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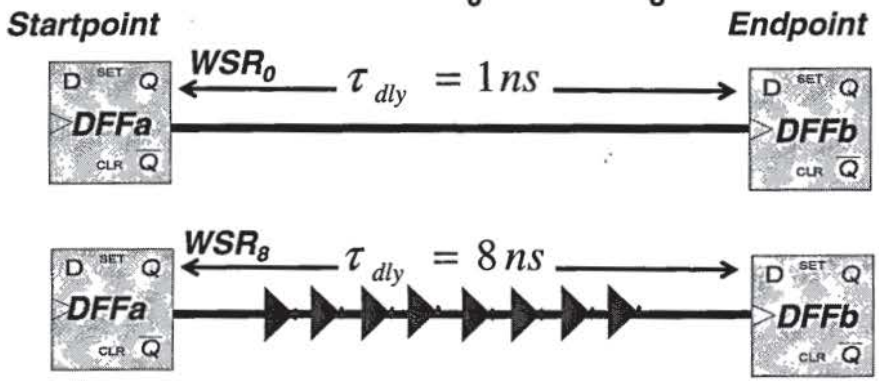
ProASIC3: Which String Would You Expect to Have a Higher SEU Cross Section? WSR_0 or WSR_8



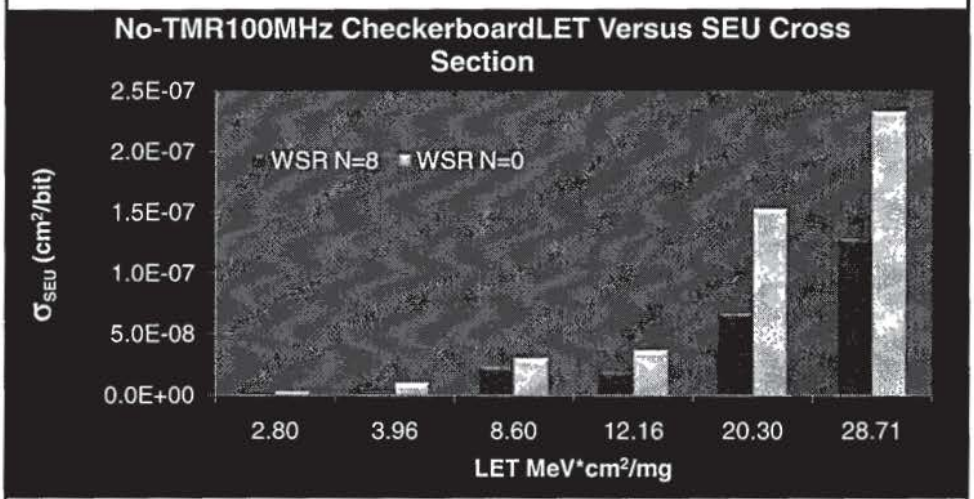
If the DFFs are not mitigated they will have the dominant σ_{SEU}

$\sigma_{SEU} \propto (1-\tau_{dly} fs)$: σ_{SEU} is inversely proportional to τ_{dly}

σ_{SEU} WSR_0 > σ_{SEU} WSR_8

σ_{SEU} Test Results: Windowed Shift Registers (WSRs) No-TMR

- *No Mitigation: σ_{SEU} WSR_0 > σ_{SEU} WSR_8 For every LET*



Agenda(First Half)

- Section I: Single Event Effects in Digital Logic
- Section II: Application of the NASA Goddard Radiation Effects and Analysis Group (REAG) FPGA SEU Model
- **Section III: Reducing System Error: Common Mitigation Techniques**
  - **Triple Modular Redundancy (TMR)**
  - **Embedded RHBD**

Example: TMR Mitigation Schemes will use Majority Voting

$$MajorityVoter = I1 \wedge I2 + I0 \wedge I2 + I0 \wedge I1$$

I0	I1	I2	Majority Voter
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Best 2 out of 3

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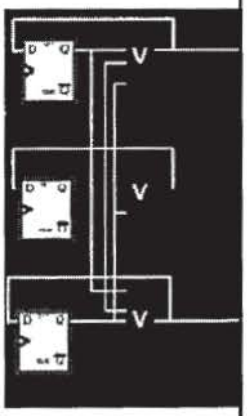
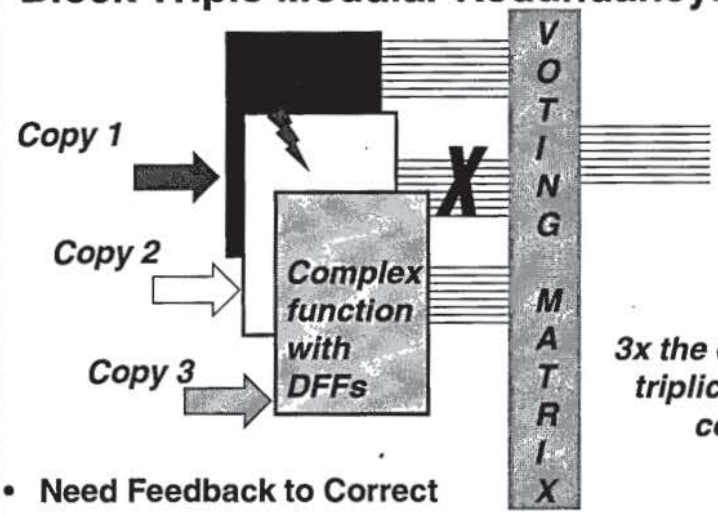
TMR: Correction vs Masking

- TMR with feedback will correct an error
- TMR with no feedback will mask an error
  - May not buy you anything if a large amount of circuitry has no correction capability
  - Triple the circuitry without correction:
    - triples the upset rate
    - may end up with the same upset rate using this scheme

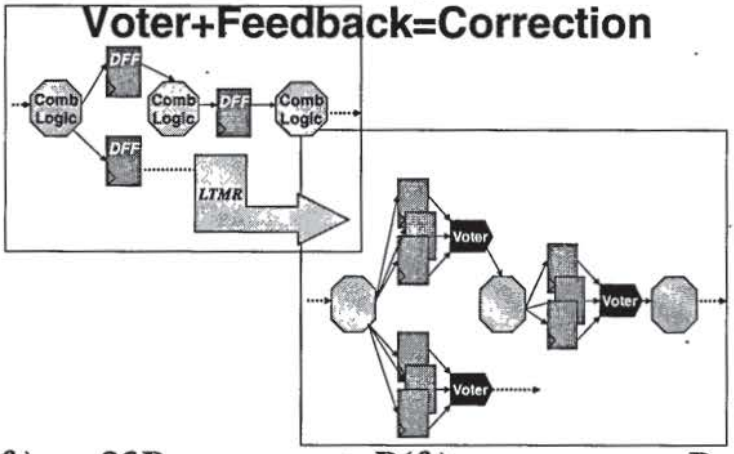


Block Triple Modular Redundancy: BTMR



- Need Feedback to Correct
- Generally can not apply internal correction from voted outputs
- Errors can accumulate – not an effective technique

Local Triple Modular Redundancy (LTMR): Only DFFs Voter+Feedback=Correction



$$P(f_s)_{error} \propto P_{configuration} + P(f_s)_{functionalLogic} + P_{SEFI}$$

$$P(fs)_{DFFSEU \rightarrow SEU} + P(f_s)_{SET \rightarrow SEU}$$

0

ProASIC3 LTMR Shift Register Data Path Model

$$\exists_{DFF}\left(\sum_{j=1}^{\#StartPoint\,DFFs} P(fs)_{DFFSEU \rightarrow SEU(j)} + \sum_{i=1}^{\#CombinatorialLogicGates} P(fs)_{SET \rightarrow SEU(i)} \right)$$

LTMR: $P_{logic}=0$

$$\exists_{DFF}\left(P(fs)_{DFFSEU \rightarrow SEU} + \sum_{i=1}^{\#CombinatorialLogicGates} P(fs)_{SET \rightarrow SEU(i)} \right)$$

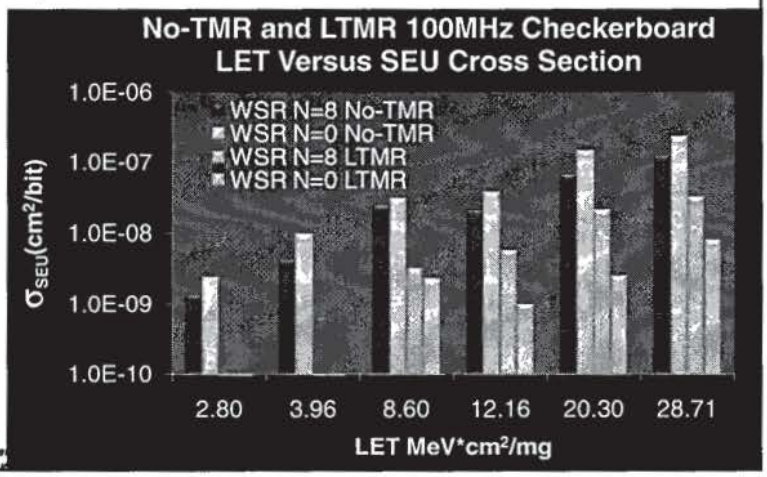
$$\sum_{i=1}^{\#CombinatorialLogicGates} P(fs)_{SET \rightarrow SEU(i)} \propto P_{gen(i)} P_{prop(i)} P_{logic} \tau_{width(i)} fs$$

As we increase #combinatorial logic gates we increase σ_{SEU}

Hence for LTMR (disregarding P_{prop}), $\sigma_{SEU} WSR_8 > \sigma_{SEU} WSR_0$

σ_{SEU} Test Results: Windowed Shift Registers (WSRs) No-TMR versus TMR

- LTMR is effective and has reduced P_{DFFSEU}
- *LTMR: SEU cross Sections $WSR_0 < WSR_8$ For every LET*



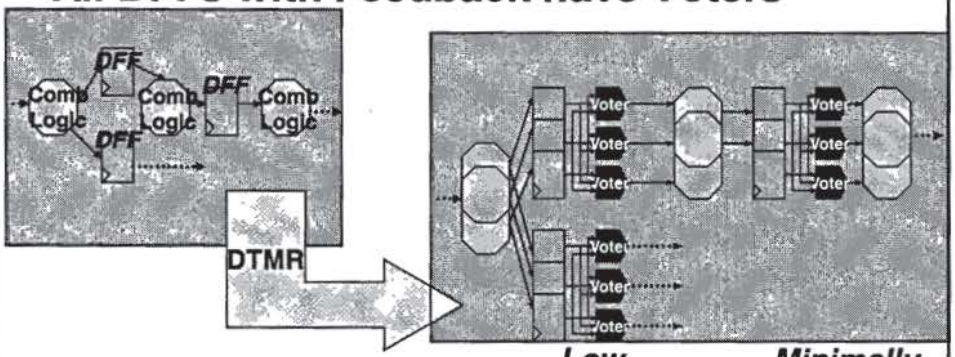
No-TMR vs. LTMR: Combinatorial Logic Effects

	No-TMR ProASIC3	LTMR ProASIC3
Significant circuit type	StartPoint DFF (sequential): SEU capture	Combinatorial: SET capture
Significant Model component	$P_{DFFSEU}(1-\tau_{dly}fs)$	$P_{gen}P_{prop}\tau_{width}fs$
Error Type	One sided function	Two-sided function
σ_{SEU} WSR8 vs. σ_{SEU} WSR0	σ_{SEU} WSR_8 < σ_{SEU} WSR_0	σ_{SEU} WSR_8 > σ_{SEU} WSR_0
Relative σ_{SEU} reasoning	WSR8 has more combinatorial Logic and more τ_{dly} between DFFs	WSR8 has more combinatorial Logic and has more opportunity for SET generation

No-TMR vs. LTMR: Frequency Effects

- The same reasoning as tdly can be used for Frequency
- No-TMR:
  - Inverse relationship to frequency: $P_{DFFSEU}(1-\tau_{dly}fs)$
  - Increase Frequency Decrease σ_{SEU}
- LTMR
  - Direct relationship to frequency: $P_{gen}P_{prop}\tau_{width}fs$
  - Increase Frequency increase σ_{SEU}

Distributed Triple Modular Redundancy (DTMR): DFFs + Data Paths All DFFs with Feedback have Voters



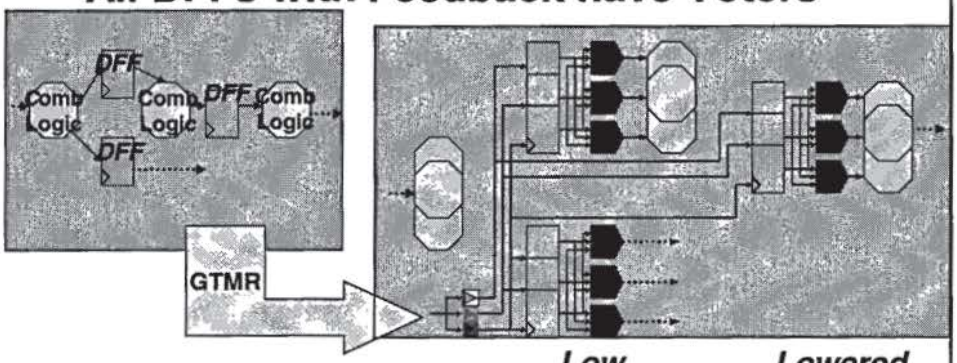
$$P(f_s)_{error} \propto P_{configuration} + P(f_s)_{FunctionalLogic} + P_{SET}$$

Low — Minimally Lowered

$$P(fs)_{DFFSEU \rightarrow SEU} + P(f_s)_{SET \rightarrow SEU}$$

0 — Low

Global Triple Modular Redundancy (GTMR):DFFs + Data Paths + Global Routes All DFFs with Feedback have Voters



$$P(f_s)_{error} \propto P_{configuration} + P(f_s)_{functionalLogic} + P_{SEFI}$$

Low Lowered

$$P(fs)_{DFF\,SEU \rightarrow SEU} + P(f_s)_{RESET \rightarrow SEU}$$

Low Low

GTMR Proves To be A Great Mitigation Strategy... BUT...

- Triplicating a design and its global routes takes up a lot of power and area
- Generally performed after synthesis by a tool– not part of RTL
- Difficult to verify
- Does the FPGA contain enough low skew clock trees? (each clock + its synchronized reset)x3

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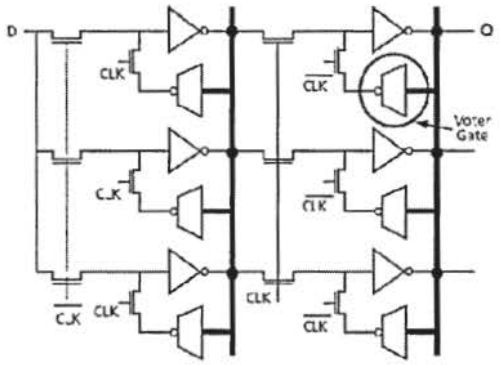
  - Triple Modular Redundancy
  - Embedded RHBD
- Section IV: When Your Mitigation Fails
- Section V: Xilinx V4
- Section VI: Fail-Safe Strategies

DFF with Embedded LTMR: Microsemi (Actel) RTAXs Family of FPGA

- Localized (only at DFF)
- Microsemi uses Wired "OR" approach to voting – no SETs on voters



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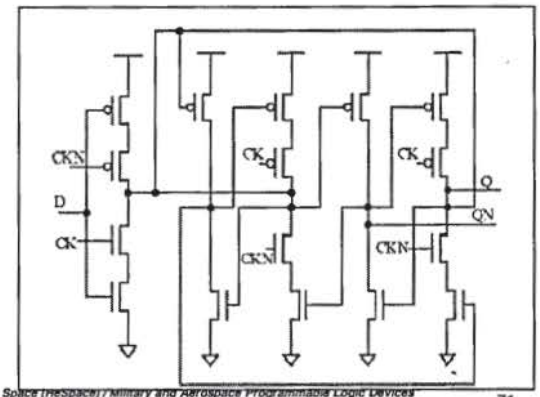
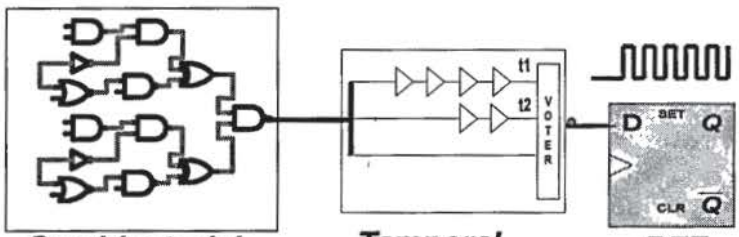
DFF with Embedded Dual Interlock Cell (DICE): Aeroflex Eclipse FPGA

- Uses a Dual Redundancy Scheme instead of LTMR
- Single nodes can become upset but their partner node will pull the output in the correct direction



Embedded Temporal Redundancy (TR): SET Filtration

- Temporal Filter placed directly before DFF
- Localized scheme that reduces SET capture
- Delays must be well controlled. FPGA designers should not implement– best if embedded
- Maximum Clock frequency is reduced by the amount of new delay



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Combining Embedded Schemes

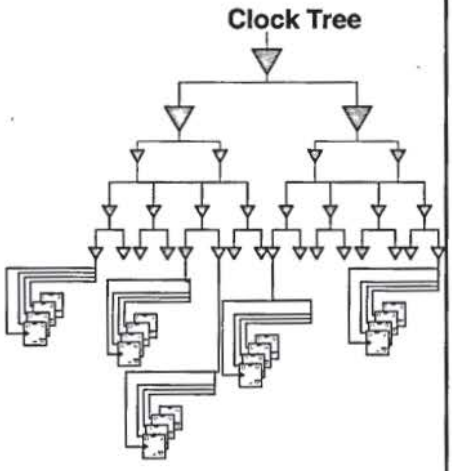
- Some Radiation Hardened by Design (RHBD) schemes combine embedded temporal redundancy with localized redundant latches:
  - TR+LTMR
  - TR+DICE
- New Xilinx RHBD FPGA (Virtex 5QV) has embedded TR+DICE

$$P(f_s)_{error} \propto P_{configuration} + P(f_s)_{functionalLogic}^{Low} + P_{SEFI}$$

$$P(fs)_{DFFSEU \rightarrow SEU}^{Low} + P(f_s)_{SET \rightarrow SEU}^{Lowered}$$

RHBD for Global Routes

- Many RH FPGAs contain hardened clock trees and other global routes
- Global structures are generally hardened by using larger buffers
- TR will not work on a global network (signal integrity, skew balancing, speed and area would be significantly affected)



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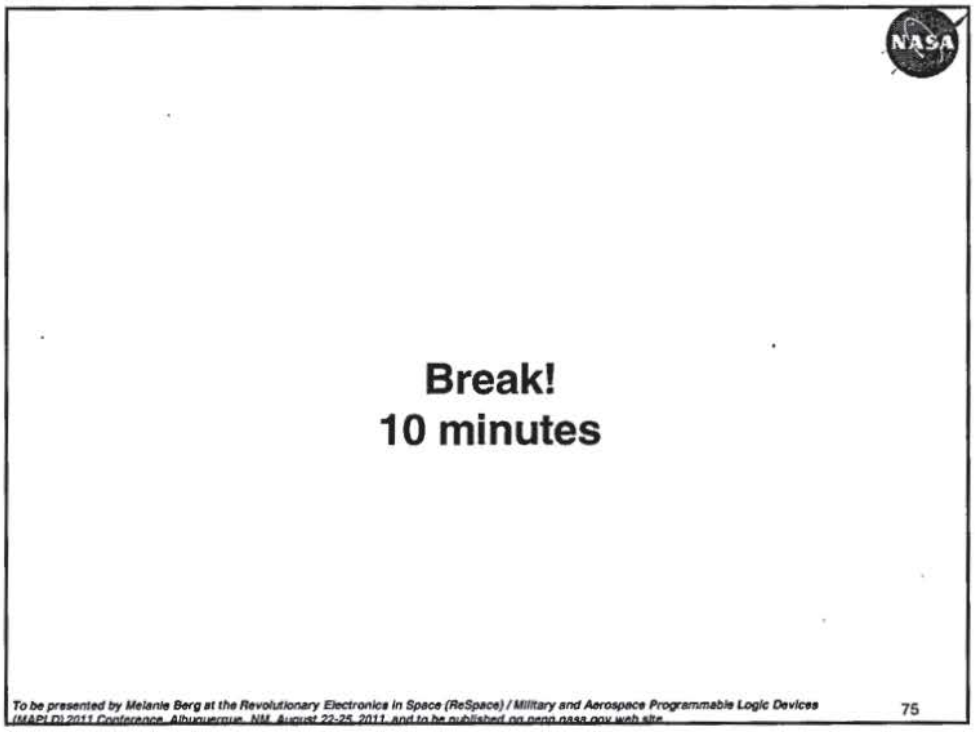
Break!
10 minutes
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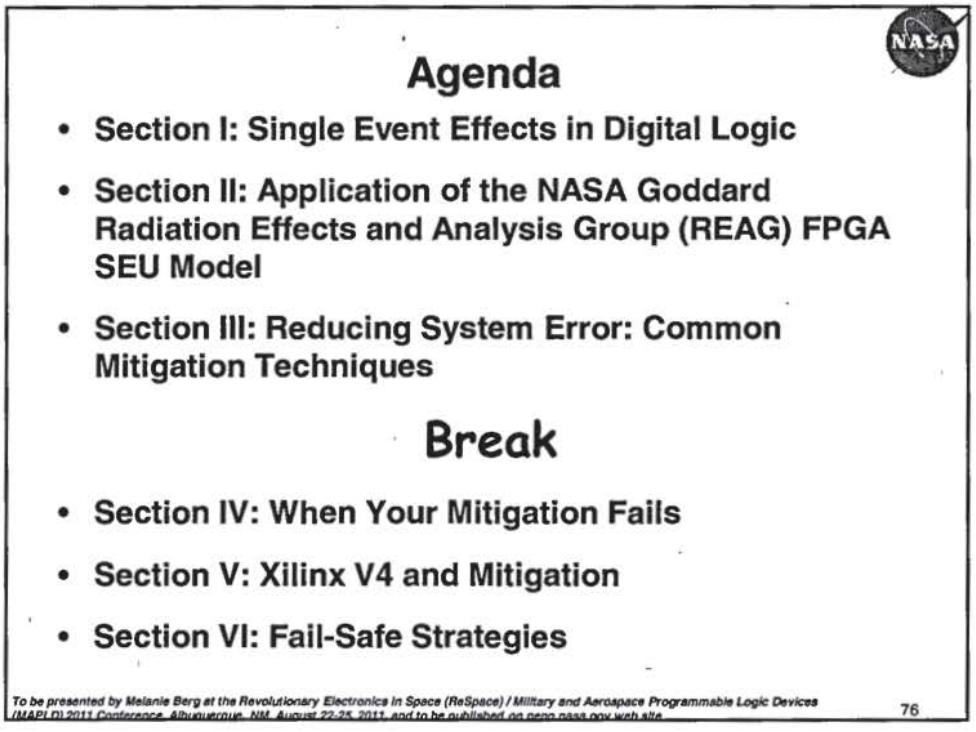
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Break
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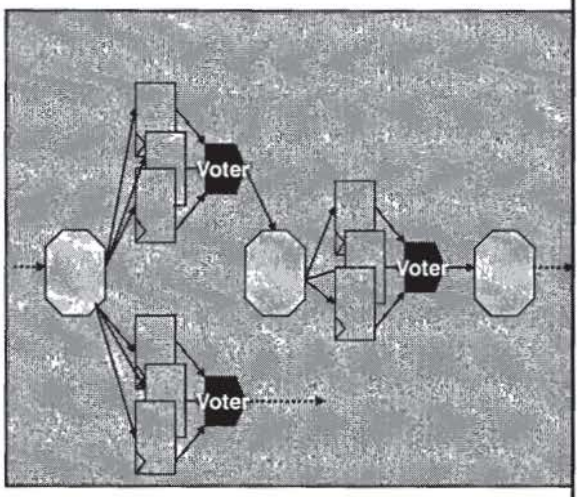
Agenda (Second Half)

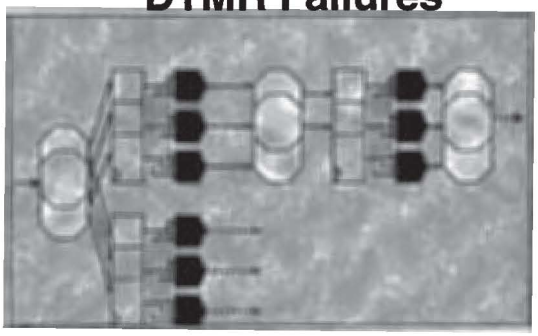
- **Section III: When Your Mitigation Fails**
- **Section V: Xilinx V4 and Mitigation Strategies**
- **Section VI: Fail-Safe Strategies**

LTMR Failure

- **Shared Data Path into DFFS**
- **Voters can upset**
- **Global routes**

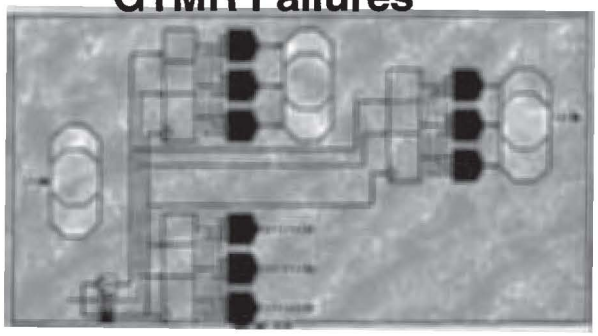


DTMR Failures



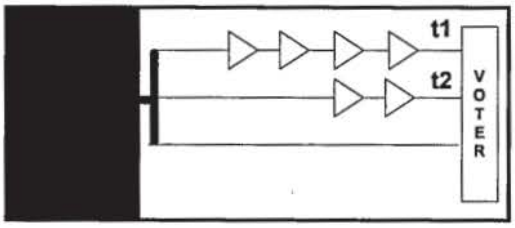
- Global routes
- Domain placement
  - possible for domains to share common routing matrix
  - Hit to shared routing matrix can take out two domains

GTMR Failures



- Domain placement
  - possible for domains to share common routing matrix
  - Hit to shared routing matrix can take out two domains
- Clock Skew
- Asynchronous clock domain crossings need additional voter insertion – tools don't auto handle

TR Failures



Temporal Filtering

Narrow SETs: No overlap

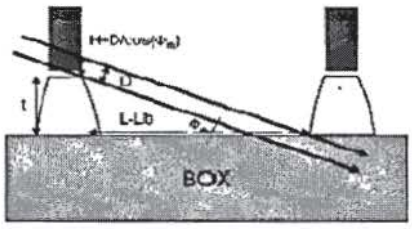
Wide SETs: Overlap

DICE Susceptibility

- **One particle strike can take out 2 nodes and break Dice**

–Source: "Radiation Hard by Design at 90nm" ; Warren Snapp et. al, MRQW December 2008

Minimum spaced DICE flip flop
(lines show critical node)



Multiple bit upset ion strike simplified geometric model

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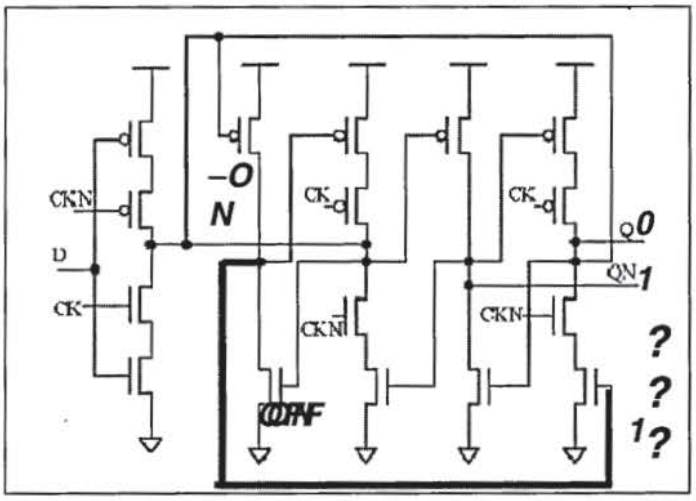
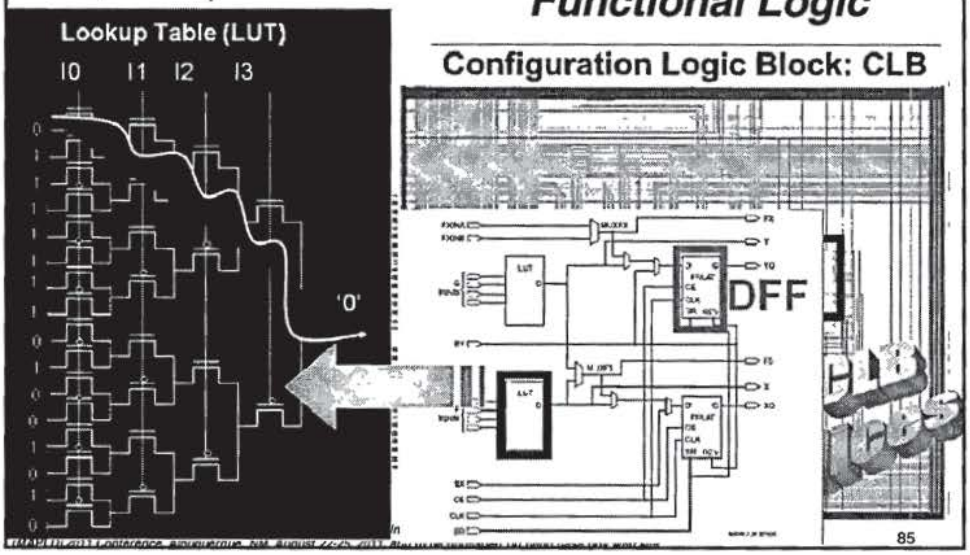
DICE Susceptibility



Agenda (Second Half)

- Section III: When Your Mitigation Fails
- **Section V: Xilinx V4 and Mitigation Strategies**
- Section VI: Fail-Safe Strategies

General Xilinx Virtex 4 FPGA Architecture



Xilinx SX55: Radiation Test Data

Xilinx Consortium: ***VIRTEX-4VQ STATIC SEU CHARACTERIZATION SUMMARY: April/2008***

	Probability	Error Rate	LEO $\frac{Upsets}{device-day}$	GEO $\frac{Upsets}{device-day}$
Configuration Memory: XQR4VSX55	$P_{configuration}$	$\frac{dE_{configuration}}{dt}$	**7.43**	**4.2**
Combined SEFIs per device	P_{SEFI}	$\frac{dE_{SEFI}}{dt}$	**7.5×10^{-5}**	**2.7×10^{-5}**

- **For non-mitigated designs the most significant upset factor is:**

$$P_{Configuration}$$

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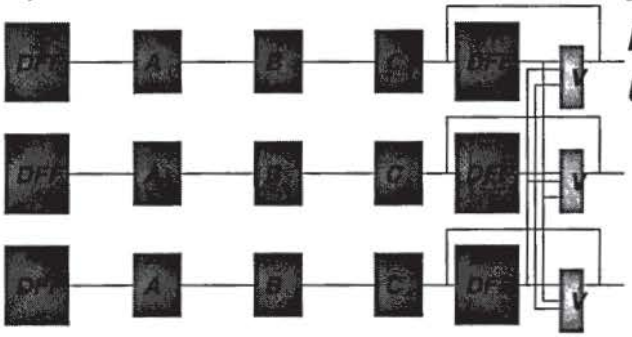
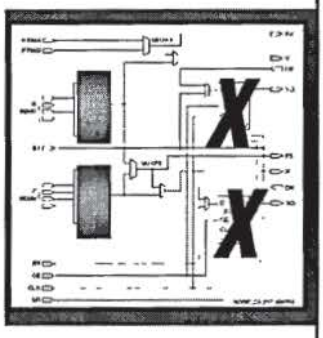
Because $P_{configuration}$ is Dominant, Use XTMR (also known as GTMR) for Critical Applications



How does XTMR affect resource utilization?

Predicting Available Resources after XTMR Insertion

- **Goal: Determine how many devices are required to implement design after XTMR insertion**
- **Because of mapping... not as much room as you think**



- **Check project FPGA maximum capacity requirements (usually 80% to 90%) of device**
- $1.2 \times 4.5 \times DFF_{unmitigated} < DFF_{datasheet}$

Xilinx V4 Takeaway Points

- Can be used in non-critical missions without any mitigation
  - Upset rates in the order of days
  - Will need to be reconfigured periodically
  - Watchdog required
  - Great for non-critical data processing
- Can be used in a critical path (beware of SEFIs) with mitigation
  - Utilize mitigation tools from a proven vendor, otherwise:
    - Design may break after GTMR (XTMR) insertion
    - Mitigation may not be placed where expected
  - Upset rates are extremely low

Agenda (Second Half)

- Section III: When Your Mitigation Fails
- Section V: Xilinx V4 and Mitigation Strategies
- **Section VI: Fail-Safe Strategies**

How Safe is Your Design?

- Understand the SEU error mode specifics?
- Are there lock-up conditions in my design?
- Does your strategy protect the entire critical path?
- Is the synthesized design fail-safe?
- Did you mitigate where you expected to mitigate?
- Can your watch-dog catch failure?
- Will your recovery scheme work?
- What are the limitations of your verification strategy?

The list goes on... Based on error signatures of the target FPGA, the designer must keep all points in mind at all stages of the design

Conclusion

- Understand the device's error signatures and upset rates before mitigation is implemented
- Not all designs are critical and may not need mitigation
- Be aware when correction is necessary:
  - Make sure you are correcting your state
  - Masking without correction can incur error accumulation and eventually break
- Detection circuits don't generally have redundancy and can be susceptible – make sure they are not making your design more susceptible (e.g. state machines)
- Perform proper trade studies to determine the type of mitigation necessary to meet requirements:
  - Upset rates
  - Area+Power
  - Complexity... completion and verification with time specified

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