Optimizing Mitigation Strategies for FPGA Critical Applications

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What's the Issue?

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If something goes wrong...

Increasing number of FPGA devices inserted into space missions

Harsh Space Radiation Environment

To be presented by Melanie Berg at the ReSpace/MAPLD 2010 Conference [Military and Aerospace Programmable Logic Devices (MAPLD)], November 1-4, 2010 in Albuquerque, NM, and on http://radhome.gsfc.nasa.gov and http://nepp.nasa.gov/.

We Can't Always do This...

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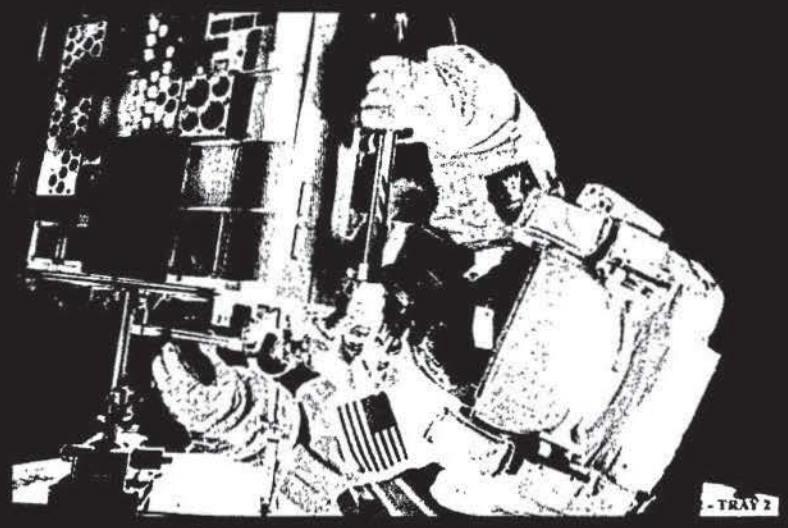

Agenda

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- **Section I:** Single Event Effects in Digital Logic
- **Section II:** FPGA Basics – Architectural Differences
- **Section III:** Reducing System Error: Common Mitigation Techniques
  - Triple Modular Redundancy:
    - Block Triple Modular Redundancy (BTMR)
    - Local Triple Modular Redundancy (LTMR)
    - Global Triple Modular Redundancy (GTMR)
- **Section IV:** The Automation Process and the Mentor Graphics Advantage

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Section I: Single Event Effects in Digital Logic

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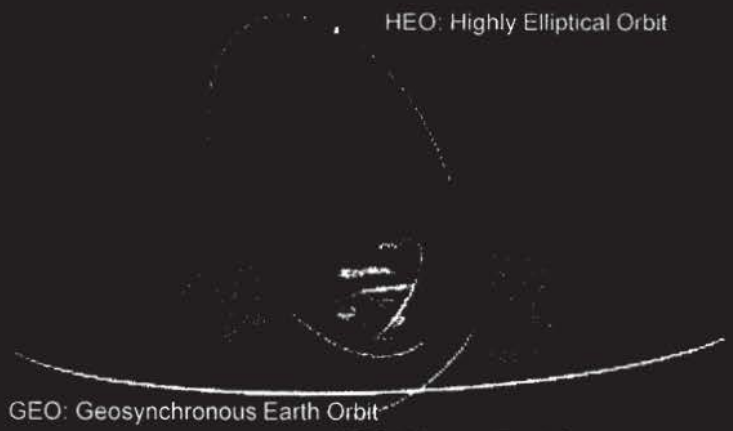

Source of Faults: SEEs and Ionizing Particles

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- Single Event Effects (SEEs)
  - Terrestrial devices are susceptible to faults mostly due to:
    - **alpha particles**: from packaging and doping and
    - **Neutrons**: caused by Galactic Cosmic Ray (GCR) Interactions that enter into the earth's atmosphere.

Energy emitted from an atom or nucleus in the form of waves or particles

- Devices expected to operate at higher altitude (Aerospace and Military) are more prone to upsets caused by:
  - **Heavy ions**: direct ionization
  - **Protons**: secondary effects

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Device Penetration of Heavy Ions and Linear Energy Transfer (LET)

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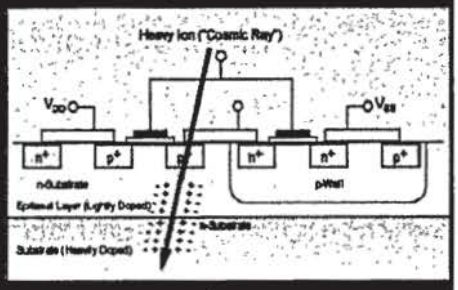
- LET characterizes the deposition of charged particles
- Based on Average energy loss per unit path length (stopping power)
- Mass is used to normalize LET to the target material



Average energy deposited per unit path length

Units

Density of target material

LET vs. Error Cross Section Graph

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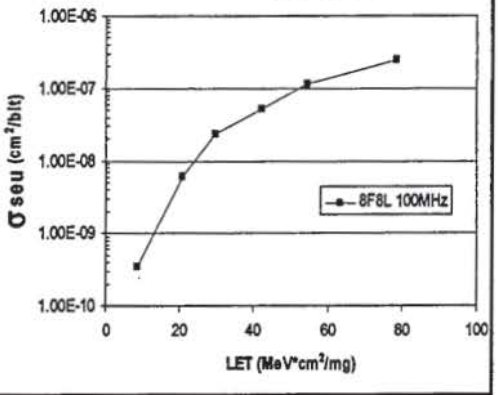
Error Cross Sections are calculated per LET value in order to characterize the number of potential faults and error rates in the space environment

Terminology:

- Flux: Particles/(sec-cm^2)
- Fluence: Particles/cm^2
- Error cross section(σ): #errors normalized by fluence
- Error cross section is calculated at several LET values (particle spectrum)

LET vs. σ:

$$\sigma_{seu} = \frac{\#errors}{fluence}$$



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Single Event Faults and Common Terminology

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- Single Event Latch Up (**SEL**): Device latches in high current state
- Single Event Burnout (**SEB**): Device draws high current and burns out
- Single Event Gate Rupture: (**SEGR**): Gate destroyed typically in power MOSFETs
- **Single Event Transient** (SET): current spike due to ionization. Dissipates through bulk
- **Single Event Upset** (SEU): transient is caught by a memory element
- **Single Event Functional Interrupt** (SEFI) - upset disrupts function

Single Event Effects (SEEs) and IC System Error

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- **SEUs or SETs can occur in:**
  - Combinatorial Logic (including global routes)
  - Sequential Logic
  - Memory Cells
- Depending on the Device and the design, each fault type will:
  - Have a probability of occurrence
  - Either have a significant or insignificant contribution to system error

Every Device has different Error Responses – We must understand the differences and design appropriately

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Radiation Induced Fault Generation

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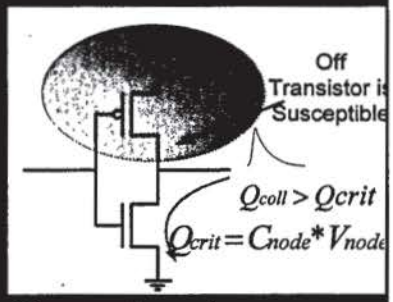
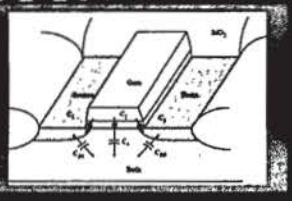
- SETs can vary in pulse width (T_{pulse}) and amplitude.
- Different FPGA processes and geometries will have different sensitivities



CAPACITANCE

- Geometry of Transistors
- Loading of Transistors
- Length of Routes
- Switching Rates

Transistor Cutoff frequencies



Each capacitance has its own f_c

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Section II: FPGA Basics – Architectural Differences

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FPGA Configuration

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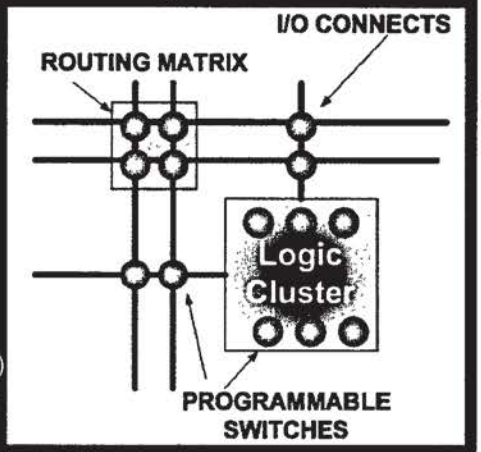
HDL → FPGA MAPPING → Configuration

- **Configuration Defines:** Arrangement of pre-existing logic via programmable switches
  - Functionality (logic cluster)
  - Connectivity (routes)
- Programming Switch Types:
  - **Antifuse:** One time Programmable (OTP)
  - **SRAM:** Reprogrammable (RP)
  - **Flash:** Reprogrammable (RP)



Antifuse FPGA Devices

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- Currently the most widely employed FPGA Devices within space applications
- Configuration is hardened due to fuse based technology (Metal to Metal)
- Localized (@ DFF node) Mitigation (TMR or DICE) is employed
- Clock and Reset lines are hardened

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ACTEL RTAX-S Architecture Basics

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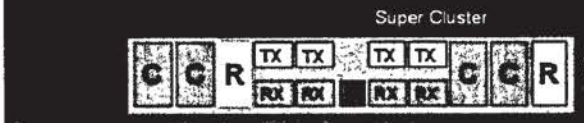

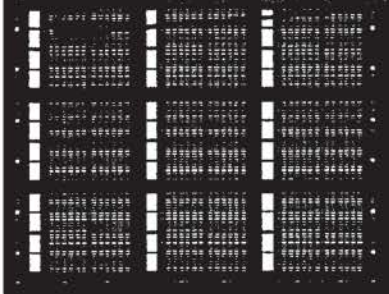

Super Cluster:
- Combinatorial Cells: C CELLS
- DFF Cells: R Cells

Source: RTAX-S/SL RadTolerant FPGAs 2009 Actel.com

ACTEL RTAX-S Combinatorial and Sequential Logic

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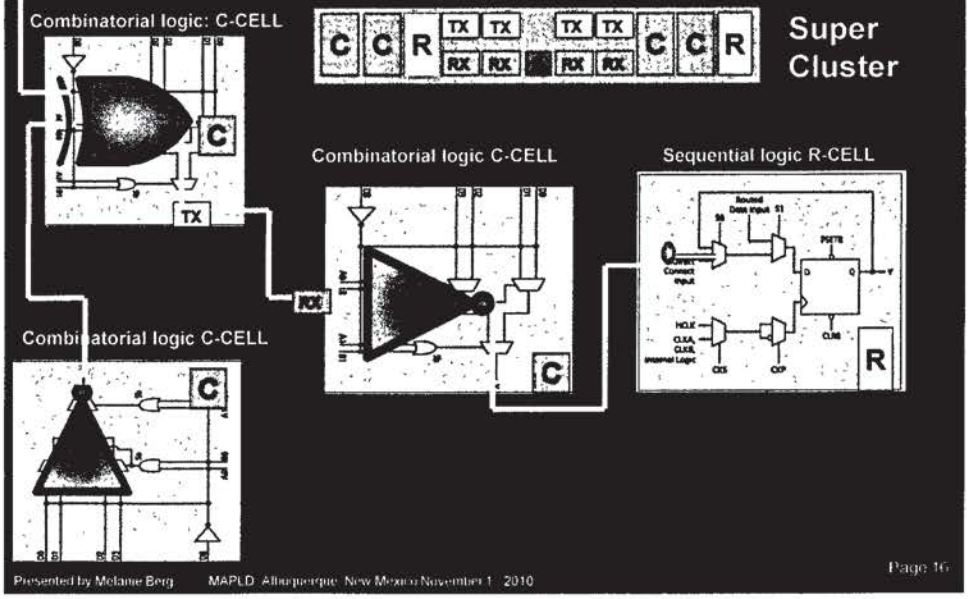

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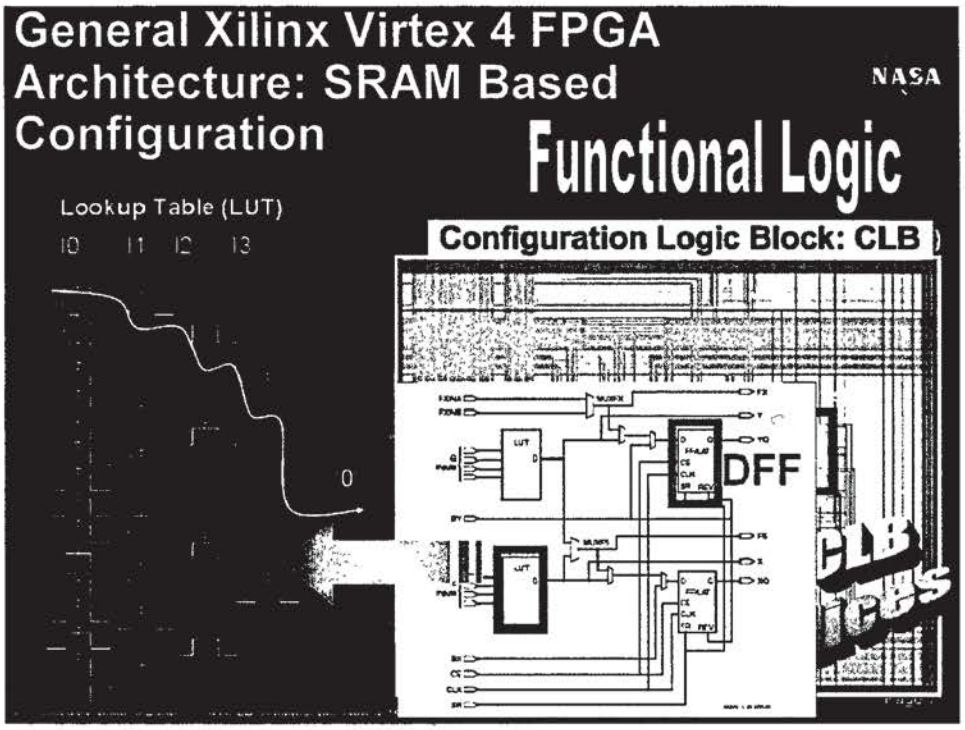

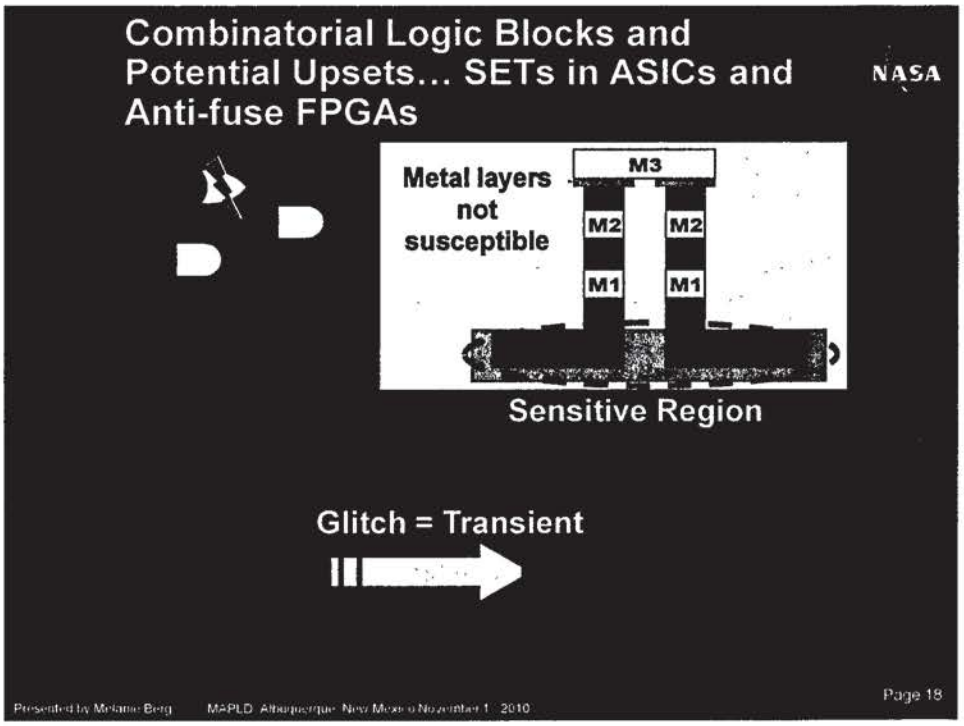

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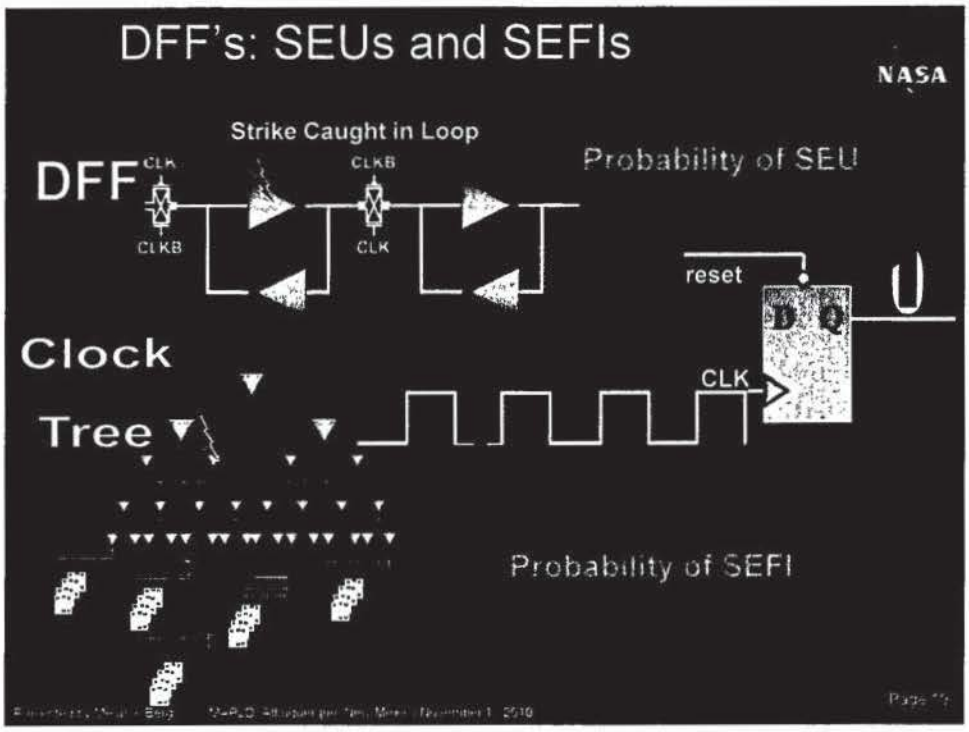

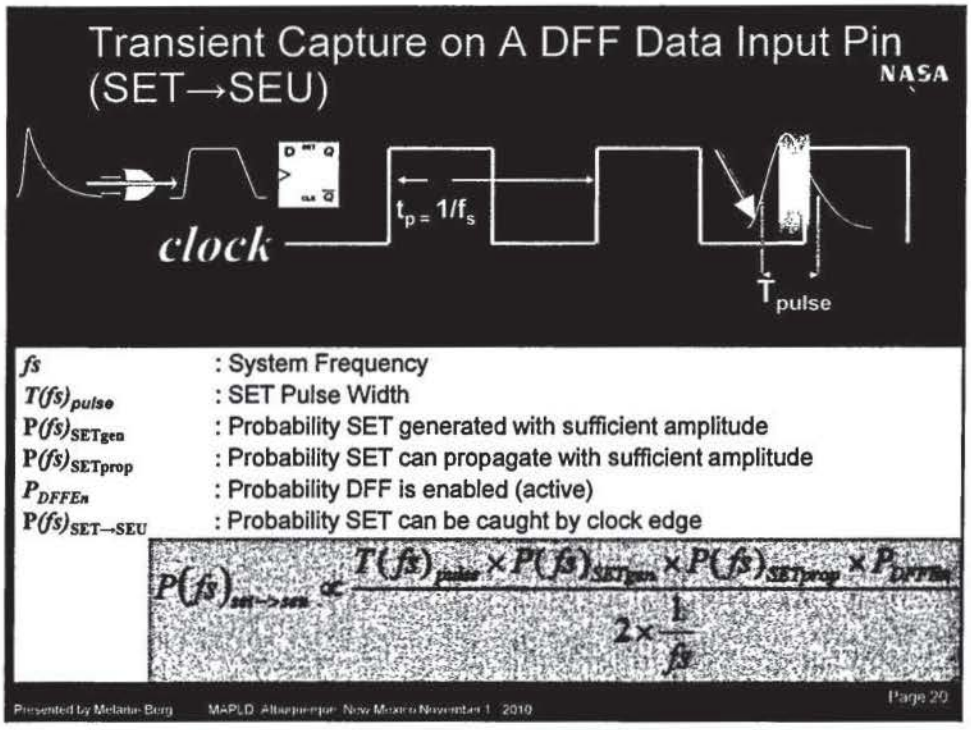

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Summary: Most Significant Factors of System Error Probability $P(fs)_{error}$

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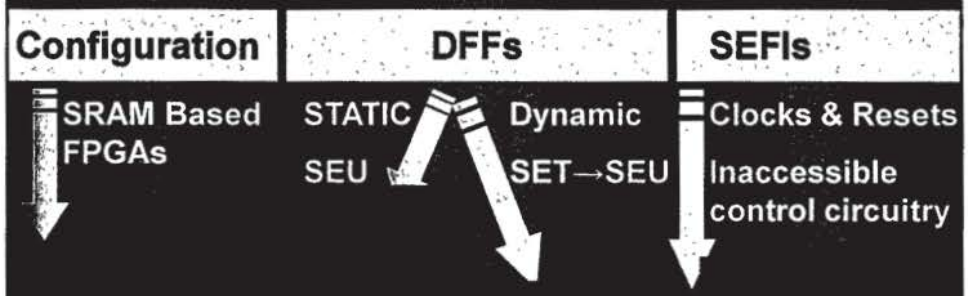

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Section III: Reducing System Error: Common Mitigation Techniques

- Triple Modular Redundancy:
  - Block Triple Modular Redundancy (BTMR)
  - Local Triple Modular Redundancy (LTMR)
  - Global Triple Modular Redundancy (GTMR)
  - Distributed Triple Modular Redundancy (DTMR)

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Mitigation

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- Error Correction or Error avoidance
- Mitigation can be:
  - **Embedded**: built into the device library cells
    - User does not verify the mitigation – manufacturer does
  - **User inserted**: part of the actual design process
    - User must verify mitigation… Complexity is a RISK!!!!!!!!
- Mitigation should reduce error…
  - Generally through redundancy
  - Incorrect implementation can increase error

Want to reduce as many terms as possible:

Example: TMR Mitigation Schemes will use Majority Voting

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I0	I1	I2	Majority Voter
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Best 2 out of 3

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Reducing System Error: Common Mitigation Techniques

- Triple Modular Redundancy:
  - Block Triple Modular Redundancy (BTMR)
  -
  -
  -

BTMR

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VOTING MATRIX

- Need Feedback to Correct
- Generally can not apply internal correction from voted outputs
- Errors can accumulate – not an effective technique

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Reducing System Error: Common Mitigation Techniques

- Triple Modular Redundancy:
  - Local Triple Modular Redundancy (LTMR)

Local Triple Modular Redundancy (LTMR): Vote+Feedback Correction

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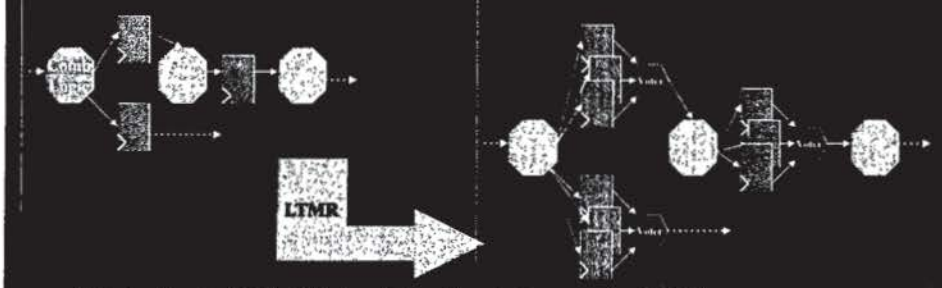

- Triple Each DFF + Vote+ Feedback Correct at DFF
- Unprotected:
  - Clocks and Resets… SEFI
  - Transients (SET->SEU)
  - Internal/hidden device logic: SEFI

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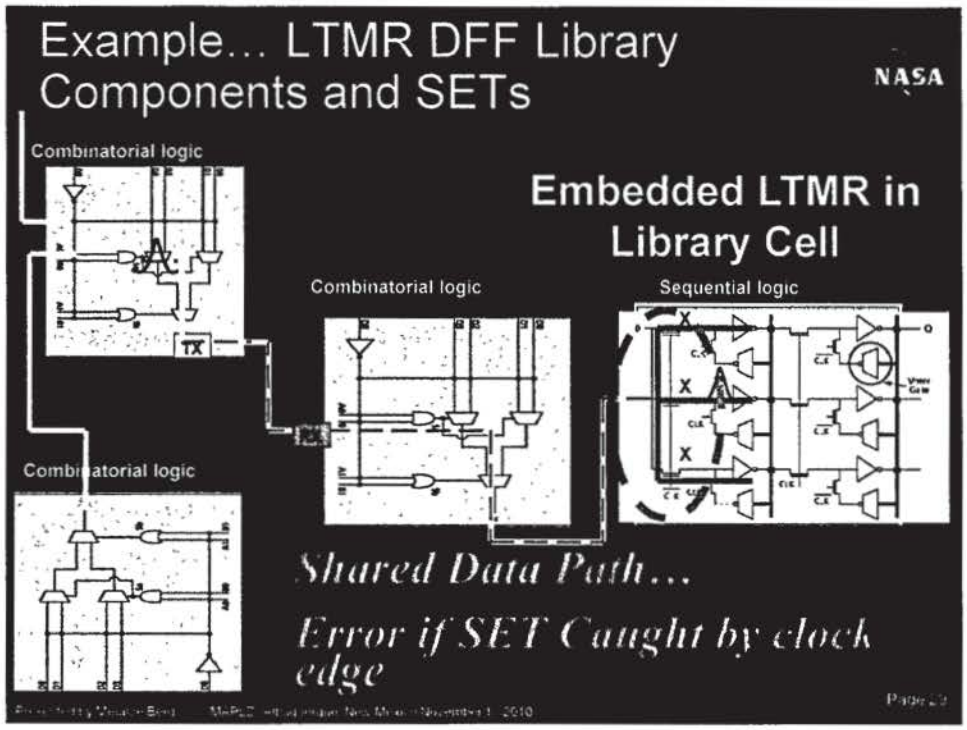
Example... LTMR DFF Library Components and SETs
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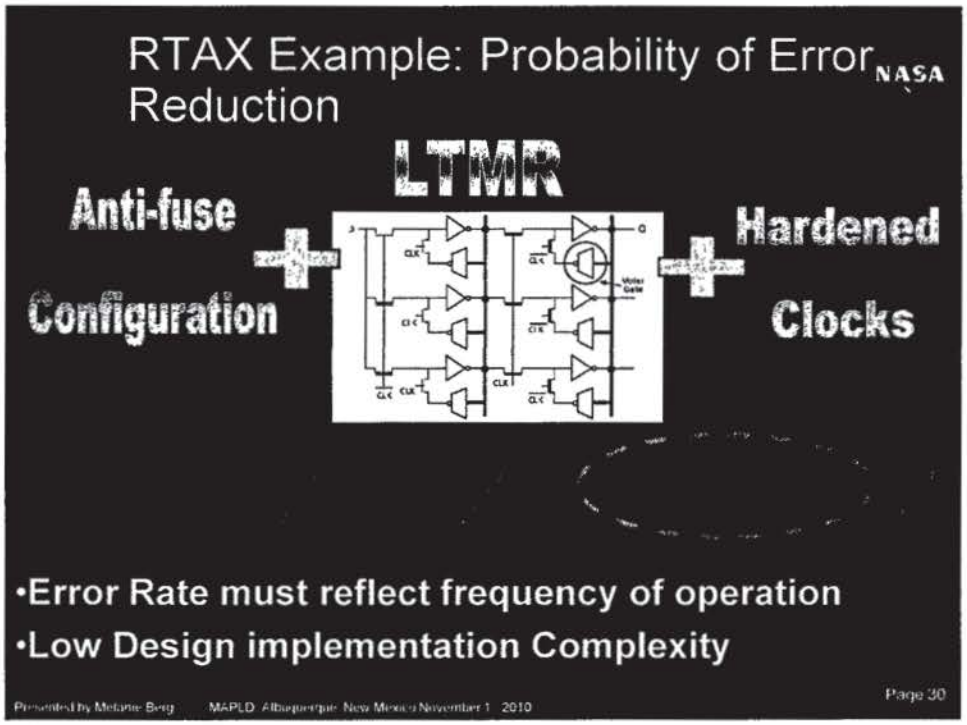
Combinatorial logic
TX
Embedded LTMR in Library Cell
Combinatorial logic
Sequential logic
Combinatorial logic
Shared Data Path...
Error if SET Caught by clock edge


RTAX Example: Probability of Error Reduction
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LTMR
Anti-fuse
Configuration
Hardened
Clocks
•Error Rate must reflect frequency of operation
•Low Design implementation Complexity
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Example...Upper-Bound Error Prediction for Actel Antifuse FPGA...LTMR + hardened Global Routes RHBD

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- Given... 15MHz to 120MHz: Dynamic Error Bit Rate

$P(fs)_{SET-SEU}$:

Source: NASA Goddard

Upper-Bound Error Prediction: Number of Bits x Bit Error Rate

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With embedded LTMR Mitigation + Hardened Clocks

10,000 DFFs

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Reducing System Error: Common Mitigation Techniques

- Triple Modular Redundancy:
  -
  -
  - Global Triple Modular Redundancy (GTMR)
  -

Global Triple Modular Redundancy (GTMR): Largest Area → Complexity

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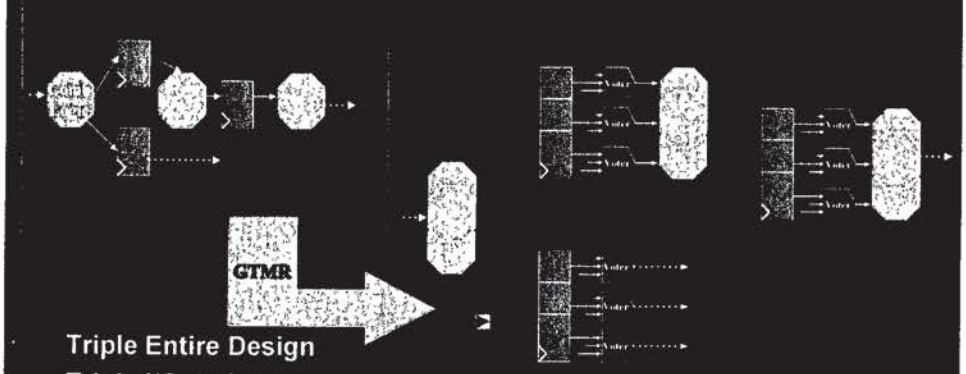

- Triple Entire Design
- Triple I/O and Voters
- Unprotected – hidden device logic SEFIs
- Can not be an embedded strategy: Complex to verify

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GTMR Proves To be A Great Mitigation Strategy... BUT...

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- Triplicating a design and its global routes takes up a lot of power and area
- Not part of the provided and well tested/characterized library elements
- Generally performed after synthesis by a tool– not part of RTL
- Difficult to verify
- Additional complications with Clock Skew and domain crossings
- Can be implemented in an ASIC... but is not considered as a contemporary methodology

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Reducing System Error: Common Mitigation Techniques

- **Triple Modular Redundancy:**
  -
  -
  -
  - **Distributed Triple Modular Redundancy (DTMR)**

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Distributed Modular Redundancy (DTMR)... GTMR without Clock Replication

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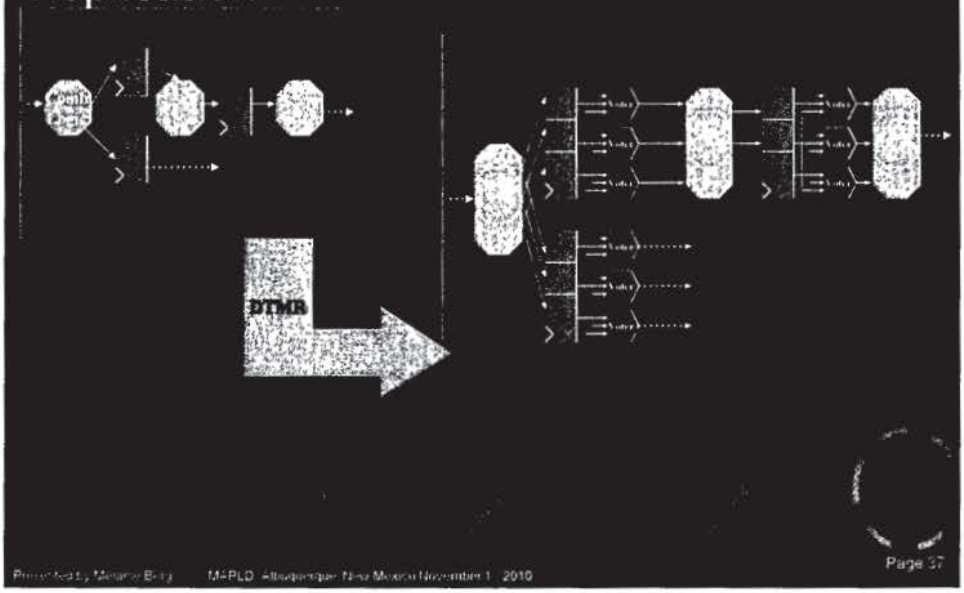

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Section IV:
The Automation Process

Automation through Synthesis

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- Mentor Graphics and Synplicity provide TMR insertion
- It is up to the designer to understand which type of TMR to implement based on the target FPGA and the target space environment

FPGA	LTMR	DTMR	GTMR
Antifuse			
Antifuse+LTMR			
SRAM			
Flash			

General Recommendation
Not Recommended but may be a solution for some situations
Will not be a good solution

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Mitigation Design Process

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Benefits of Automation

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- Difficult to implement mitigation schemes manually with VHDL or Verilog
  - Synthesis Optimization
  - Designer error
  - Mitigation Optimization (voter reduction)
- May reduce the probability of insertion design error:
  - Coding errors are difficult to detect
  - Utilizes a structured and well defined insertion process

Example: Design Error and Mitigation

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- Only 2 valid paths at any given Moment due to erroneous manual design
- If an SEE error occurs in one of the functional paths, the voters will not be able to mitigate
- May not be detected during simulation

Incorrect Voter Insertion: Example with 16ns Time Constraint

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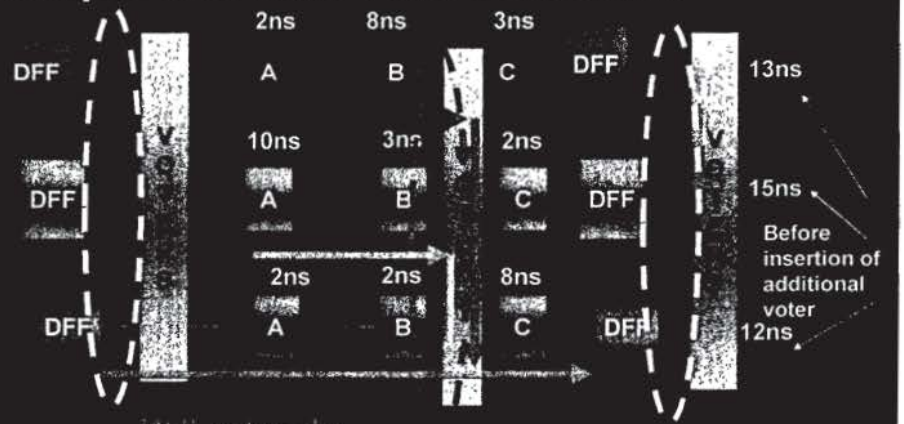

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Section IV:

The Mentor Advantage

Up-to-Date Radiation Effects Knowledge

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- The best designers can create the worst designs:
  - Must understand radiation effects in order to mitigate properly
  - Each FPGA device has different error modes and signatures
- Mentor has established a close relationship with the radiation effects community
- Knowledge of current FPGA test results is the premise of Precisions mitigation strategies
- Mitigation has been utilized in NASA Goddard Radiation Effects particle accelerator experiments

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Voter Insertion

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- Intelligent handling of many special cases
  - Logic Reduction
  - Primary top-level design outputs
  - Clock Enable Handling
  - Control Domain Crossings
  - Multiply-Accumulate Circuits
  - Latches
  - Combinatorial Loops
  - Black Boxes
- We don't have time to discuss all:
  - Primary top-level design outputs
  - Control Domain Crossings
  - Black Boxes

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Section IV:

The Mentor Advantage:

- Logic Reduction (GTMR and DTMR)

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Basis of Automated Process

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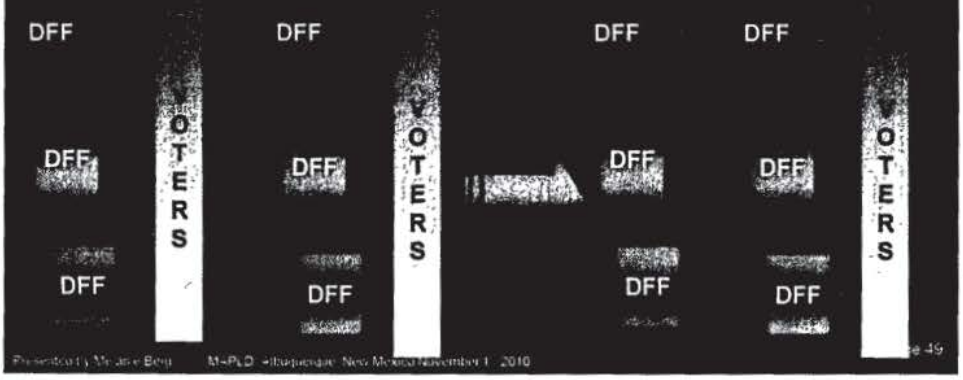
- Voters are placed after DFFs
- **Logic Reduction:** Voters are not placed in paths of "always enabled" DFFs that are not part of a feedback loop

Logic reduction Example: No feedback – No enable



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Section IV:

The Mentor Advantage:

- Primary top-level design outputs

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Voter Insertion: Outputs

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- Most Design guidelines will not allow combinatorial logic after a register directly feeding an output
- The user has a choice
- Primary top-level design outputs:
  - Mapping register into fabric
  - Tripling top-level IO (or not!!!!!!!)
  - Mapping register into pad cell (path convergence)

Common DTMR and GTMR I/O Strategies

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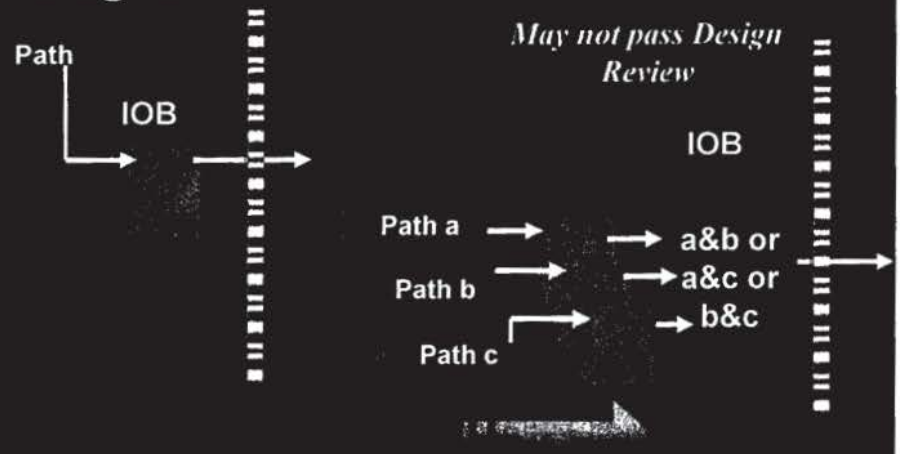
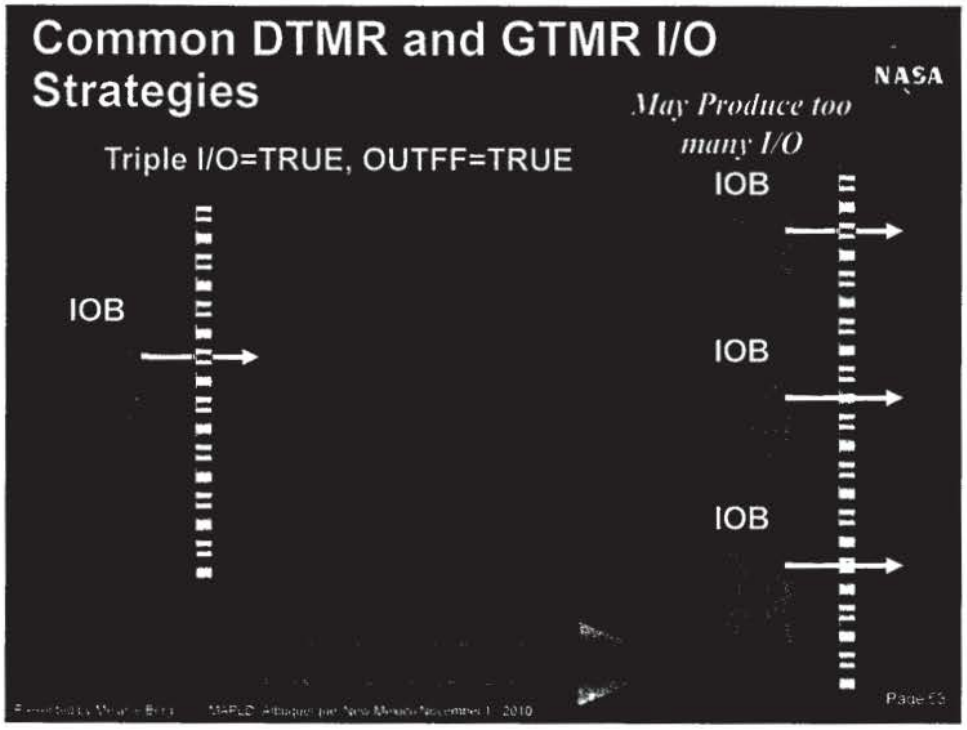
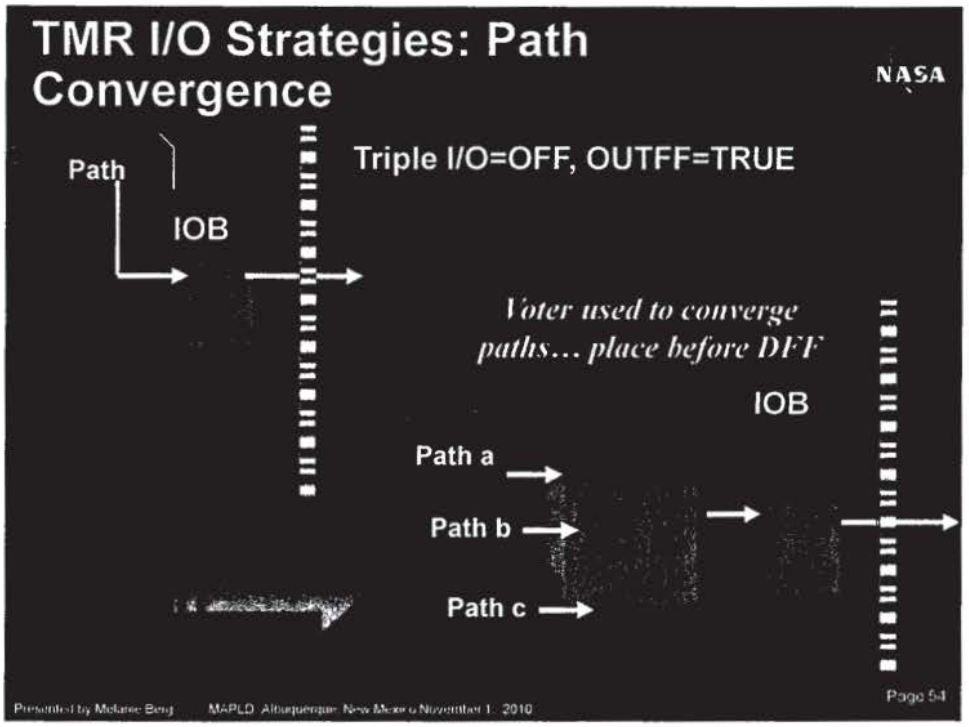


Triple I/O=OFF, OUTFF=FALSE





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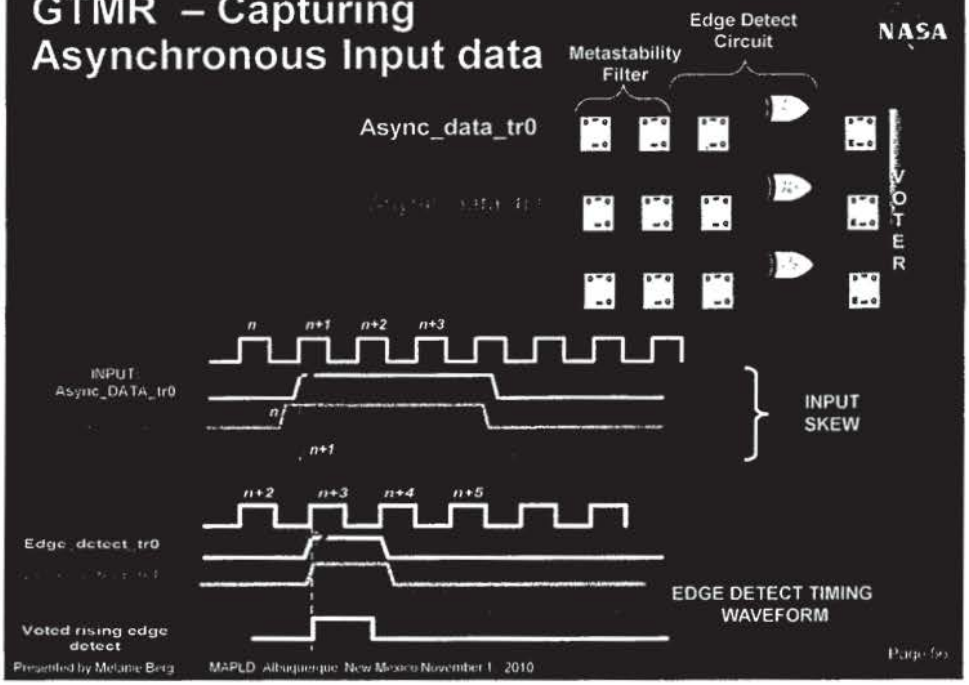
Section IV:

The Mentor Advantage:

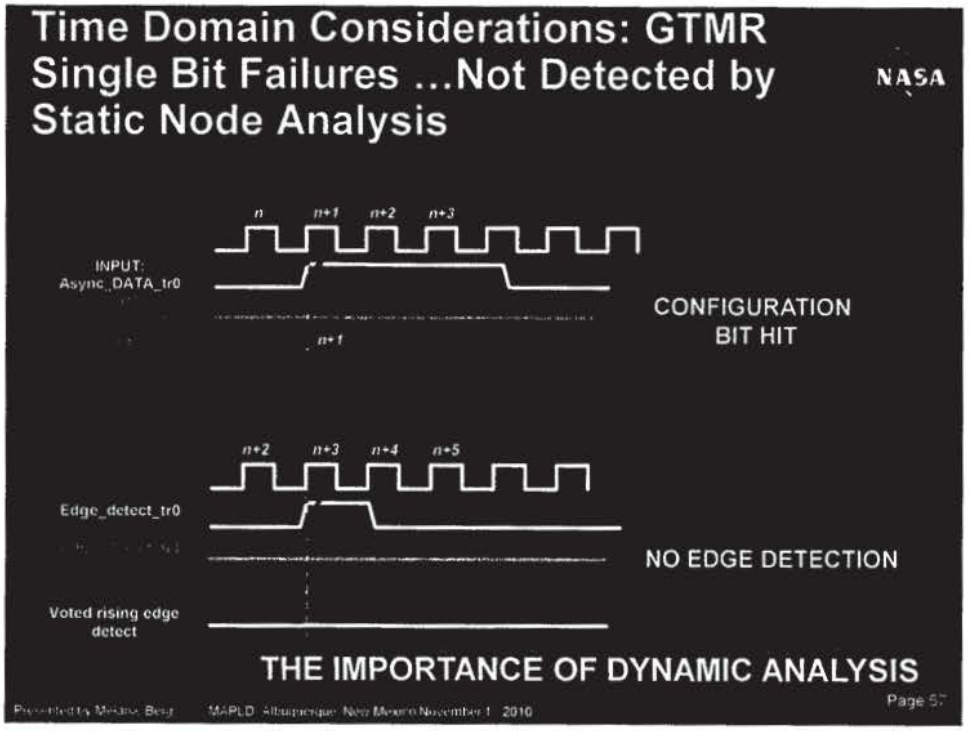
- Control Domain Crossings... GTMR issue

GTMR – Capturing Asynchronous Input data

NASA



To be presented by Melanie Berg at the ReSpace/MAPLD 2010 Conference [Military and Aerospace Programmable Logic Devices (MAPLD)], November 1-4, 2010 in Albuquerque, NM, and on http://radhome.gsfc.nasa.gov and http://nepp.nasa.gov/.


Time Domain Considerations: GTMR Single Bit Failures ...Not Detected by Static Node Analysis
NASA
n
n+1
n+2
n+3
INPUT: Async_DATA_tr0
n+1
CONFIGURATION BIT HIT
n+2
n+3
n+4
n+5
Edge_detect_tr0
NO EDGE DETECTION
Voted rising edge detect
THE IMPORTANCE OF DYNAMIC ANALYSIS
Presented by Melanie Berg
MAPLD Albuquerque New Mexico November 1 2010
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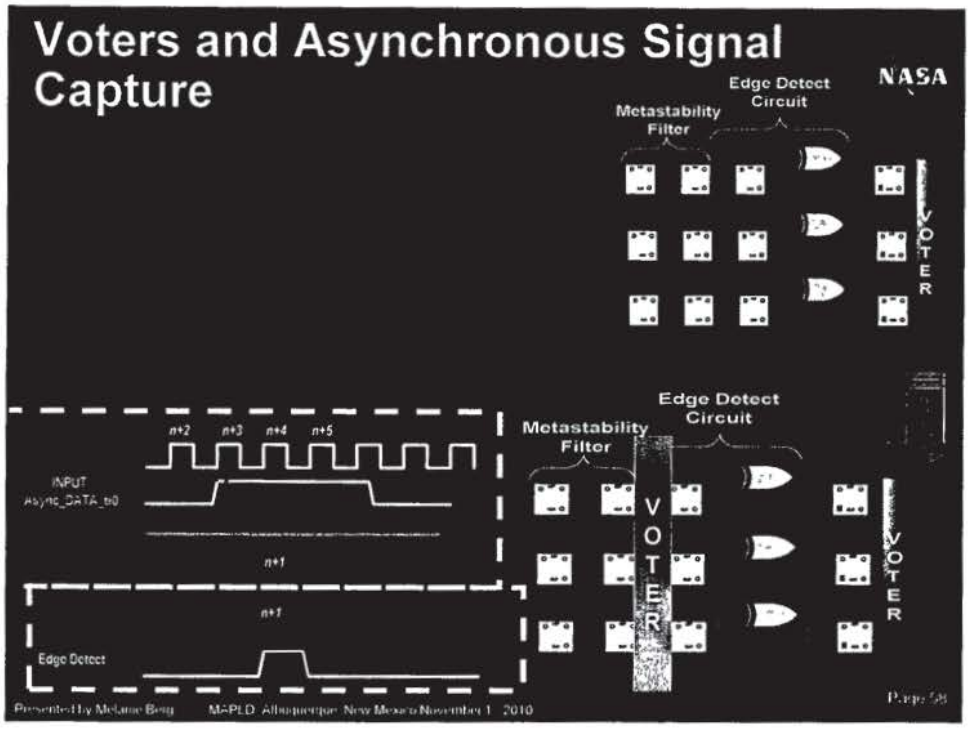
Voters and Asynchronous Signal Capture
NASA
Edge Detect Circuit
Metastability Filter
VOTER
n+2
n+3
n+4
n+5
INPUT
Async_DATA_tr0
n+1
n+1
Edge Detect
Edge Detect Circuit
Metastability Filter
VOTER
VOTER
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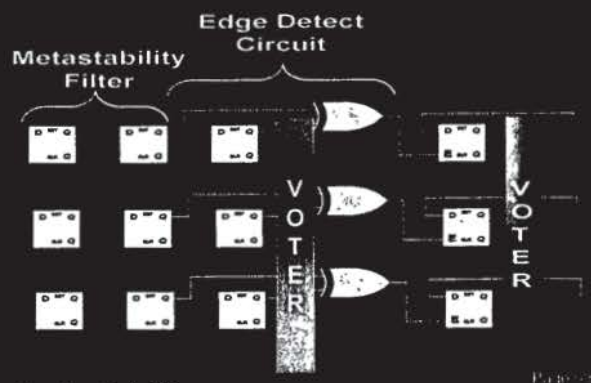
Clock Domain Crossings and Automation

NASA

User will want to put an attribute to ensure voter in this asynchronous path



NASA

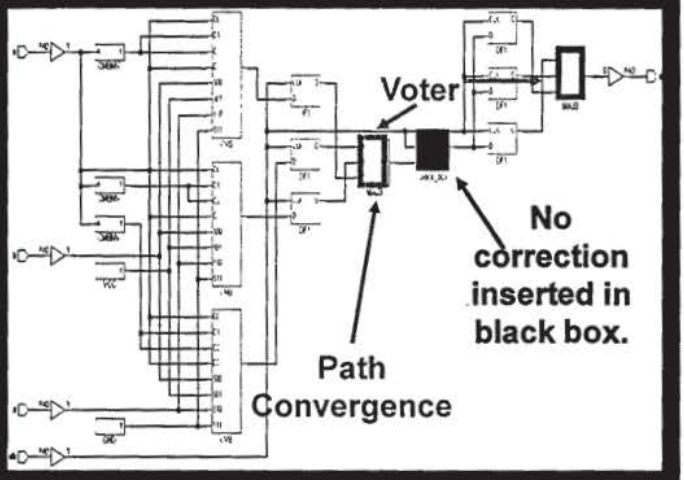
Section IV:

The Mentor Advantage:

- Black Boxes

DTMR Black Box Handling

NASA



DTMR result. Voters are used to converge tripled logic at black box inputs. Black box outputs fan out to tripled logic.

Summary

NASA

- SEEs will affect FPGAs in space radiation environments
- TMR has been the most effective SEE mitigation technique
- There are many types of TMR:
  - BTMR
  - LTMR
  - DTMR
  - GTMR
- The goal is to select the optimal TMR scheme regarding:
  - SEE requirements
  - Area, Power, Speed

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Summary (Continued)

NASA

- Mentor has integrated different TMR schemes into their synthesis package.
- The designer must be aware of the target FPGA and its SEE sensitivity before using any automated approach
- Strategies are robust:
  - Flexible based on FPGA susceptibility
  - Many user options
  - Validated via radiation testing
- After TMR insertion, a rigorous review and simulation process must be performed

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