Incorporating Probability Models of Complex Test Structures to Perform Technology Independent FPGA Single Event Upset Analysis

M. Berg, *Member IEEE,* H. Kim, M. Friendlich, C. Perez, C. Seidleck, K. LaBel, *Member IEEE*

***Abstract*—We present SEU test and analysis of the Microsemi ProASIC3 FPGA. SEU Probability models are incorporated for device evaluation. Included is a comparison to the RTAXS FPGA illustrating the effectiveness of the overall testing methodology.**

***Index Terms*—FPGA, ProASIC3 versus RTAXS, SEU, Test and Analysis**

I. Introduction

An effective method for modeling Single Event Upset (SEU) probabilities ($P(fs)_{error}$) in Field Programmable Gate Array (FPGA) devices has been presented[1][2]. It is a top-down modeling approach. The top-level of the FPGA $P(fs)_{error}$ model was shown to have three major components (1):

- Configuration SEU cross section ($P_{configuration}$)
- Data path or functional logic SEU cross section ($P_{FuctionalLogic}$)
- Single Event Functional Logic SEU cross section (P_{SEFI})

$$P(fs)_{error} \propto P_{configuration} + P_{FunctionalLogic} + P_{SEFI} \quad (1)$$

The SEU Probability model is used by NASA Goddard Radiation Effects and Analysis Group (REAG) as a Single Event Effects (SEE) data analysis tool. Upsets that occur during radiation testing are differentiated and are categorized in order to enhance device evaluation. The model is a reflection of the SEU cross section (σ_{SEU}) for a synchronous digital system. Operational frequency (*fs*) is understood to be the inverse of clock period (τ_{clk}) as in (2).

$$\tau_{clk} = \frac{1}{fs} \quad (2)$$

The importance of this subject matter is to present Microsemi ProASIC3 FPGA SEU behavior under a variety of conditions while illustrating how the REAG SEU model facilitates a detailed analysis that spans across FPGA device technologies. Microsemi RTAXS data[2] will be used as a comparison.

II. $P(FS)_{ERROR}$ Model Components

Before radiation testing is performed, models of expected SEU probabilities based on mitigation and device logic structure are constructed. The models are used as reference points during radiation testing. During the analysis phase, the models are refined to reflect SEU results from radiation testing. The following is a more detailed discussion of each element in (1).

A. FPGA Configuration and $P_{configuration}$

Configuration is a separate technology than the functional logic. Accordingly, it has its own categorization of upsets. It has been shown through Configuration SEE radiation testing of Antifuse[1]-[4] and Flash technologies[3][4] that $P_{configuration}$ is considered zero as in (3).

$$\textit{Antifuse and Flash Configuration: } Pconfiguration \rightarrow 0: \quad (3)$$

The RTAXS has an antifuse configuration [7] while the ProASIC3 has a flash configuration [8]. Because $P_{configuration}$ is essentially zero for these devices, the following discussion focuses on $P(fs)_{functionalLogic}$ and P_{SEFI}.

B. Functional Logic Data Path Upsets and $P_{functionalLogic}$

The functional logic data path is comprised of: Combinatorial Logic, Flip-Flops (DFFs), and Routes. Table 1 illustrates upset types that can potentially occur in a FPGA data path. In a synchronous design, every DFF is connected to a global clock signal. Because a DFF is master-slave edge

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M. D. Berg is with MEI Technologies, Landham, MD USA. She is in support of NASA Goddard Space Flight Center, Greenbelt, MD 20771 USA phone: 301-286-2153; fax: 301-286-4699; e-mail: Melanie.D.Berg@NASA.gov.

H. S. Kim is with MEI Technologies, Landham, MD USA. He is in support of NASA Goddard Space Flight Center, Greenbelt, MD 20771 USA.

M. A. Friendlich is with MEI Technologies, Landham, MD USA. He is in support of NASA Goddard Space Flight Center, Greenbelt, MD 20771 USA.

C. E. Perez is with MEI Technologies, Landham, MD USA. He is in support of NASA Goddard Space Flight Center, Greenbelt, MD 20771 USA.

C. M. Seidlick is with MEI Technologies, Landham, MD USA. She is in support of NASA Goddard Space Flight Center, Greenbelt, MD 20771 USA

K. A. LaBel is NASA Goddard Space Flight Center, Greenbelt, MD 20771 USA

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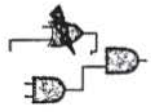
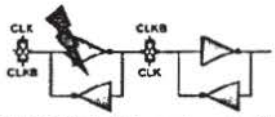
flip-flop its internal structure uses both a global clock (CLK) and its logical inverse (CLKB).

TABLE 1: COMBINATORIAL LOGIC VERSUS SEQUENTIAL LOGIC

Term	Definition
Logic function generation (computation)	Captures and holds state of combinatorial logic
	
SET: Glitch in the combinatorial logic: Capture is frequency dependent	SEU: Next state capture can be frequency dependent
Double-sided	Single-sided

1) Synchronous Design Concepts and the Functional Data Path

The essence of synchronous design considers DFFs as boundary points. In a design, each boundary point DFF will have a cone of logic feeding it. The cone is defined to be a backwards trace from an End-Point DFF that stops at its previous stage DFFs (Start-Point DFFs). The trace includes the Start-Point DFFs and all combinatorial logic within the path. One cone of logic is illustrated in Fig. 1.

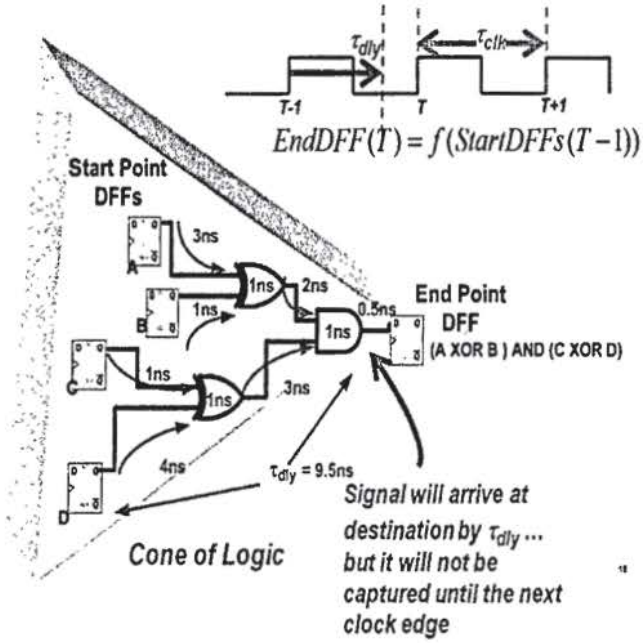


Fig. 1 Start-Point DFFs → End Point DFFs t_{dly} and the Cone of Logic

2) $P(fs)_{functionalLogic}$ Evaluation for Synchronous Designs

In order to analyze $P(fs)_{functionalLogic}$, each DFF is evaluated as an End-Point with a cone of logic backwards trace. τ_{dly} is the delay from a Start-Point DFF to an End-Point DFF within a cone of logic. There is a unique τ_{dly} for every Start-Point to End-Point. By definition of synchronous design: $\tau_{dly} < \tau_{clk}$. Equation (4) is a breakdown of $P(fs)_{functionalLogic}$ by Start-Point DFF and combinatorial logic.

TABLE 2: DEFINITION OF TERMS IN EQUATION 4

Term	Definition
$P_{DFFSEU \rightarrow SEU}$	Probability that the Start-Point DFF will incur a SEU and that it will be captured by an End-Point
$P_{SET \rightarrow SEU}$	Probability that the Start-Point DFF will incur a SEU and it will be captured by an End-Point

$$P(fs)_{functionalLogic} \propto \exists_{DFF}\left(\sum_{j=1}^{\#StartPointDFFs} P(fs)_{DFFSEU \rightarrow SEU(j)} + \sum_{i=1}^{\#CombinatorialCells} P(fs)_{SET \rightarrow SEU(i)}\right) \quad (4)$$

3) Capturing Start-Point DFF Upsets ($P(fs)_{DFFSEU \rightarrow SEU}$)

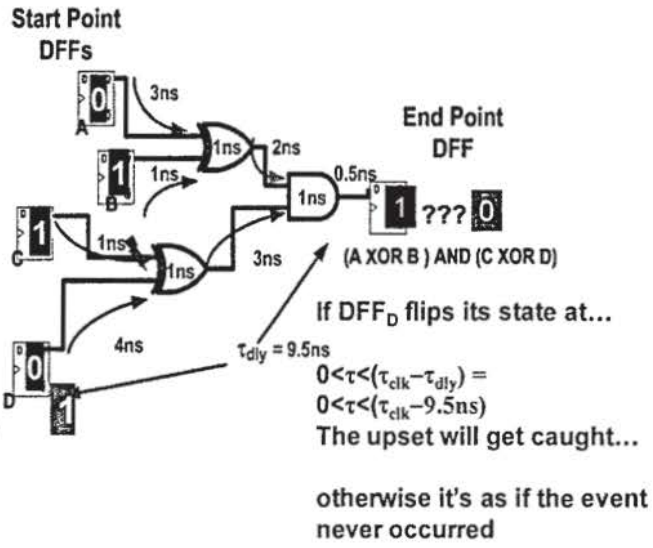


Fig. 2: Will the End-Point DFF capture the Start-Point SEU? Capture occurs if $\tau<\tau_{clk}-\tau_{dly}$: giving the one-sided signal enough time to reach the End-Point DFF

TABLE 3: DEFINITION OF TERMS

Term	Definition
P_{DFFSEU}	Probability the Start-Point DFF will incur a SEU
$1-\tau_{dly}fs$	Portion of clock cycle that the End-Point DFF can capture a Start-Point DFF SEU before the next clock edge. Assumes the SEU Start-Point DFF is always enabled and will have a valid value at the next clock edge
P_{gen}	Probability a combinatorial gate will incur a SET
P_{prop}	Probability the SET can propagate to an End-Point DFF

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τ_{width}/fs	SET width to clock period ratio

If a Start-Point DFF incurs a SEU (P_{DFFSEU}) it will occur at time τ as a single sided function (see Table 1) somewhere within a clock period (τ_{clk}). It will not manifest as a system upset unless an End-Point DFF captures the single sided upset at the next clock edge. An End-Point will only capture the Start-Point upset if it occurs at τ such that after propagating through the delay path (τ_{dly}), the single sided upset arrives at the data pin of the End-Point prior to the clock edge as shown in Fig. 3 and (5).

$$\tau < \tau_{clk} - \tau_{dly} \tag{5}$$

The portion of the clock period that a Start-Point DFF SEU can be captured by an End-Point DFF is shown (6).

$$\frac{\tau}{\tau_{clk}} < 1 - \frac{\tau_{dly}}{\tau_{clk}} = 1 - \tau_{dly} fs \tag{6}$$

The probability that P_{DFFSEU} will manifest as a system error ($P_{DFFSEU \rightarrow SEU}$) is reflected (7).

$$P(fs)_{DFFSEU \rightarrow SEU} \propto \exists_{DFF} \left(\sum_{j=1}^{\#StartPoint\ DFFs} P_{DFFSEU(j)} (1 - \tau_{dly(j)} fs) \right) \tag{7}$$

4) System Upsets due Combinatorial logic ($P_{SET \rightarrow SEU}$)

If a SET occurs in a combinatorial logic gate within the cone of logic for an End-Point DFF, it has the possibility of being captured by its End-Point with a probability of ($P(fs)_{SET \rightarrow SEU}$). It has been shown [1][2] that the upper-bound $P(fs)_{SET \rightarrow SEU}$ for a synchronous design is proportional to the following probabilities: generation of a SET (P_{gen}), propagation of the SET (P_{prop}), and capture of the SET. In addition, the SET capture is proportional to the width (τ_{width}) of the SET with respect to the fs as shown in (8).

$$P_{SET \rightarrow SEU} \propto \exists_{DFF} \left(\sum_{i=1}^{\#CombinatorialCells} (P_{gen(i)} P_{prop(i)} \tau_{width(i)} fs) \right) \tag{8}$$

5) Putting it all together DFF and Combinatorial Logic Upsets

As previously mentioned, data path susceptibility ($P(fs)_{functionalLogic}$) is based on the cone of logic Start-Point DFF capture ($P(fs)_{DFFSEU \rightarrow SEU}$) and combinatorial logic gate capture ($P(fs)_{SET \rightarrow SEU}$) as shown in (9).

$$P(fs)_{functionalLogic} \propto \exists_{DFF} \left(\sum_{j=1}^{\#StartPoint\ DFFs} P_{DFFSEU(j)} (1 - \tau_{dly(j)} fs) + \sum_{i=1}^{\#CombinatorialCells} P_{gen(i)} P_{prop(i)} \tau_{width(i)} fs \right) \tag{9}$$

C. Single Event Functional Interrupt (P_{SEFI})

A Single Event Functional Interrupt (SEFI) is a SEU that forces the FPGA to be inoperable. According to the NASA REAG SEU Model, P_{SEFI} has two major categories:

1) Global Route SEFI: $P_{GlobalRoutes}$

As previously mentioned, in a synchronous design, all DFFs must be connected to a clock. In addition, all DFFs should be connected to a reset. Clock and reset signals are categorized as global routes because they are connected to a large number of components.

An upset in a global route can cause catastrophic events because a large number of elements can be affected simultaneously. Subsequently, global route networks have been categorized as a SEFI.

2) Hidden Logic SEFI: $P_{HiddenLogic}$

Some FPGA devices have additional logic that are inaccessible to the designer. The hidden logic is used for a variety of operations depending on the manufacturer. The ProASIC3 and RTAXS contain JTAG circuitry [4][6]. If the circuitry were to incur a SEU, it is possible for the FPGA's I/O to become inoperable and hence cause catastrophic responses, i.e. a SEFI. However, if the circuitry is grounded during operation, it has been proved that no SEFIs are possible [4][6].

3) ProASIC3 and RTAXS P_{SEFI} Equation

Regarding the ProASIC3 and RTAXS FPGA devices, the hidden logic contribution to P_{SEFI} is considered zero. Hence, P_{SEFI} is only affected by the FPGA design's global routes.

$$ProASIC3\ and\ RTAXS: P_{SEFI} \propto P_{GlobalRoutes} \tag{10}$$

III. Analysis of Model Components

It is intuitive to expect that a non-mitigated design will have a significantly higher σ_{SEU} than a mitigated design. It is not necessarily intuitive to determine the strength of the mitigation or the dominant source of SEUs. However, component significance can be determined using Table 4 and σ_{SEU} data.

TABLE 4: ANALYSIS OF SEU CAPTURE EFFECTS: $P_{DFFSEU \rightarrow SEU}$ VERSUS $P_{SET \rightarrow SEU}$

	$P_{DFFSEU \rightarrow SEU}$	$P_{SET \rightarrow SEU}$
Logic	DFF Capture	Combinatorial SET Capture
Capture percentage of clock period	$1-\tau_{dly}fs =$ $1-\tau_{dly}/-\tau_{clk}$	As frequency increases, $P_{DFFSEU \rightarrow SEU}$ increases

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Frequency Dependency	Increase in frequency decreases $P_{DFFSEU \rightarrow SEU}$	Increase in frequency increases $P_{SET \rightarrow SEU}$
Combinatorial Logic Effect	Increase in Combinatorial logic increases τ_{dly} and decreases $P_{DFFSEU \rightarrow SEU}$	Increase in Combinatorial logic increases $P_{SET \rightarrow SEU}$

Based on Table 4, the following is a list of trends used for evaluating σ_{SEU} data and determining dominant sources of susceptibility:

$P(fs)_{DFFSEU \rightarrow SEU}$ Dominance – Most SEUs stem from Captured Start-Point DFFs. This is true when:

- There is an increase in the number of combinatorial logic blocks or τ_{dly} and the σ_{SEU} ($P(fs)_{error}$) decreases in response
- There is an increase in frequency and the σ_{SEU} decreases in response

$P(fs)_{SET \rightarrow SEU}$ Dominance – Most SEUs stem from Captured Combinatorial Logic SETs. This is true when:

- There is an increase in frequency and σ_{SEU} increases in response
- There is an increase in combinatorial logic and σ_{SEU} increases in response

Local Mitigation Strength: if the design has been mitigated using a localized-DFF mitigation scheme such as Localized Triple Modular Redundancy (LTMR)[1] or Dual Inter Cell (DICE)[6]:

- It is expected that the DFFs are masked from σ_{SEU} contribution. $P(fs)_{DFFSEU \rightarrow SEU}$ should be insignificant and hence σ_{SEU} is lower.
- However, if $P(fs)_{DFFSEU \rightarrow SEU}$ has the most significant error contribution for a localized-DFF mitigation scheme, then the mitigation scheme is considered weak because it is not fully masking DFF upsets.

IV. Reducing System Error: Triple Modular Redundancy Schemes

Before testing is performed, general models of expected SEU probabilities based on mitigation and device logic structure are constructed. The models are used as reference points during radiation testing. During the analysis phase, the models are refined to reflect SEU results from radiation testing.

For the ProASIC3 and RTAXS, as previously mentioned, $P_{configuration}$ is near zero. Substituting $P(fs)_{DFFSEU \rightarrow SEU}$ and $P(fs)_{SET \rightarrow SEU}$ in (1) for $P(fs)_{functionalLogic}$, a non-mitigated ProASIC3 or RTAXS design is expected to have a σ_{SEU} cross as reflected in (11).

$$No - Mitigation\ \sigma_{SEU}:$$
$$P(fs)_{Error} \propto P_{DFFSEU \rightarrow SEU} + P_{SET \rightarrow SEU} + P_{SEFI} \quad (11)$$

In order to reduce σ_{SEU}, mitigation is applied to the FPGA design. A common form of mitigation is Triple Modular Redundancy (TMR). TMR is a scheme such that a group of circuitry is triplicated and then voted. The mitigation is a majority voter i.e. best-two-out-of three. It is important to differentiate and signify the TMR scheme based on which circuits are redundant so that the user is aware of the strength of the mitigation strategy. The following is a discussion of two TMR schemes: Localized TMR (LTMR) and Distributed TMR (DTMR).

A. Localized TMR (LTMR)

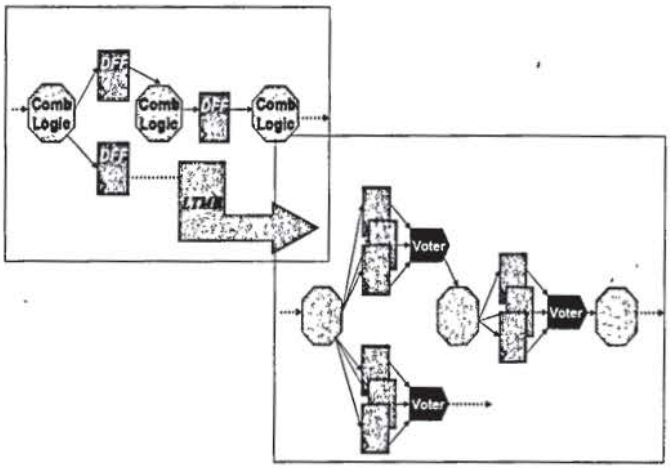

Fig 3: Localized Triple Modular Redundancy (LTMR). DFFs are triplicated and a voter is inserted into the data path.

LTMR is the process of triplicating each DFF of a design and inserting a voter after each DFF triplication [1][7]. The LTMR process is illustrated in Fig 3. A limitation of LTMR is that shared data paths exist as inputs to the triplicated DFFs. Consequently data path SETs are not mitigated and have the ability to be captured [1][2][5].

As a synopsis of the mitigation power of ProASIC3 and RTAXS LTMR, DFFs ($P_{DFFSEU \rightarrow SEU}$) are mitigated, but data paths ($P_{SET \rightarrow SEU}$) are not. If follows that (11) is reduced to (12) with LTMR insertion.

$$LTMR\ \sigma_{SEU}: P(fs)_{error} \propto P_{SET \rightarrow SEU} + P_{SEFI} \quad (12)$$

B. Distributed TMR(DTMR)

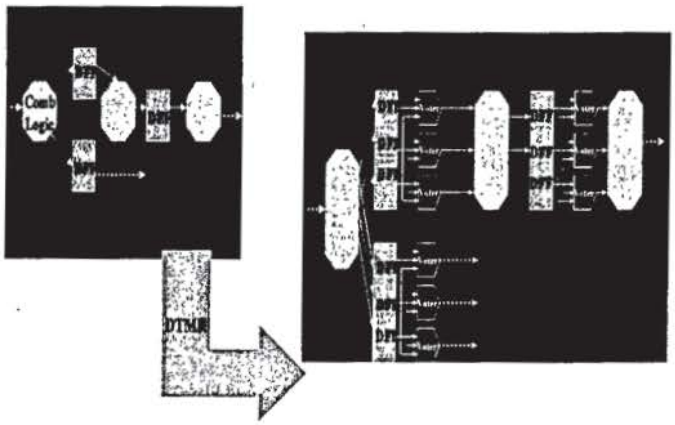

Fig 4 Distributed Triple Modular Redundancy (DTMR). The entire design is triplicated and a voter is inserted into each of the data paths.

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DTMR is the process of triplicating the entire design [1][7] excluding global routes such as clocks, resets, and global enables. DTMR is illustrated in Fig 4. No shared data paths exist. The points of susceptibility are only attributed to the global routes (or manufacturer hidden logic). In this manuscript global routes have been grouped into P_{SEFI}. Accordingly, the DTMR mitigation strategy is expected to reduce (11) to (13). Due to the dominance of P_{SEFI} in DTMR circuits, DTMR becomes a prime method for evaluating global routes during SEE testing.

$$DTMR\ \sigma_{SEU}: P(fs) \propto P_{SEFI} \quad (13)$$

V. ProASIC3 and RTAXS SEE Test Structures

The Device-Under-Test (DUT) test structures followed the NASA REAG FPGA testing methodology [2] implementing Windowed Shift Registers (WSR) strings and Counter Arrays. Only data pertaining to WSR chains are presented.

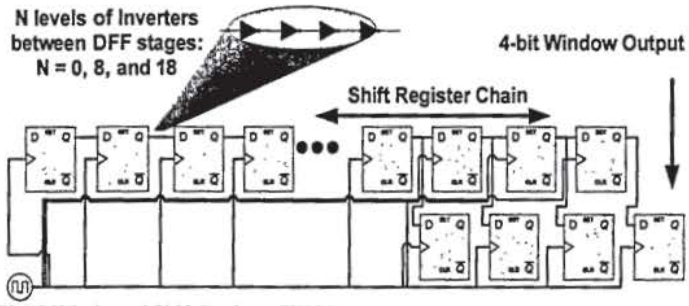

Fig. 5 Windowed Shift Register (WSR)

A WSR is a shift register with a different output scheme as illustrated in Fig. 5. Instead of outputting the last DFF once every clock cycle, a WSR outputs the last 4 DFFs once every 4 clock cycles. The parallel output has proven successful for high speed transmission [1].

Windowed Shift Register (WSR) Nomenclature

- WSR_0: N=0 Chain … Only DFFs
- WSR_8: N=8 Chain… 8 Inverters per 1 DFF
- WSR_{16}: N=16 Chain… 16 Inverters per 1 DFF

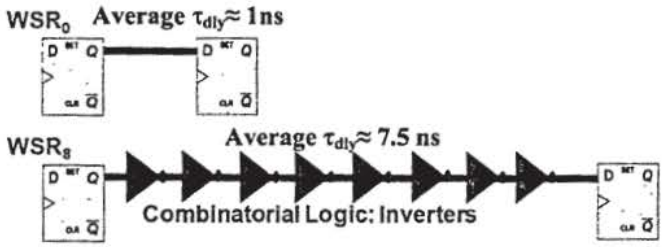

Fig. 6: Theoretical representation of one stage of a WSR chain. Actual WSR FPGA implementation general has additional combinatorial logic within each stage. Average $\tau_{dly}|_{WSR0} \approx$ 1ns and Average $\tau_{dly}|_{WSR80} \approx$ 7.5ns

Fig. 6 is a schematic representation of one stage of a WSR_0 and WSR_8 shift register. Test structure WSR chains contain hundreds of stages per WSR string [5] in order to increase event statistics during SEU testing.

It is important to note that although WSR_0 represents a WSR with only DFFs, in actual FPGA implementations, a small portion of additional-unexpected combinatorial logic can exist within the shift register stages. The additional logic is not shown in Fig. 6.

Static Timing Analysis (STA) has been performed on the WSR test structures. STA indicates that the average τ_{dly} for WSR_0 ($\tau_{dly}|_{WSR0}$) ≈1ns and the average τ_{dly} for WSR_8 ($\tau_{dly}|_{WSR8}$) ≈7.5ns.

The LTMR and DTMR ProASIC3 designs have been inserted using the automated synthesis tool: Mentor Precision-RTL [7].

VI. Heavy Ion SEU Testing

Heavy-Ion testing has been performed at Texas A&M using the NASA REAG Low Cost Digital Testing (LCDT) System[4][5].

A. SEU Cross Section Calculation

While the ProASIC3 is exposed to an active heavy-ion beam, designs are operating and outputs are compared to expected values for each clock cycle. If an output is not equivalent to its expected state, then an upset is recorded. σ_{SEU}s are based on the number of observed upsets normalized by the active beam particle fluence. Depending on the evaluation, an additional normalization step may be implemented to enhance analysis.

B. WSR Chains

Each WSR chain (e.g. N=0, N=8, and N=16) has a unique SEU cross section (σ_{WSRN_SEU}) and is normalized by the number of DFFs (bits) contained in the string. Equation (14) shows σ_{WSRN_SEU}.

$$\sigma_{WSRN_SEU} = \frac{\#\ WSR\ Upsets}{\#Particles \cdot \#WSR_DFFbits}\left[\frac{cm^2}{bit}\right] \quad (14)$$

C. Global Routes

Because global routes are connected to multiple DFF cells, one upset can affect a significant number of DFFs. Subsequently, global routes are not normalized by bit. SEU cross sections are measured by device. Equation(15) shows σ_{SEFI}.

$$\sigma_{SEFI} = \sigma_{Global_Route} = \frac{\#\ Global\ Upsets}{\#Particles}\left[\frac{cm^2}{device}\right] \quad (15)$$

D. SEU Cross Section Analysis

After the SEU cross sections are calculated, comparisons are performed to their expected models and across designs. WSRs are evaluated to determine:

- $P(fs)_{DFFSEU \rightarrow SEU}$ versus $P(fs)_{SET \rightarrow SEU}$ dominance: Which elements mostly contribute to the overall σ_{SEU}: DFFs or combinatorial logic?
- Frequency dependency: Is there a strong $P_{SET \rightarrow SEU}$ component? If frequency dependence is significant, frequency based σ_{SEU} data should be used as input to error rate calculations.
- Other SEU Model effects and trends as previously described in Section III.

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VII. Heavy Ion Test Results and Analysis

A. ProASIC3 Analysis

One would expect that WSR_8 σ_{SEU} (σ_{WSR8_SEU}) will always be greater than WSR_0 σ_{SEU} (σ_{WSR0_SEU}) because WSR_8 chains have more logic. However, σ_{SEU} data reveals that this is not always a valid assumption. Fig. 7 illustrates that for ProASIC3 No-TMR WSRs, $\sigma_{WSR0_SEU} > \sigma_{WSR8_SEU}$ across all LETs.

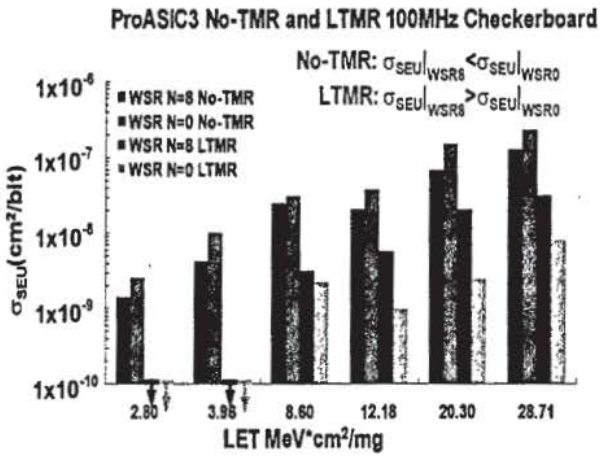

Fig. 7: ProASIC3 WSR_0 and WSR_8 with No-TMR and user-Inserted LTMR. For No-TMR WSR_0 has higher SEU Cross section than WSR_8. With LTMR the trend is switched, WSR_8 has a higher SEU cross section than WSR_0

Why are No-TMR ProASIC3 $\sigma_{WSR0_SEU} > \sigma_{WSR8_SEU}$ for every LET? Consider τ_{dly}. With No-TMR, the DFFs are not mitigated. Hence $P_{DFFSEU \rightarrow SEU} > 0$ and there is a $\tau_{dly} fs$ dependence. It is known that:

$\tau_{dly}|_{WSR0} < \tau_{dly}|_{WSR8}$ (Fig. 6) and $\sigma_{SEU} \propto (1-\tau_{dly} fs)$ (as shown in (7)), hence it follows that No-TMR: $\sigma_{WSR0_SEU} > \sigma_{WSR8_SEU}$. This can be further observed using the REAG FPGA SEU Model and σ_{SEU} data. Equation (16) reflects the σ_{SEU} heavy ion data in Fig. 7 and the fact that $\sigma_{WSR0_SEU} > \sigma_{WSR8_SEU}$.

$$(P(fs)_{DFFSEU \rightarrow SEU} + P(fs)_{SET \rightarrow SEU})|_{WSR_0} > (P(fs)_{DFFSEU \rightarrow SEU} + P(fs)_{SET \rightarrow SEU})|_{WSR_8} \quad (16)$$

There is no combinatorial logic in the WSR_0 string; hence the left side of (16) is reduced and forms (17).

$$(P(fs)_{DFFSEU \rightarrow SEU})|_{WSR_0} > (P(fs)_{DFFSEU \rightarrow SEU} + P(fs)_{SET \rightarrow SEU})|_{WSR_8} \quad (17)$$

Substitutions are made for $P(fs)_{DFFSEU \rightarrow SEU}$ and $P(fs)_{SET \rightarrow SEU}$ (17) to form (18):

$$P_{DFFSEU}\left(1 - \frac{\tau_{dly}|_{WSR_0}}{\tau_{clk}}\right) > P_{DFFSEU}\left(1 - \frac{\tau_{dly}|_{WSR_8}}{\tau_{clk}}\right) + \sum_{i=1}^{8} P(fs)_{SET \rightarrow SEU(i)} \quad (18)$$

Equation (18) reveals the tdly significance with respect to the σ_{SEU}. In addition, rearrangement (18) leads to (19) and shows that DFFs are more SEU susceptible than combinatorial logic.

$$P_{DFFSEU} > \frac{\tau_{clk}}{\tau_{dly}|_{WSR_8} - \tau_{dly}|_{WSR_0}} \sum_{i=1}^{8} P(fs)_{SET \rightarrow SEU(i)} \quad (19)$$

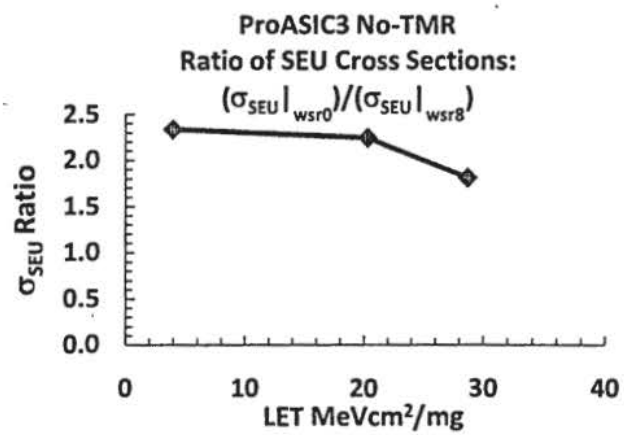

Fig. 8: Ratio of ProASIC3 No-TMR WSR_0 to WSR_8 σ_{SEU} across LET

A more detailed inspection of relative σ_{SEU}'s for the ProASIC3 No-TMR WSR_0 and WSR_8 is illustrated in Fig. 8. It can be seen that as LET increases, the ratio of WSR_0 to WSR_8 slightly decreases. This can be explained using (17) or (18). As LET increases, SETs increase in significance. Consequently, the $P(fs)_{SET \rightarrow SEU}$ component becomes more significant and subsequently reduces the relative difference between σ_{WSR0_SEU} and σ_{WSR8_SEU}.

B. ProASIC3 LTMR-WSRs: $P_{SET \rightarrow SEU}$

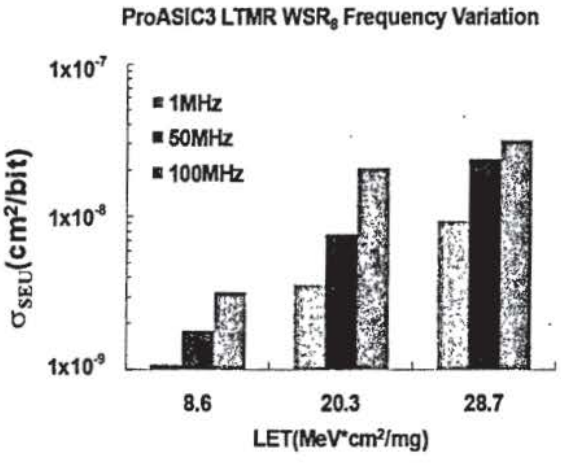

Fig. 9: ProASIC3 LTMR WSR_0, WSR_8 and. As the frequency increases or the number of combinatorial blocks increases, the σ_{SEU} increases.

Fig. 7 illustrates that with user-inserted LTMR, the overall σ_{SEU} is reduced and now $\sigma_{WSR0_SEU} < \sigma_{WSR8_SEU}$. This is as expected because $P(fs)_{DFFSEU \rightarrow SEU}$ is mitigated with LTMR. Consequently, with LTMR insertion, $P(fs)_{SET \rightarrow SEU}$ is now the significant component. In addition the σ_{SEU} data in Fig. 7 and Fig. 9 show the dominance of $P(fs)_{SET \rightarrow SEU}$ for a LTMR design. Given the σ_{SEU} data, the dominance of $P(fs)_{SET \rightarrow SEU}$,

and the effects of (18), the following hold true for LTMR ProASIC3 designs:

- As the number of combinatorial logic gates increases, $P(fs)_{SET \rightarrow SEU}$ increases and hence σ_{SEU} increases. i.e. LTMR $\sigma_{WSR0_SEU} < \sigma_{WSR8_SEU}$, as illustrated in Fig. 7
- As frequency increases, σ_{WSRN_SEU} also increases, as illustrated in Fig. 9

C. *ProASIC3 versus RTAXS Analysis*

1) *RTAXS Embedded LTMR versus LTMR-ProASIC3*

Fig. 10 is a comparison between RTAXS WSRs (contains embedded LTMR) with the ProASIC3 WSRs (contains user inserted LTMR). It is shown that although the RTAXS has an overall lower σ_{SEU}, the LTMR'd ProASIC3 σ_{SEU} are not drastically higher. In addition, the data shows that the LET threshold (LET_{TH}) for the LTMR'd ProASIC3 is statistically similar to the RTAXS.

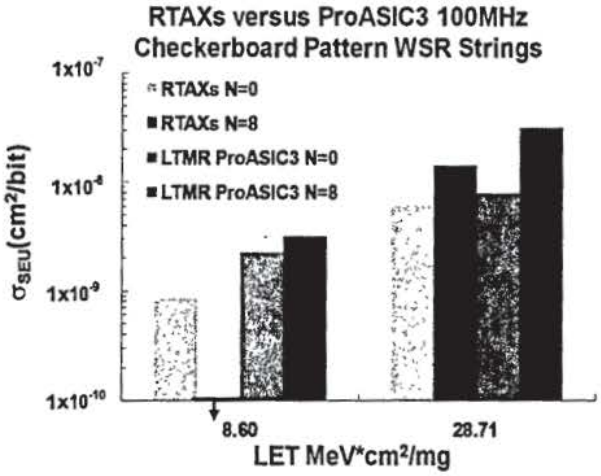

Fig. 10: RTAXS with embedded LTMR versus ProASIC3 with user inserted LTMR. WSR Test Structures

ProASIC3 σ_{WSRN_SEU} are higher than RTAXS σ_{WSRN_SEU} for two major reasons:

1. The ProASIC3 is a commercial grade part containing gates with switching rates considerably higher than the RTAXS[4][6]. In addition, the routing network of the ProASIC3 has less capacitive loading than the RTAXS as fan-out and length increases. By definition, faster switching rates and less capacitance lead to a higher SET P_{prop} than slower circuits that contain significant capacitive loading.
2. The RTAXS embedded mitigation scheme uses a wired-or as a voter[3][4]. The wired–or does not contribute to the σ_{SEU} because it does not use transistors to perform the voting. However, the ProASIC3 voters utilize a number of transistors to perform the "best-two-out-of-three function and hence have a significant contribution to the overall σ_{SEU}. Fig. 6 illustrates the difference between RTAXS and ProASIC3 mitigation schemes.

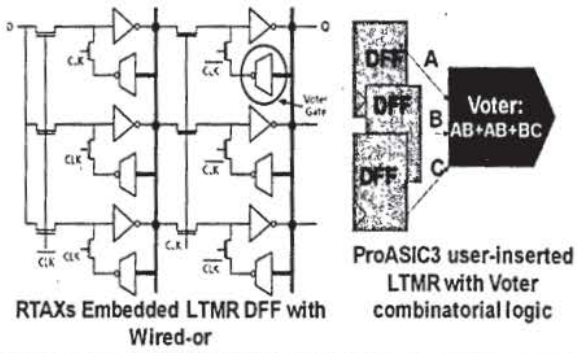

Fig. 11: RTAXS embedded LTMR[4] versus ProASIC3 user-inserted LTMR

2) *σ_{SEU} reduction with an increase in combinatorial logic: ProASIC3 versus RTAXS*

As previously mentioned, one would expect that $\sigma_{WSR0_SEU} < \sigma_{WSR8_SEU}$ because WSR_8 chains have more logic (i.e. WSR_8 contains more combinatorial logic between DFF stages than WSR_0). However, we have shown that this is not always the case. In support, Fig. 7 illustrates that across all LET values the No-TMR-ProASIC3 $\sigma_{WSR0_SEU} > \sigma_{WSR8_SEU}$. This No-TMR trend is due to dominant $P(fs)_{DFFSEU \rightarrow SEU}$ and τ_{dly}. By inserting LTMR, the data shows that the trend reverses. For LTMR-ProASIC3 $\sigma_{WSR0_SEU} < \sigma_{WSR8_SEU}$ for all LET values due to the mitigation of $P(fs)_{DFFSEU \rightarrow SEU}$.

Regarding the SEU response to increasing combinatorial logic in the RTAXS, it has also been observed that an increase in combinatorial logic at LET <10MeV*cm^2/mg can reduce σ_{SEU} due to attenuation of SETs [2]. Although the RTAXS and the No-TMR ProASIC3 both have trends where $\sigma_{WSR0_SEU} > \sigma_{WSR8_SEU}$, the conditions and rationales for the unexpected SEU response are completely different.

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TABLE 5: COMPARISON OF PROOFS EXPLAINING WHY $WSR_8\ \sigma_{SEU} < WSR_0\ \sigma_{SEU}$ PROASIC3 VERSUS RTAXS

	No-TMR ProASIC3	RTAXS embedded LTMR
Significant component	$P_{DFFSEU}(1-\tau_{dly}fs)$	$P_{gen}P_{prop}\tau_{width}fs$
Significant circuit type	DFF (sequential): SEU	Combinatorial: SET
Error Strength	One sided function is generally strong (assuming SEU is not a metastable event). Has the strength to propagate to the End-Point DFF	Two-sided function. Low LETs produces small SETs. Higher LETs produce larger SETs with more energy to propagate to End-Point DFF
Variables responsible for $WSR_8\ s_{SEU} < WSR_0\ s_{SEU}$	$\tau_{dly} * fs$ or τ_{dly}/τ_{clk}	P_{prop} or τ_{width}
LET values when valid	Across all LETs because τ_{dly} is constant and P_{DFFSEU} remains significant	Non-Linear across LET because P_{prop} is weaker at low LETs

Table 5 provides the variation in factors that influence the $\sigma_{WSR0_SEU} > \sigma_{WSR8_SEU}$ response for No-TMR ProASIC3 and RTAXS WSRs.

D. DTMR ProASIC3 Results and P_{SEFI}

Equation (13) shows that DTMR mitigates all of $P(fs)_{functionalLogic}$ forcing P_{SEFI} to be the dominant σ_{SEU}. Subsequently, DTMR FPGA designs facilitate test and analysis of P_{SEFI}.

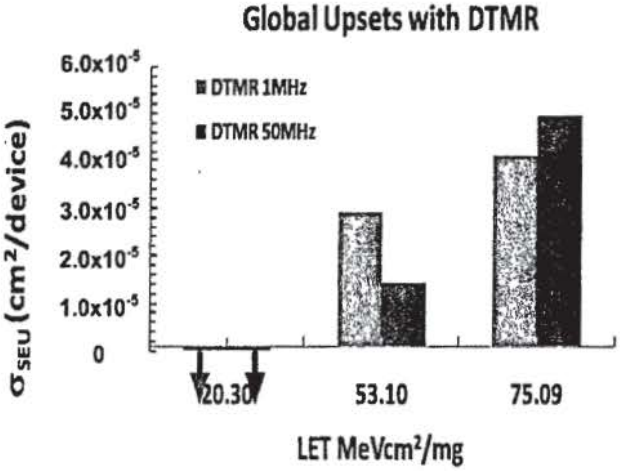

Fig. 12: DTMR WSR Global Route SEU Cross Sections operating at 50MHz and 1MHz with checkerboard data pattern. Cross Sections are per device. No Global SEUs were observed below LET = 20.3MeVcm²/mg at 50MHz

It is noted that no global route upsets were observed below 53.1MeV*cm²/mg for WSR strings. However, for more complex test structures, global route upsets were observed at 20.3 MeV*cm²/mg and above [5]. More testing is expected to be completed to increase statistics and enhance ProASIC3 global route analysis.

Global routes are expected not to have a frequency dependence because they are not captured SEUs. However, they can cause a SEU to be captured. As an example, a SET that occurs on a global route (e.g. a clock) can cause a DFF to capture the state of its data pin at an erroneous point in time regardless of clock frequency. The σ_{SEU} data reflects this assumption and does not show frequency dependence.

As previously mentioned, global routes are designed to connect to a large number (tens of thousands) of DFF clock or reset pins. Generally their routing structures are accomplished as a tree of buffers [1][4][6]. The buffers are required to have switching rates (rise-fall times) in the picoseconds range while driving a considerable capacitive load. The σ_{SEU} data in Fig. 12 shows a relatively high LET_{TH} for global routes. This suggests that ProASIC3 global networks have an inherent hardness due to their high-drive capability and capacitive damping throughout their routes.

VIII. CONCLUSION

The NASA REAG FPGA SEU testing methodology has been applied to Actel RTAXS and ProASIC3 FPGA devices. Because the ProASIC3 is a commercial grade device, mitigation strategies have been inserted into the DUT designs. Each design with and without mitigation has been evaluated to determine the effectiveness of the various mitigation strategies.

During the development and test phases, high level REAG FPGA SEU models assisted with DUT design creation and were used as points of reference during testing. Post-irradiation, SEU test results were analyzed and applied to the expected SEU probability models to develop more precise models. The refined FPGA SEU models have proven to reliably reflect the σ_{SEU} data, mitigation strategy, and synchronous design component effects (DFFs and combinatorial logic).

Regarding heavy-ion data, ProASIC3 LTMR has proven to improve SEU performance with respect to No-TMR ProASIC3 designs by increasing the LET_{TH} to near 8.6MeV*cm²/mg and reducing the overall σ_{SEU}.

When comparing the LTMR ProASIC3 to the RTAXs SEU data, it has been shown that the ProASIC3 LTMR LET Threshold (LET_{TH}) is compatible with the RTAXS LET_{TH}. However, the overall ProASIC3 LTMR cross sections are higher than the RTAXS cross sections. In addition, σ_{SEU} reduction was observed as the number of combinatorial logic blocks were increased for both devices. However, it has been shown that the cause for the σ_{SEU} reduction in both devices and when it occurs are due to completely different conditions.

Using the REAG FPGA model illustrated why DTMR isolates P_{SEFI} and subsequently is an effective method for test and evaluation of P_{SEFI}. Heavy ion data show that ProASIC3 DTMR has improved the SEU response by increasing LET_{TH} to near 20MeV*cm²/mg.

The testing methodology developed by NASA REAG

includes test preparation, test execution, and data analysis. The approach has proven to be a successful, technology-independent means to facilitate device evaluation and comparison studies.

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