

Prolonged 500 °C Operation of 100+ Transistor Silicon Carbide Integrated Circuits

David J. Spry^{1,a}, Philip G. Neudeck^{1,b*}, Dorothy Lukco², Liangyu Chen³, Michael J. Krasowski¹, Norman F. Prokop¹, Carl W. Chang², and Glenn M. Beheim¹

¹NASA Glenn Research Center, 21000 Brookpark Rd., Cleveland, OH 44135 USA

²Vantage Partners LLC, NASA Glenn, 21000 Brookpark Rd., Cleveland, OH 44135 USA

³OAI, NASA Glenn, 21000 Brookpark Rd., Cleveland, OH 44135 USA

^aDavid.J.Spry@nasa.gov, ^bNeudeck@nasa.gov

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Abstract. This report describes more than 5000 hours of successful 500 °C operation of semiconductor integrated circuits (ICs) with more than 100 transistors. Multiple packaged chips with two different 4H-SiC junction field effect transistor (JFET) technology demonstrator circuits have surpassed thousands of hours of oven-testing at 500 °C. After 100 hours of 500 °C burn-in, the circuits (except for 2 failures) exhibit less than 10% change in output characteristics for the remainder of 500 °C testing. We also describe the observation of important differences in IC materials durability when subjected to the first nine constituents of Venus-surface atmosphere at 9.4 MPa and 460 °C in comparison to what is observed for Earth-atmosphere oven testing at 500 °C.

Introduction

Most envisioned applications of $T > 450$ °C silicon carbide integrated circuits (SiC ICs) require long-term operation in extreme conditions. Of the variety of SiC device approaches investigated to date for possible use in such applications [1,2], only SiC junction field effect transistor (JFET) ICs have reported 1000+ hours of 500 °C SiC integrated circuit operation [3-7] and 521 hours of operation directly exposed to the corrosive 9.4 MPa 460 °C Venus surface environment [8]. Inherent advantages of SiC JFET device structure towards achieving prolonged $T > 450$ °C operation include all-pn-junction isolation and insensitivity to p-type contact resistance. While more recent demonstrations of these JFET IC have employed two levels of interconnect to support greatly increased IC complexity, the initial reported prototypes were limited to 24 transistors or less per circuit. This work describes the first long-term 500 °C experimental demonstration results from substantially up-scaled complexity SiC JFET ICs of more than 100 transistors per chip/circuit.

Experimental

Process. The 10-mask IC fabrication process implemented on a 76mm diameter SiC epiwafer is nearly identical to previous two-level interconnect 4H-SiC JFET IC wafer process runs [3-7], except that a modified mask layout with more complicated circuitry was employed, the 1360 °C implant activation anneal was extended from 4 hours to 100 hours (with the aim of higher degree of implant dopant activation), and the contact to SiC was a 50 nm titanium layer instead of hafnium. Laboratory procedures and hardware intended to minimize/address previously reported JFET IC fabrication non-idealities [5] including sodium contamination were employed.

Circuits. Two technology demonstration digital IC designs were implemented using a depletion-mode SiC JFET logic gate circuit approach [9]. The first IC (Fig. 1a) is a 195-transistor 16-bit random access memory (RAM) configured in a 4x4 array of 6-transistor memory cells with supporting address/read/write drive/sense circuitry. The second IC (Fig. 1b) is a 175-transistor clock signal generator with electronically selectable divide by 2 or 4 output signal ($\div 2/\div 4$ Clock) achieved using

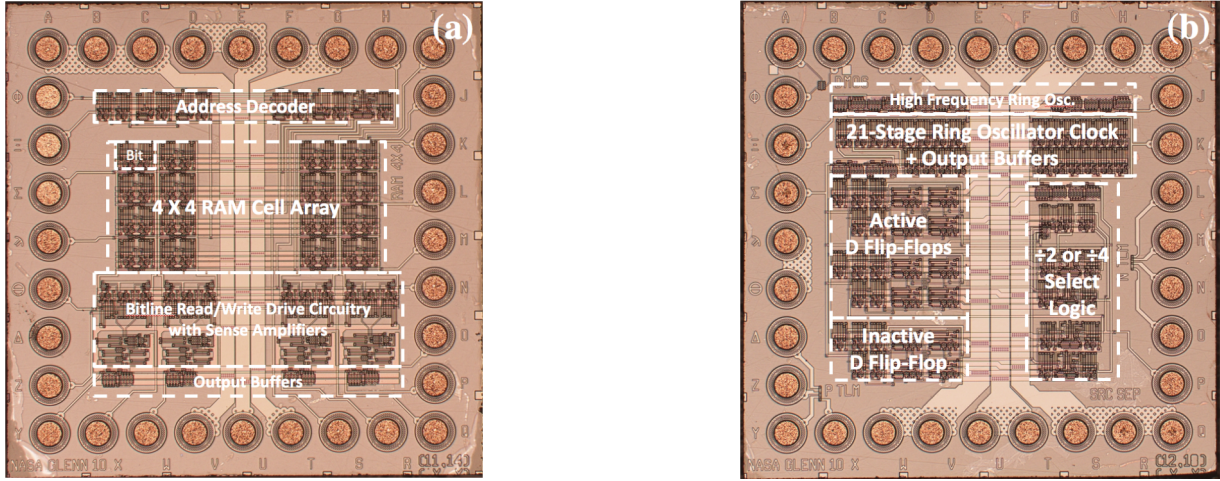


Fig. 1. Optical images of 3mm x 3mm 500 °C durable 4H-SiC JFET demonstration ICs prior to packaging. Annotations denote functional subcircuit blocks of each IC. (a) RAM chip with 195 JFETs. (b) $\div 2/\div 4$ clock chip with 175 active JFETs.

control logic and D-type flip flops. Both designs represent nearly an order of magnitude increase in circuit complexity and transistor count over prior 1000+ hour 500 °C durable JFET IC reports [3-7].

25 °C Probe Testing. The wafer was electrically mapped via probe-test measurements at 25 °C prior to wafer dicing and circuit packaging. Substantial systematic dependence of JFET threshold voltage V_T on device distance from the center of the wafer (r) quantitatively consistent with a prior JFET IC was observed (see [10] for details and its mitigation in circuit design). Table I presents the IC wafer map yield statistics for regions within 25 mm of the wafer center where JFET V_T fell within designed circuit specifications of $|V_T| < 10$ V. As seen in Table I, 25 °C functional circuit yields around 70% were obtained.

Table I. 25 °C Probe Test Yield for 100+ JFET SiC ICs

Demonstration IC	IC JFET Count	# Good/# Tested $r \leq 25$ mm	% Yield $r \leq 25$ mm
16-bit RAM	195	19/27	70%
$\div 2/\div 4$ Clock	175	19/26	73%

Prolonged 500 °C Testing. Following probe testing, the wafer was diced into 3 mm x 3 mm chips and selected functional chips were bonded into high-temperature-durable packaging [11] for prolonged 500 °C testing in room-air ovens. Table II summarizes the results to date of these tests, some of which are on-going past 5000 hours of 500 °C circuit operation. Figures 2 and 3 respectively show recently measured 500 °C functional waveforms from a $\div 2/\div 4$ clock IC (#2, Table II) and a RAM IC (#2, Table II). Figure 4 plots measured 500 °C testing time evolution of base frequency f_{CLK} and output high V_{OH} and output low V_{OL} voltages for the clock ICs. Following the first 100 hours of

Table II. Summary of 500 °C Packaged IC Tests

Packaged IC Sample	500 °C Test Hours	Status
16-bit RAM #1	1525 h	Suspended
16-bit RAM #2	5040 h	Running
$\div 2/\div 4$ Clock #1	470 h	Failed
$\div 2/\div 4$ Clock #2	5200 h	Running
$\div 2/\div 4$ Clock #3A	4377 h	Running
$\div 2/\div 4$ Clock #3B	4377 h	Running
$\div 2/\div 4$ Clock #3C	2090 h	Failed

RAM#1 was tested as 12-bit due to damage/failure of one row/word line during packaging.

Clock chips 3A, 3B, 3C reside in same package.

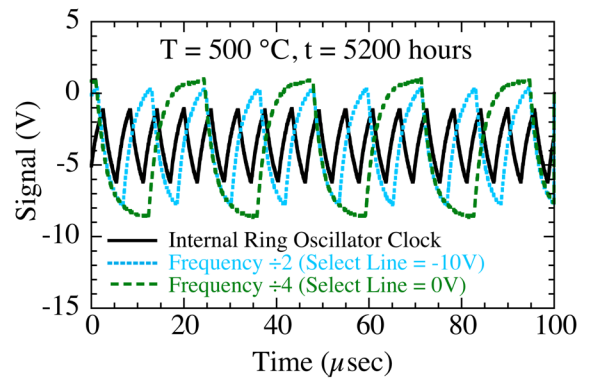


Fig. 2. Measured waveforms showing operation of $\div 2/\div 4$ clock IC at 5200 hours of 500 °C oven testing.

initial 500 °C burn-in, the circuits (except for the two failures noted in Table II) exhibit less than 10% change in output characteristics for the remaining thousands of hours of 500 °C operational testing conducted to date. The data shown in Table II demonstrate an unprecedented and mission-enabling combination of 500 °C IC durability and complexity. All IC failures studied to date have been traced to oxidation-induced open-circuiting of TaSi₂ interconnect initiated at cracks in overlying dielectric that on-going research is seeking to mitigate [7,12].

Venus Environment Durability. A previously reported 3-week demonstration of SiC JFET IC operation directly immersed/exposed (no package lid) in 9.4 MPa, 460 °C atmospheric composition found at the surface of Venus (CO₂, N₂, SO₂, H₂O, CO, OCS, HCl, HF, and H₂S) [8] combined with the above Earth-atmosphere results have spurred development of new Venus lander mission concepts and hardware with the goal of returning long-term scientifically important measurements from the surface of Venus. The Long-Lived In-Situ Surface Explorer (LLISSE) [13] is one such initial mission concept example of a > 100-fold smaller/lighter Venus lander with > 100-fold longer surface mission duration that uniquely demonstrated SiC JFET IC Venus-environment durability could enable.

Materials analysis studies (to be published elsewhere) conducted on samples from the 3-week Venus surface environment IC test [8] indicate that important chemical reactions occur in the Venus atmosphere that are not observed in T > 460 °C Earth-atmosphere oven-testing. Transition metals react to form sulfides in the Venusian environment, while SiC, SiO₂, Al₂O₃ remain stable. Exposed bare Pt film (200 nm thick) forms PtS whiskers, but the same Pt film over-coated and anneal-mixed with 1 μm Au film forms PtS spheres.

The dielectric stack for the TaSi₂ IC interconnects [3-7] behaves very differently in Venus-atmosphere testing compared to Earth air testing. Figure 5a shows a microscopic cross-section of typical dielectric cracking observed after prolonged T ≥ 500 °C testing in Earth air [12]. The crack reaches the TaSi₂ layer and then the TaSi₂ itself oxidizes tens of microns on either side. As the TaSi₂ oxidizes, its volume increases, exacerbating the cracking process. In contrast, Figure 5b shows the microscopic cross-section of a crack examined in the sample tested for 3 weeks in Venus surface environment. The crack did not propagate into the

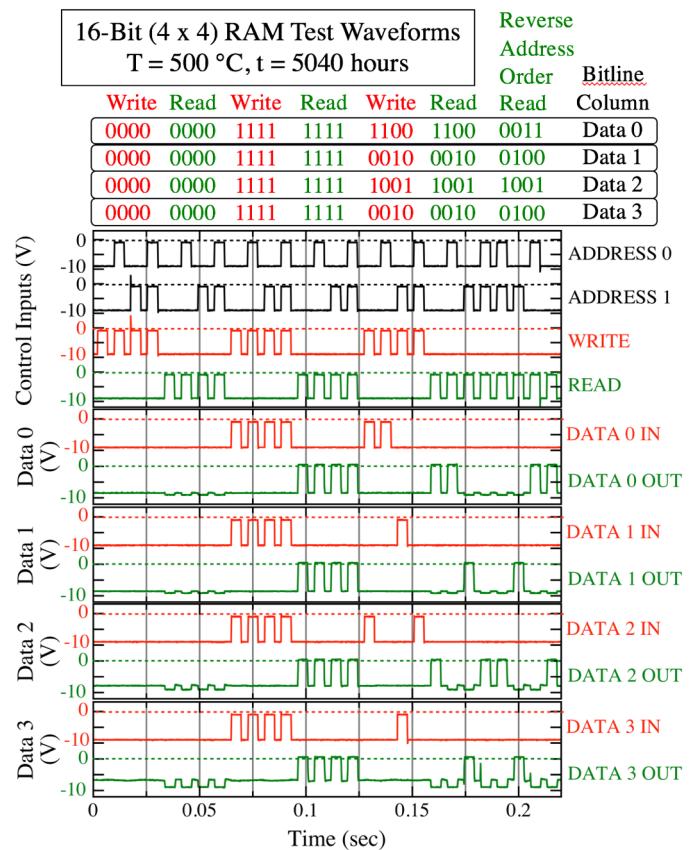


Fig. 3. Measured 16-bit RAM waveforms showing read and write functionality of all bits at 5040 hours of a 500 °C oven test.

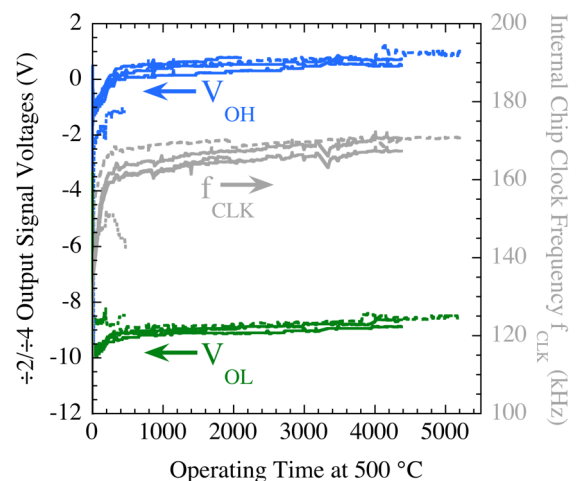


Fig. 4. Time evolution of ÷2/÷4 clock IC output properties for 5 chips in 500 °C oven testing. 3 of 5 chips remain functioning under test.

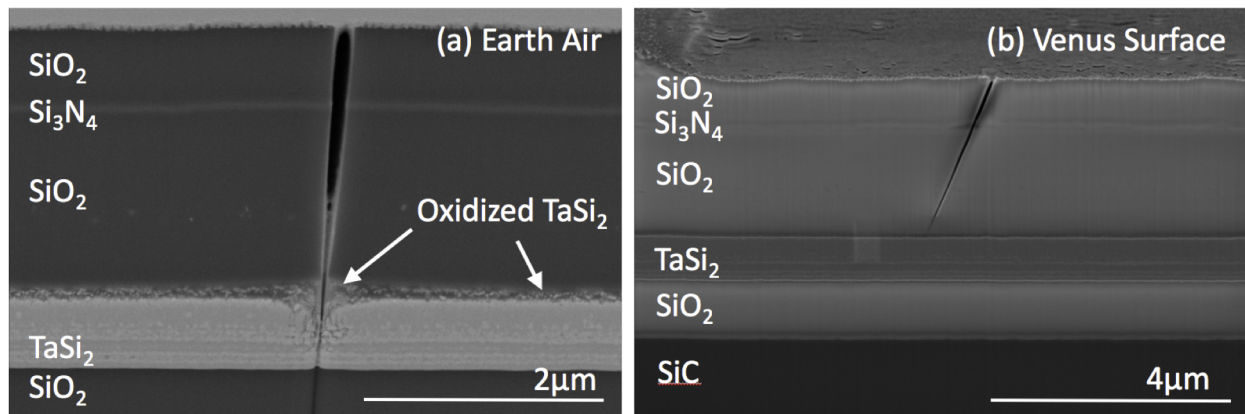


Fig. 5. Microscopic cross-sections of: (a) Crack typical of prolonged $T \geq 500$ °C testing in air (727 °C for this sample) [13]. The crack allows the top surface of the TaSi₂ film to oxidize which exacerbates failure. (b) Crack in IC sample tested in Venus surface condition. The crack reaches the top of the TaSi₂ but does not propagate through the TaSi₂ and there is no observable evidence of TaSi₂ film oxidation.

TaSi₂ and there is no evidence of TaSi₂ oxidation with associated film expansion (swelling).

From the materials study results obtained to date, we conclude that high-fidelity reproduction of the Venus surface environment is a critical necessity for proper development and qualification of electronics intended for long-term operation of Venus surface missions. Temperature and/or pressure without including the complete chemistry (including trace amounts of HCl at 0.5 ppm and HF at 2.5 ppb that were found as reacted products in some samples) is not a sufficient means of screening electronics for long-term operation in the Venusian surface environment.

Summary

The complexity of 4H-SiC JFET IC's proven durable for 1000's of hours at 500 °C has been substantially increased from 24 transistors to 175+ transistors. Testing in high-fidelity reproduction of the Venus surface environment is necessary to continue electronics development and qualification testing building towards long-term Venus surface missions.

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