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# Life Cycle Analysis of a SpaceCube Printed Circuit Board Assembly Using Physics of Failure Methodologies

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## Executive Summary

In this reliability life cycle evaluation of the SpaceCube 2.0 processor card, a partially populated version of the card is being evaluated to determine its durability with respect to typical GSFC mission loads. The card under study has two column grid array (CGA) Xilinx Virtex 5 FPGAs and two cPCI connectors mounted on an Isola P95 polyimide multilayer printed wiring board. The revised design is suggested for future use in the SpaceCube processor platform.

The surface mount FPGAs are a change to the previous SpaceCube design and are potentially a source of early failures given the accumulation of stresses and consequently, damage that a printed wiring assembly undergoes throughout the NASA integration and testing cycle, launch, and low earth orbit thermal cycles.

Using the University of Maryland's CALCE SARA (Center for Advanced Life Cycle Engineering Simulation Assisted Reliability Assessment) advanced life cycle analysis software, this assembly has been virtually built, analyzed and evaluated using a Monte Carlo analysis for two on-orbit cases: no thermal control (i.e., heaters) to control the amount of thermal fluctuation and with active thermal heating to maintain the board at 20°C at the cold extremes of low earth orbit.

In addition to the two life cycle evaluation cases on this assembly, a third environmental case was built in CALCE to model a thermal vacuum cycling test being conducted by the SpaceCube team between -55°C

and 100°C . This test has experienced a single failure, and the number of thermal cycles to failure did fall within reasonable limits of the prediction software. While a single point is not enough information to validate a model's ability to predict failure, it does indicate that the model could possibly be a predictor of the on-orbit life cycle reliability.

If the model can be used as a reasonable predictor of the reliability of the board assembly, then the results indicate that the design would generally not fully meet mission reliability needs for even Class D and C low earth orbit (LEO) expected mission lives (<2 years per NASA NPR 8705.4) without significant improvement in robustness of the board assembly in a single string mission architecture. Redundancy would not necessarily improve reliability since both printed circuit boards will accumulate similar levels of environmentally caused damage over the I&T and mission life cycle. Experience at GSFC has shown a board level reliability allocation of 99% or above is needed to maintain the overall mission reliability to acceptable levels.

At 99% reliability, the modeled lifetime was estimated to be 245 days (8 months), which falls short of fully meeting Class C and D expected mission lives by nearly 1-1/2 years.

The critical predicted failure mode is an electrical open in the CGA solder joints due to thermally induced fatigue. A design change to the board material to better match the coefficients of thermal expansions between Printed Wiring Board (PWB) and the chip carrier material on the FPGAs is recommended. It may also warrant very specific control limits of on-orbit thermal extremes in order to minimize the thermally induced strains.

Some basic comparisons of the average effects of different printed wiring board materials and varying dimensional features are discussed, and future detailed analysis and trade studies using the CALCE SARA PWA model and Monte Carlo analysis capabilities are recommended. The goal of the trade study would be to find a design that maximizes the on-orbit life of the column grid array solder joints, while avoiding an increase in the failure likelihood from one of the other previously benign failure modes modeled, such as a plated through hole failure.

# Contents

# Figures

Tables

# Introduction

The Center for Advanced Life Cycle Engineering Simulation Assisted Reliability Assessment software (University of Maryland, College Park, MD, 2014) (hereafter referred to by its acronym, CALCE SARA) features a suite of tools that can analyze the reliability of printed wiring assemblies (PWAs) that are subjected to vibration and thermal cycling environments. This includes the printed circuit board (PCB), electrical, electronic, & electromechanical (EEE) parts, as well as the interconnects. With the tool, the user creates a virtual model of the PWA specific design and quality parameters, and defines environmental conditions. Thermal and vibration analyses may be simulated, in addition to life cycling. The software utilizes a physics-of-failure approach to execute algorithms and output an array of performance information, potential failure mechanisms, and quantified expected life.

In this, CALCE SARA implements an easy-to-use methodology to validate designs and assess risk of PWAs. Because the simulation is in an entirely virtual environment, design parameters can be manipulated, and the high cost or complications associated with real-life testing can be minimized. Use of model-based assurance and design validation has great potential for NASA, and this exercise with CALCE SARA explores utility for electronic systems.

The SpaceCube project at NASA Goddard Space Flight Center (GSFC) is seeking to use a newly designed processor card which features two XILINX Virtex-5QV FPGAs, a ceramic column grid array package. A simulation of this PWA was created in CALCE SARA to evaluate its expected life, and to compare the results with the limited thermal cycle testing being performed by the project in a GSFC laboratory.

The objectives of this CALCE SARA PWA exercise included:

1. Run a lifecycle analysis of an actual assembly, applying typical thermal and vibration loading profiles. These include loads experienced during qualification and testing, launch, and 2 variations of a low earth orbit (LEO) thermal profile.
2. An evaluation of the expected life time with respect to an estimated reliability need of 99% at 5 years for a single critical electronics card.
3. Using CALCE SARA PWA software to replicate an unpowered thermal vacuum cycling test being performed by the SpaceCube project.
4. Use the results to evaluate the software's capabilities for PWA design validation and risk assessment.
5. Identify and vary PCB parameters that could affect the PWA reliability.
6. Apply the knowledge from the simulations to rank any identified risks and recommend potential mitigations for the project.

# Methodology

A diagram of the basic methodology utilizing the CALCE SARA PWA software is shown below, and in addition, a short summary describing the steps to performing the life cycle study on this specific board follows:

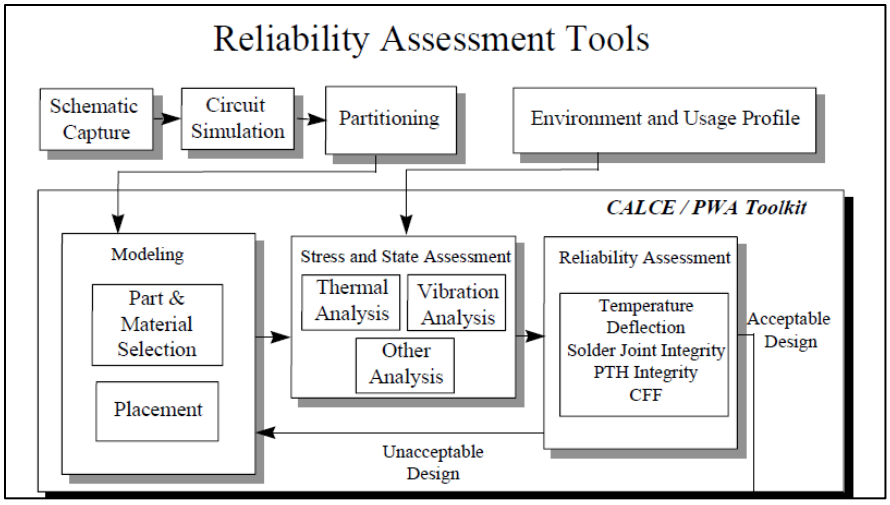



*Figure 1. Diagram showing inputs, processes and outputs for performing PWA life cycle analysis with CALCE SARA PWA (Osterman & Stadterman, 1999).*

- Determine which life cycles the board should see and the details of each. In this report, there will be three cases under study.
    - **Case 1:** The populated processor card (PWA) will virtually undergo environmental testing as specified in GSFC-STD-7000A, General Environmental Verification Standard (GEVS) for GSFC Flight Programs and Projects. Specifically protoflight levels of vibration and thermal testing, acceptance level launch random vibration loads (to simulate the actual launch), thermal vacuum test conditions and finally, thermal cycling at 16 times per day between hot and cold states to simulate a low earth orbit. The processor board will not have active thermal controls to prevent the board temperature from drifting below 20°C. The components U2 and U3 will be powered to their maximum estimated power dissipation of 5.9 watts.
    - **Case 2:** The same case as Case 1, but the processor card (PWA) will utilize thermal boundary conditions reflective of having thermostatically controlled heaters to maintain the board at a minimum temperature of 20°C at the cold cycle of the orbit.
    - **Case 3:** A special case being used to simulate an unpowered thermal vacuum test of a processor card (PWA) populated the same as the simulated design. The testing has been ongoing and there has been 1 recorded failure at the time of this writing.
- Obtain the details of the SpaceCube board under study, including drawings, and CAD models if available.
- Input the board design, either by import or manual interface provided in the CALCE SARA PWA software. For this study, an ODB++ file was made available and the details of the printed wiring board were imported.
- Populate the PWA components under study; for this analysis, the components installed onto the PWB are as follows:
    - 2 each, Xilinx5 CGAs, shown as components U2 and U3 on the model.
    - 2 each, cPCI connectors, shown as J1 and J2 on the model.
- Input (into CALCE SARA PWA) the PWB layer stack-up per supplied drawings, including the material properties of each layer and percentage of metallization on each.
- Populate any material constants for items/materials not already resident in the CALCE SARA PWA materials library. In addition to the typical mechanical properties such as material strengths, moduli, and Poisson's ratios, other properties must be identified from literature or other

existing libraries, including coefficients of thermal expansion, thermal conductivity coefficients, fatigue exponents, etc.

- Populate dimensional and interconnect properties of components, including those that can be input as statistical distributions.
- Create each vibration analysis case in the CALCE SARA PWA vibration analysis module. For this study, there were two vibration cases created. The first case simulates the GEVS qualification level random vibration loads in the Z axis (perpendicular to the plane of the board) to simulate integration and testing (I&T) loads. The second simulates the actual launch environment at the GEVS acceptance level random vibration loads in the Z axis, which are lower than qualification levels. CALCE SARA PWA software does not have the ability to perform vibration analysis in the X and Y axes.
- Create steady state thermal analyses for each of the hot and cold cases described by each of the 3 lifecycle cases above. Once the results are generated for each, they will then be imported into the life profile module which describes the particular cycling rates and dwell times the processor board will see.
- Create the individual lifecycle profiles for each of the 3 cases. Each lifecycle profile describes which types and how much exposure to each type of loading the PWA will see. These will be used in the "Failure Analysis" module of CALCE. Temperature distribution sets (there are others, but temperature was the only ones populated on this study) will be created in this module as well in order to vary the resulting PWA temperatures to capture uncertainty in the results.
- Run the failure analysis for each of the lifecycle profiles. A built-in Monte Carlo simulation can be utilized, specifying the number of runs and the desired failure population. A component level failure view is displayed showing components that have passed or failed the lifecycle analysis at the specified failure levels, as well as the times to failure of each component after each run of the Monte Carlo simulation. The resulting outputs can be used directly or evaluated further using other statistical tools.

# Model Uncertainty

CALCE SARA PWA was designed primarily as a life cycle prediction tool that can use finite element outputs as inputs to its life prediction models in order to be able to predict and provide insight into the design weaknesses under the expected operating conditions that can limit the reliability of the printed wiring assembly under study.[1] Once weaknesses are identified, the software can aid the design and reliability engineers to optimize the design life by providing a virtual trade space in which different materials or environmental controls can be simulated to determine their effects over the desired lifetime and environment.

As with any model based analysis, best efforts are made to incorporate the most accurate information into the model, but even the best models are not able to perform a perfect prediction of real life. Uncertainties are always introduced either through the selection of the input variable values, as well as any possible approximations inherent in the modeling software that make a particular calculation less rigorous, saving processing time.

In addition to performing thermal and mechanical stress analyses, CALCE SARA PWA is able to apply statistical distributions for several of the input properties, as well as on the simulation results in order to provide bounds on the uncertainties involved in performing what would otherwise be a deterministic analysis.

[1] While CALCE SARA PWA does have the ability to perform both thermal and mechanical finite element analyses, that is not its primary function.

There are differences between a model and the actual behavior of the item under study, but understanding those uncertainties can help with the confidence in the results, and help give insight into how to reduce uncertainties in future versions of a particular analysis.

### 1.1.1 Aleatory Uncertainty

The ability to set up and perform a Monte Carlo analysis that simultaneously samples multiple variables is one of the advantages of using CALCE SARA PWA over some of the traditional finite element-only type software tools. The largest part of this uncertainty is the parametric uncertainty involving specifying material properties and the boundary conditions for the thermal and mechanical analyses. However, several of the material and attach property variables used as inputs to the thermal and mechanical analyses in CALCE SARA PWA can be input as statistical distributions. This functionality is also available to be applied to resulting vibration and temperature analysis outputs, which are then used as inputs to the life cycle analysis.

One source was the selection of the boundary conditions for the thermal analyses; these were based on typical design values and were not provided from a mission specific, more detailed thermal analysis or supporting test data results. Uncertainty with respect to this was input as a uniform distribution with a variation of +/-5°C (default from CALCE literature) on the resulting temperatures output from the thermal analyses.

In CALCE SARA PWA the two available input distributions are the uniform distribution and the triangular distribution. For this set of analyses, all distributions selected were uniform distributions with upper and lower limits specified. A list of variables that were input as distributions is shown below.

| Variable | Distribution | Upper Limit | Lower Limit |
|---|---|---|---|
| Component Attachment | | | |
| Solder Height (U2&U3) | Uniform | 0.1 mm | 0.001 mm<br><br>(CALCE recommended value between 0.08 and 0.025 mm) |
| Solder Bond Area (U2 & U3 CGA specification) | Uniform | 0.385 mm^2 | 0.3465 mm^2<br><br>(10% reduction in area from nominal pad area) |
| Standoff Height (U2 & U3 Drawing Tolerances) | Uniform | 2.35 mm | 2.05 mm |
| Post Thermal Analysis | | Upper Variation | Lower Variation |
| Maximum Package Temperature | Uniform | +5°C with respect to analysis result | -5°C with respect to analysis result |
| Minimum Package Temperature | Uniform | +5°C with respect to analysis result | -5°C with respect to analysis result |
| Package CTE | Uniform | 0.5 ppm/C | -0.1 ppm/C |
| Maximum Board Temperature | Uniform | +5°C with respect to analysis result | -5°C with respect to analysis result |
| Minimum Board Temperature | Uniform | +5°C with respect to analysis result | -5°C with respect to analysis result |

### 1.1.2 Epistemic Uncertainty

In addition to the statistical uncertainty of the inputs, the structure of a particular model itself also introduces uncertainty simply due to certain assumptions which may include or discount particular details.

For CALCE SARA PWA, an example of this is the ability to make finite element meshing finer or coarser, meaning there could potentially be some amount of lost detail in the output.

Some of the sources of the epistemic uncertainty in this analysis are:

- Using a 30 X 30 finite element mesh for the thermal analyses
- Using a 10 X 10 finite element mesh for the vibration analyses
- CALCE performs vibration analysis in the Z axis only (X and Y are performed in qualification testing as well as Z). Cumulative damage for the X and Y axes are not accumulated.
- Using a uniform distribution rather than a potentially more descriptive distribution such as a triangular distribution
- Running only 2000 Monte Carlo simulation runs; more runs could provide information on extreme cases

Assumptions in this model, which are justified in the relevant sections of the paper, included:

- The blind vias in the PCB were not represented, given that they would outlive PTHs.
- The PWA model was only populated with the FPGAs and cPCI connectors.
- An insulated boundary condition was used at the J1 and J2 connectors in the thermal analyses.
- The power dissipated in the cPCI connectors is very small and assumed to be nearly zero.
- The effect of heaters was simulated as a thermal boundary condition, as opposed to being defined as an actual component.
- The connector plate did not affect the clamping of the board to the structure.
- Qualification levels of integration & testing were assumed since it is unknown whether the design will be flown as a protoflight version.

# Model Definition

The printed circuit board and parts were first defined in the PWA Designer tool.

## PWA Creation from CAD Import

To create the baseline virtual model for this project, a computer-aided design (CAD) file was supplied by SpaceCube, which CALCE SARA could interpret and import directly into the program. This creates the board outer dimensions (190 mm x 100 mm x 2.873 mm) and places the components on the board. The PWA parts were limited to the FPGAs (CGA) and connectors to most accurately represent the configuration being investigated by the SpaceCube project.

In the SpaceCube life test, the board was partially populated with the FPGAs (CGA) and connectors, placed in a thermal vacuum chamber, and thermal-cycled to generate a number of cycles to failure. This was done for the purpose of studying the CGA reliability under severe thermal cycling conditions.

That same thermal test case was simulated in this analysis (Case 3) so the life test and modelled results could be directly compared. Future work could include performing this physics of failure analysis on the fully populated assembly.

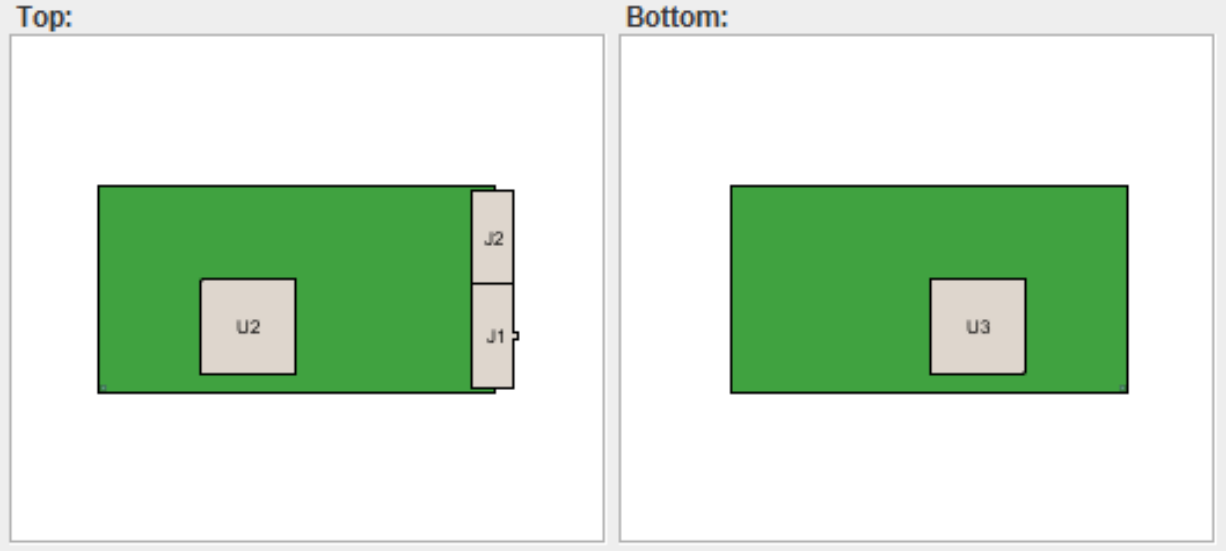



*Figure 2. PWA base model in CALCE SARA*

Note: U2 and U3 are aligned at the same location on each side.

## PWB Definition

The board material properties were assigned based upon an existing library within CALCE SARA as well as user-defined entries. The copper (pwb.Cu) and epoxy (pwb.epoxyF) materials were pre-existing in the library, while a material was created to represent the ISOLA P95 polyimide material (denoted as simply "polyimide" in the table below) which was specifically used in the SpaceCube board. The Arlon85NT polyimide material was also created to be used alongside the epoxy fiberglass material as a varied attribute in the SpaceCube life cycling analysis. The ISOLA P95 and Arlon 85NT materials were specified with the values from the manufacturer technical data sheets, or, where unspecified in some cases, typical polyimide values were assigned.

*Table 1. Board Materials*

| Material ID: | Material Name: | X Elastic Mod<br>MPa | Y Elastic Mod<br>MPa | Z Elastic Mod<br>MPa | XY Poisson's<br>dimensionles | YZ Poisson's | ZX Poisson's |
|---|---|---|---|---|---|---|---|
| Cu | Cu cold Rolled ... | 121000.0 | 121000.0 | 121000.0 | 0.345 | 0.345 | 0.345 |
| epoxyF | Epoxy Fiberglass | 17200.0 | 17200.0 | 17200.0 | 0.3 | 0.3 | 0.3 |
| polyimide | polyimide | 26834.0 | 26834.0 | 24062.0 | 0.187 | 0.164 | 0.164 |
| arlon85nt | Arlon 85NT | 22063.0 | 22063.0 | 22063.0 | 0.15 | 0.15 | 0.15 |

| Density: kg/m^3 | X Conductivity W/mC | Y Conductivity W/mC | Z Conductivity W/mC | X Coefficient ppm/C | Y Coefficient ppm/C | Z Coefficient ppm/C | Specific Heat J/(kg-degK) |
|---|---|---|---|---|---|---|---|
| 8940.0 | 418.0 | 418.0 | 418.0 | 17.0 | 17.0 | 17.0 | 385.0 |
| 1938.0 | 0.2 | 0.2 | 0.2 | 17.6 | 17.6 | 70.0 | 878.6 |
| 1420.0 | 0.4 | 0.4 | 0.4 | 13.0 | 13.0 | 55.0 | 1090.0 |
| 1370.0 | 0.2 | 0.2 | 0.2 | 9.0 | 9.0 | 93.0 | 1090.0 |

| Tensile Stren MPa | Glass Transit degC | Maximum Us degC |
|---|---|---|
| 221.0 | 1085.0 | 1085.0 |
| 276.0 | 130.0 | 130.0 |
| 249.0 | 260.0 | 140.0 |
| 45.0 | 250.0 | 393.0 |

The CAD import creates the board geometry, however the internal layer properties needed to be manually defined. This included the number of layers, thickness of each layer, and percent metallization (to determine the extent of circuit artwork or to define plane layers). The board stack-up from the project design drawing (not shown due to proprietary nature) was used to create the layer parameters, as well as circuit artwork provided by the program (also not shown).

*Table 2. Layer Definition*

| Position | Layer Id | Thickness<br>mm | Percent Metalli | Dielectric Mater | Metalization Ma |
|---|---|---|---|---|---|
| 1.0 | 1Layer_1 | 0.05334 | 50.0 | pwb.polyimide | pwb.Cu |
| 2.0 | 2Dielectric_1... | 0.1016 | 0.0 | pwb.polyimide | pwb.Cu |
| 3.0 | 3Layer_2 | 0.01524 | 98.0 | pwb.polyimide | pwb.Cu |
| 4.0 | 4Dielectric_2... | 0.0889 | 0.0 | pwb.polyimide | pwb.Cu |
| 5.0 | 5Layer_3 | 0.03048 | 95.0 | pwb.polyimide | pwb.Cu |
| 6.0 | 6Dielectric_3... | 0.1016 | 0.0 | pwb.polyimide | pwb.Cu |
| 7.0 | 7Layer_4 | 0.03048 | 95.0 | pwb.polyimide | pwb.Cu |
| 8.0 | 8Dielectric_4... | 0.0889 | 0.0 | pwb.polyimide | pwb.Cu |
| 9.0 | 9Layer_5 | 0.01524 | 98.0 | pwb.polyimide | pwb.Cu |
| 10.0 | 10Dielectric_... | 0.127 | 0.0 | pwb.polyimide | pwb.Cu |
| 11.0 | 11Layer_6 | 0.01524 | 20.0 | pwb.polyimide | pwb.Cu |
| 12.0 | 12Dielectric_... | 0.1143 | 0.0 | pwb.polyimide | pwb.Cu |
| 13.0 | 13Layer_7 | 0.01524 | 98.0 | pwb.polyimide | pwb.Cu |
| 14.0 | 14Dielectric_... | 0.127 | 0.0 | pwb.polyimide | pwb.Cu |
| 15.0 | 15Layer_8 | 0.01524 | 20.0 | pwb.polyimide | pwb.Cu |
| 16.0 | 16Dielectric_... | 0.1143 | 0.0 | pwb.polyimide | pwb.Cu |
| 17.0 | 17Layer_9 | 0.01524 | 98.0 | pwb.polyimide | pwb.Cu |
| 18.0 | 18Dielectric_... | 0.127 | 0.0 | pwb.polyimide | pwb.Cu |
| 19.0 | 19Layer_10 | 0.01524 | 20.0 | pwb.polyimide | pwb.Cu |
| 20.0 | 20Dielectric_... | 0.1143 | 0.0 | pwb.polyimide | pwb.Cu |
| 21.0 | 21Layer_11 | 0.05334 | 98.0 | pwb.polyimide | pwb.Cu |
| 22.0 | 22Dielectric_... | 0.127 | 0.0 | pwb.polyimide | pwb.Cu |
| 23.0 | 23Layer_12 | 0.05334 | 98.0 | pwb.polyimide | pwb.Cu |
| 24.0 | 24Dielectric_... | 0.1143 | 0.0 | pwb.polyimide | pwb.Cu |
| 25.0 | 25Layer_13 | 0.01524 | 20.0 | pwb.polyimide | pwb.Cu |
| 26.0 | 26Dielectric_... | 0.1143 | 0.0 | pwb.polyimide | pwb.Cu |
| 27.0 | 27Layer_14 | 0.01524 | 98.0 | pwb.polyimide | pwb.Cu |
| 28.0 | 28Dielectric_... | 0.1143 | 0.0 | pwb.polyimide | pwb.Cu |
| 29.0 | 29Layer_15 | 0.01524 | 20.0 | pwb.polyimide | pwb.Cu |
| 30.0 | 30Dielectric_... | 0.127 | 0.0 | pwb.polyimide | pwb.Cu |
| 31.0 | 31Layer_16 | 0.01524 | 98.0 | pwb.polyimide | pwb.Cu |
| 32.0 | 32Dielectric_... | 0.1143 | 0.0 | pwb.polyimide | pwb.Cu |
| 33.0 | 33Layer_17 | 0.01524 | 20.0 | pwb.polyimide | pwb.Cu |
| 34.0 | 34Dielectric_... | 0.127 | 0.0 | pwb.polyimide | pwb.Cu |
| 35.0 | 35Layer_18 | 0.01524 | 98.0 | pwb.polyimide | pwb.Cu |
| 36.0 | 36Dielectric_... | 0.0889 | 0.0 | pwb.polyimide | pwb.Cu |
| 37.0 | 37Layer_19 | 0.03048 | 95.0 | pwb.polyimide | pwb.Cu |
| 38.0 | 38Dielectric_... | 0.1016 | 0.0 | pwb.polyimide | pwb.Cu |
| 39.0 | 39Layer_20 | 0.03048 | 95.0 | pwb.polyimide | pwb.Cu |
| 40.0 | 40Dielectric_... | 0.0889 | 0.0 | pwb.polyimide | pwb.Cu |
| 41.0 | 41Layer_21 | 0.01524 | 98.0 | pwb.polyimide | pwb.Cu |
| 42.0 | 42Dielectric_... | 0.1016 | 0.0 | pwb.polyimide | pwb.Cu |
| 43.0 | 43Layer_22 | 0.05334 | 50.0 | pwb.polyimide | pwb.Cu |

An update to CALCE SARA (version 8.1) introduced the capability to import vias from the ODB++ board CAD file. The execution did not successfully interpret the blind vias in the design, predominantly located underneath the FPGAs. This was considered to be a minor omission for this analysis, given that blind vias will outperform through-hole vias in the context of barrel plating failures, which is the only PTH failure mode assessed by the software. In reality, the blind vias may have had a slight impact on the thermal and vibrational analyses, given the additional metallization for heat transfer and stiffening. However, the failure mechanisms in the thermal and vibration analysis are dominated by other factors, including the laminate material expansion properties and the part mass, respectively. Thus it is assumed that the blind vias would have a negligible impact on this analysis, and they were left out of the model. Future updates to the CALCE SARA software to read in the blind via features could resolve this discrepancy.

The original unpopulated board drawing (ODB++ format) file was imported into CALCE SARA (figure was omitted due to proprietary design information). Figure 3 and Figure 4 show the resulting models as interpreted by CALCE SARA PWA.

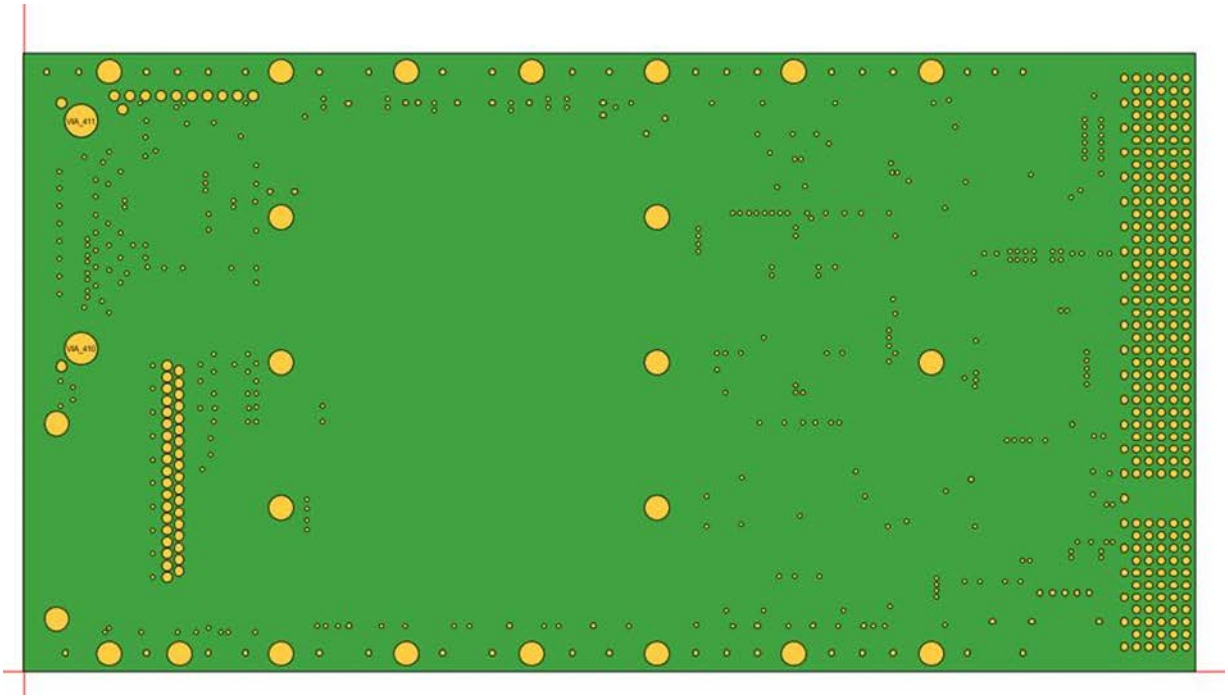


*Figure 3. Drilled holes as imported from the project drawing ODB++ file and viewed in CALCE SARA PWA.*

The final board configuration with components and vias appears as below.

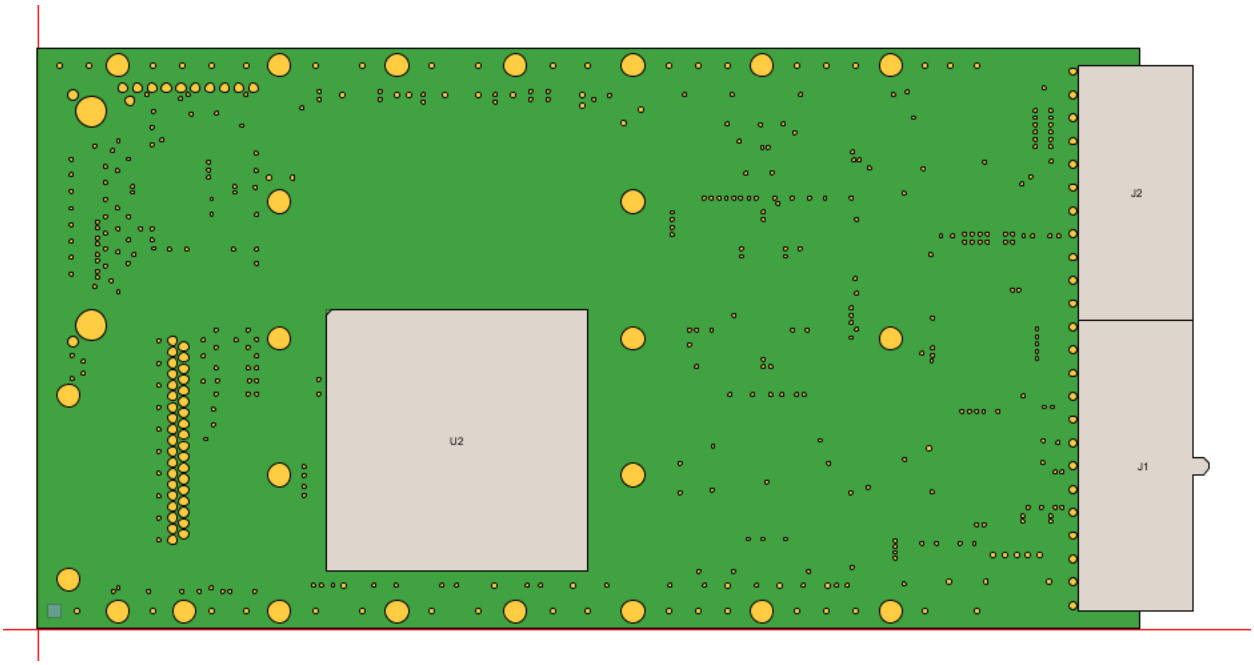



*Figure 4. PWA ODB++ import with components and holes.*

## Parts Definition

The components were imported from the supplied CAD file, including the two cPCI connectors (311P822-MC-110-AS-D and 311P822-MC-110-BS-D) and the two XILINX Virtex-5QV FPGAs (XQR5VFX130°C F1752). To note, the full assembly contained many other components, but the analysis was limited to the FPGAs and cPCI connectors which were being used in the SpaceCube project's preliminary testing. The part and attach properties were defined as shown below. The CALCE material "ceramicCC" was used for the FPGAs, with an amendment to the CTE value (5.5 ppm/C) to reflect the real part specification.

*Table 3. Part Materials and Parameters.*

| Combined Ma | Material ID: | Material Name: | X Elastic Modulus MPa | Y Elastic Modulus MPa | Z Elastic Modulus MPa | XY Poisson's Rat dimensionless | Density: kg/m^3 |
|---|---|---|---|---|---|---|---|
| component... | ceramicCAP | Ceramic Chip ... | 1.04E7 | 1.04E7 | 1.04E7 | 0.17 | 3000.0 |
| component... | ceramicRES | Ceramic Chip ... | 310000.0 | 310000.0 | 310000.0 | 0.3 | 3970.0 |
| component... | plastic | Plastic | 15900.0 | 15900.0 | 15900.0 | 0.25 | 1206.0 |
| component... | ceramicCC | Ceramic Chip ... | 351645.0 | 351645.0 | 351645.0 | 0.17 | 2601.0 |

| X Conductivity: W/mC | Y Conductivity: W/mC | Z Conductivity: W/mC | X Coefficient of Th ppm/C | Y Coefficient of Th ppm/C | Z Coefficient of Th ppm/C | Specific Heat: J/(kg-degK) | Maximum Usage degC |
|---|---|---|---|---|---|---|---|
| 4.2 | 4.2 | 4.2 | 9.2 | 9.2 | 9.2 | | |
| 15.0 | 15.0 | 15.0 | 7.1 | 7.1 | 7.1 | 765.0 | 150.0 |
| 0.67 | 0.67 | 0.67 | 15.0 | 15.0 | 15.0 | 1046.0 | 196.0 |
| 16.7 | 16.7 | 16.7 | 5.5 | 5.5 | 5.5 | | |

| Identifier | Part Description | Device Type | Package Type | Package Name | Part Library | Part Length mm | Part Width mm | Part Thickness mm | Package Material Referer |
|---|---|---|---|---|---|---|---|---|---|
| CGA484_1... | | microcircuit | generic | | | 29.17 | 29.17 | | component.ceramicCAP |
| CGA_FF17... | FPGA Xilinx XQR5FX130CF1... | microcircuit | generic | XQR5FX130... | microcircuit | 45.0 | 45.0 | 9.25 | component.ceramicCC |
| CON-2CP-... | 311P822-MC-110-BS-D | connector | generic | | | 49.9999 | 22.500082 | 11.0 | component.plastic |
| CON-2CP-... | 311P822-MC-110-BS-D | connector | generic | | | 43.999912 | 19.800064 | 10.75 | component.plastic |

| Part Weight grams | Max I/O | Part Outline Ty | Interconne mm | Intercor mm | Standoff H mm | Solder mm | Solder Bo Bond Area mm^2 | Max Temp. degC | Theta JC C/W | Thermal F | Vibration F | Mechanic | MC Fatigu | Interconne | Lead Mate |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 484.0 | Rectangle | | | | | | | | 0.0 | | | | column | |
| 50.0 | 1752.0 | Rectangle | 41.0 | 41.0 | 2.2 | 0.1 | 0.385 | 125.0 | 0.1 | 1.0 | 1.0 | 1.0 | 1.0 | column | |
| 15.3 | 123.0 | Rectangle | 12.0 | 42.0 | 0.1 | 0.1 | 2.75 | 125.0 | 0.1 | 1.0 | 1.0 | 1.0 | 1.0 | thruhole | via.Cu |
| 15.3 | 121.0 | Rectangle | 12.0 | 42.0 | 0.1 | 0.1 | 2.75 | 125.0 | 0.1 | 1.0 | 1.0 | 1.0 | 1.0 | thruhole | via.Cu |

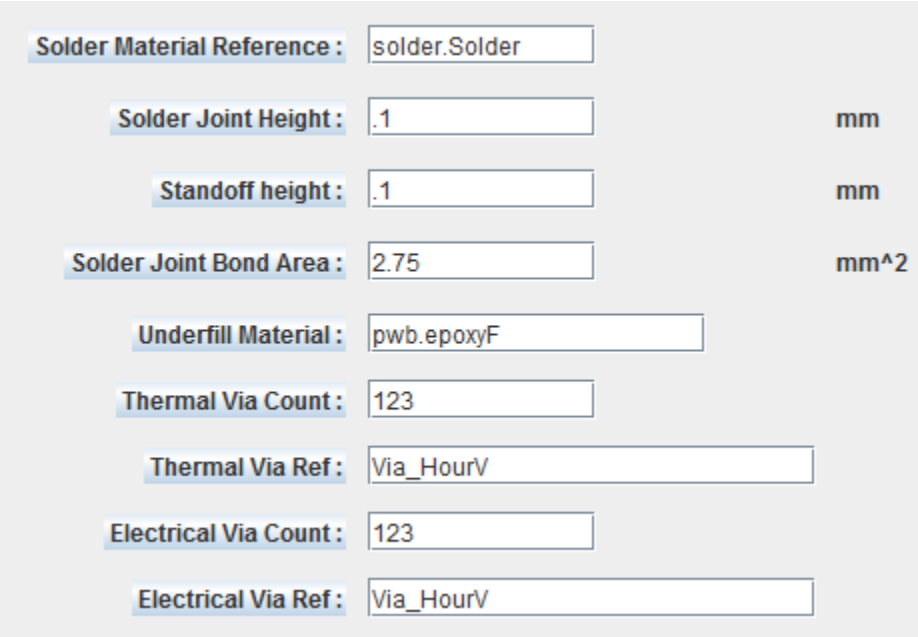



*Figure 5. cPCI Connector Attach Parameters (J1, J2).*

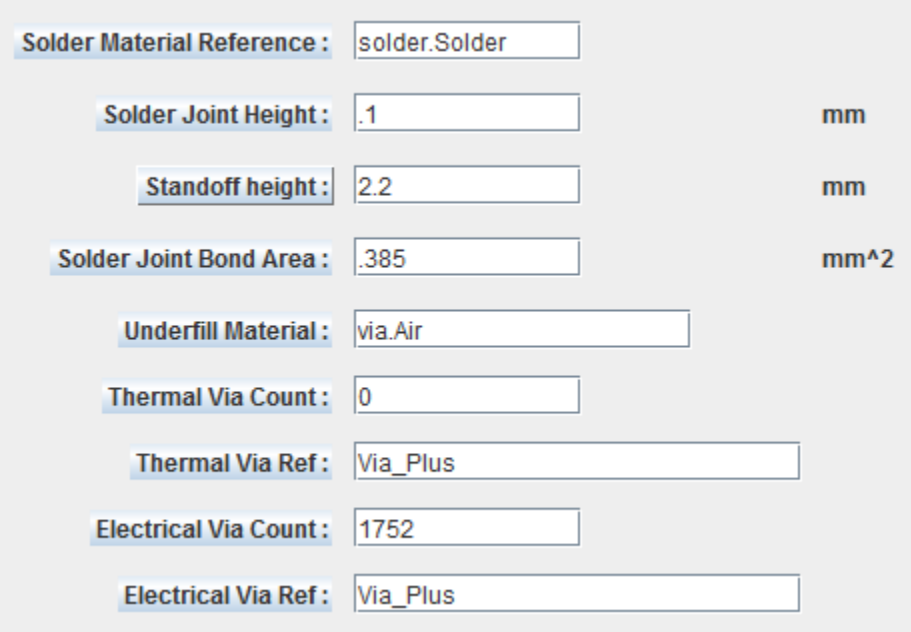



*Figure 6. FPGA Attach Parameters (U2, U3).*

# Thermal Analysis

The Thermal Analysis Manager tool was used to evaluate the powered board in a thermal vacuum (TVAC) testing environment as well as for on-orbit conditions. Seven individual finite element analyses were run to describe the high and low steady state temperatures at each high and low point of the thermal cycles for each of the 3 life cycle cases discussed in later sections. The results of these analyses were imported to that life profile and were used to estimate the useful life consumed by qualification/protoflight thermal vacuum testing as well as on-orbit conditions.

Two low earth orbit cases were analyzed to show the difference in estimated lifetimes: one with active thermal control (board heaters) that maintains the boards near 20°C at the cold conditions, and another without active thermal control that allowed the board temperature to drop with the boundary conditions/box temperature.

The third case simulated a thermal vacuum cycling life test that had been conducted by the Space Cube project to understand which failure modes the design could see using surface mount (CGA) components.

### 1.1.3 Component Power Levels

Power dissipation values provided by the design engineers estimate that the maximum power dissipated by the U2 and U3 CGA components is 5.922 watts each and is considered a worst case high value. The estimated power dissipated in J1 and J2 is very small based on the published resistance values, and for the analyses estimated to be very near zero. These values were input into the CALCE thermal analysis for this design and scenarios. Power dissipated in the components can be scaled down (by the user) from the maximum values provided in the CALCE SARA PWA thermal module once a more specific value is provided based on the application. This was not done as part of this task, so the maximum power dissipation values were used.

For the case involving the unpowered thermal vacuum chamber testing, the power dissipation in the components is zero.

## Thermal Parameters

Setting up the thermal analysis cases in CALCE SARA PWA involved loading the board ODB++ model with its material properties, defining environmental conditions and other interactions such as the thermal boundary conditions related to the aluminum housing, ambient temperatures, heat transfer mechanisms, and board and housing emissivities.

### 1.1.4 Boundary Conditions

The boundary conditions for the thermal analysis are shown below, and are consistent throughout each of the thermal analysis cases described below, varying the ambient and aluminum housing steady state temperatures.

A representative example is shown below in Figure 7. This particular case is for the thermal vacuum low qualification temperature case. The light green bars indicate the boundary conditions on the board and are coincidental with the PWA to aluminum housing contact points. The boundary condition shown in black is indicative of an insulated area around J1 and J2 connectors. This is assumed to be insulated for three reasons: 1) the top and bottom areas do not make contact with the housing, and in a vacuum there is minimal heat transfer to the walls of the outer housing out the edges, 2) the connectors J1 and J2 are made of plastic with the exception of the pins, and do not make significant contact with their surroundings, and 3) coupled with the assumption that J1 and J2 dissipate nearly zero power, the assumption that the area acts as if it were insulated is conservative.

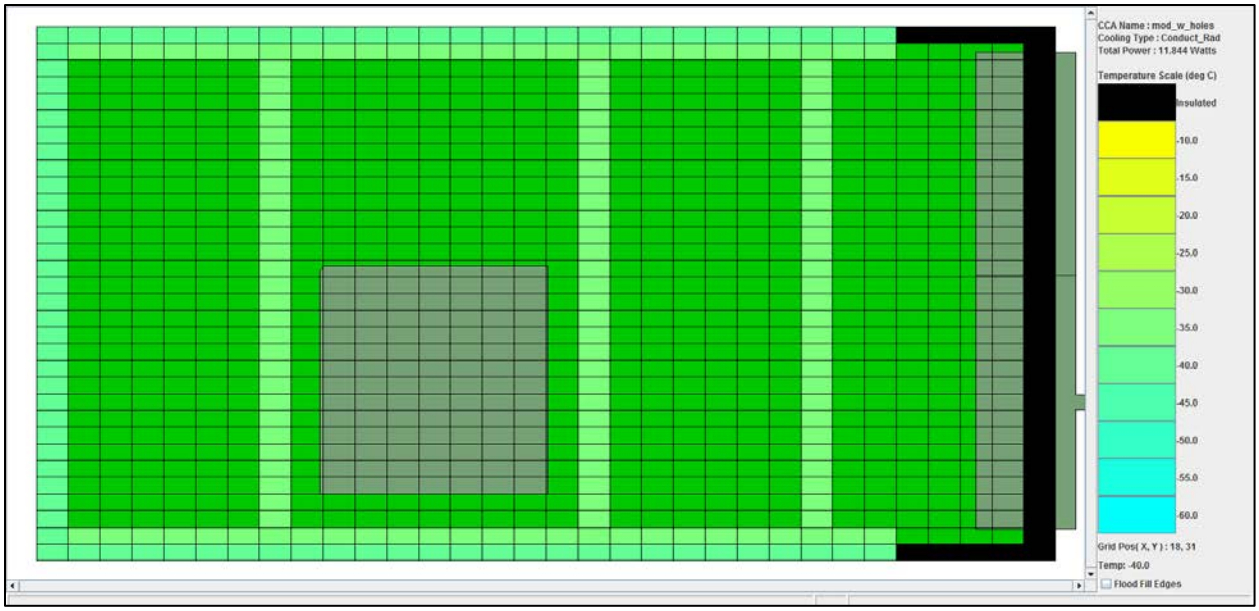



*Figure 7. Example case showing the boundary conditions of the PWB under study.*

### 1.1.5 Heat Transfer Mechanisms

In a thermal vacuum chamber and on-orbit, there are no gases to interact with and carry away the heat being generated in the board via convection, so conduction and radiation were the mechanisms selected in the CALCE thermal module for this series of analyses. The thermal conductivity values of the materials were are defined in the CALCE SARA PWA material database. For the thermal radiation mechanism, the board and aluminum housing emissivities were required to be specified in the thermal analysis module and were selected as follows.

| Material | Emissivity |
|---|---|
| Anodized Aluminum | 0.77 (Incropera & DeWitt) |
| PWB Solder Mask | 0.9 (Incropera & De Witt) |

A screen shot of the other parameters required is shown below. Note the only changes will be to the ambient temperature for each case. The ambient temperature is assumed to be temperature inside the PWA housing assuming it is installed into its box:

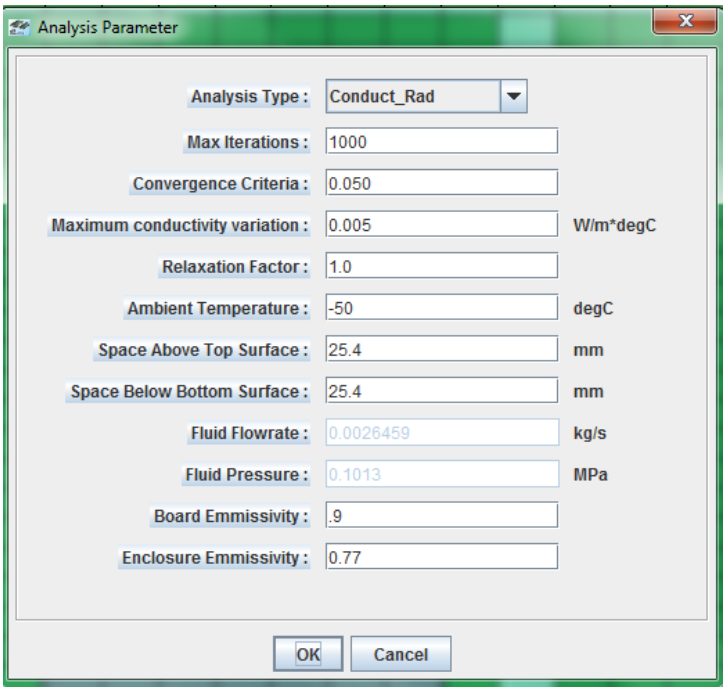



*Figure 8. Representative thermal analysis parameter inputs for the CALCE SARA PWA thermal analysis. The ambient temperature value will change for each thermal case.*

*Table 4. Boundary Conditions for Each Thermal Analysis Case.*

| Thermal Analysis Case | Boundary Temperatures | Ambient Temperature |
|---|---|---|
| Thermal Vac Qualification/Protoflight Levels High | 65°C on perimeter<br>70°C on crossbars | 65°C |
| Thermal Vac Qualification/Protoflight Level Low | -40°C on perimeter<br>-35°C on crossbars | -40°C |
| On-orbit High Temperature | 50°C on perimeter<br>55°C on crossbars | 50°C |
| On-orbit Low Temperature Without Thermal Control | -30°C on perimeter<br>-25°C on crossbars | -30°C |
| On-orbit Low Temperature With Thermal Control to Maintain PWB around 20°C | 15°C on perimeter<br>20°C on crossbars | 15°C |

## Thermal Analysis Results

A steady state solution for each thermal plateau condition in Table 4 was found using the above thermal cases using the CALCE SARA PWA thermal analysis module. Each of the figures below shows the resulting temperatures. The results of each case are used as inputs to the life cycle definition which defines the various thermal loads the PWA will see for each of the life cases.

In each of the cases, the resulting component, junction, and board temperatures do not exceed the maximum temperature limits given in manufacturer specifications (Xilinx, 2012) or NASA EEE-INST-002

(NASA NEPP, 2008). At the worst case condition (protoflight high ambient temperatures, powered, max power), the max junction temperatures of U2 and U3 are more than 40°C less than the manufacturer's maximum of 125°C .

The results for the 5 thermal plateaus in Table 4 are given in the following sections; the results for the unpowered thermal vacuum testing are not shown, but incorporated into the life analyses in the applicable sections.

### 1.1.6 Thermal Vacuum Qualification/Protoflight High Temperature

The boundary conditions for the protoflight high temperature case were selected to be the same as the thermal analysis to determine if the resulting board and component temperatures were reasonably similar to the detailed thermal finite element analysis shown in Figure 11. Overall, the CALCE SARA PWA results indicate component and board temperatures that are 7-10 C lower than the thermal analysis shown in Figure 11. Possible reasons for this are:

- The board being analyzed in CALCE is not a fully populated processor board, and is not dissipating as much power as the fully populated board (shown in the analysis results in Figure 11), which would be consistent with generally higher temperatures.
- Boundary conditions around the perimeter of the board were all set to the same value (65°C) in the CALCE model. This would be consistent with the way it is indicated in the drawing (carrier with board installed), and also consistent with a standalone configuration in a thermal vacuum test. In contrast, the analysis in Figure 11 uses a box base temperature of 65°C as the equivalent boundary condition and runs the analysis with the card and carrier installed in the box.
- The possibility that the thermal analysis run in Figure 11 assumes the presence of an adjacent powered PWB installed in the processor box with both a higher emissivity value as well as radiating additional heat (due to power dissipation) between cards. The CALCE SARA PWA version of this model assumes an anodized aluminum surface at ambient temperature adjacent to the processor board with an emissivity that is roughly 14% lower than that of a solder mask coating.

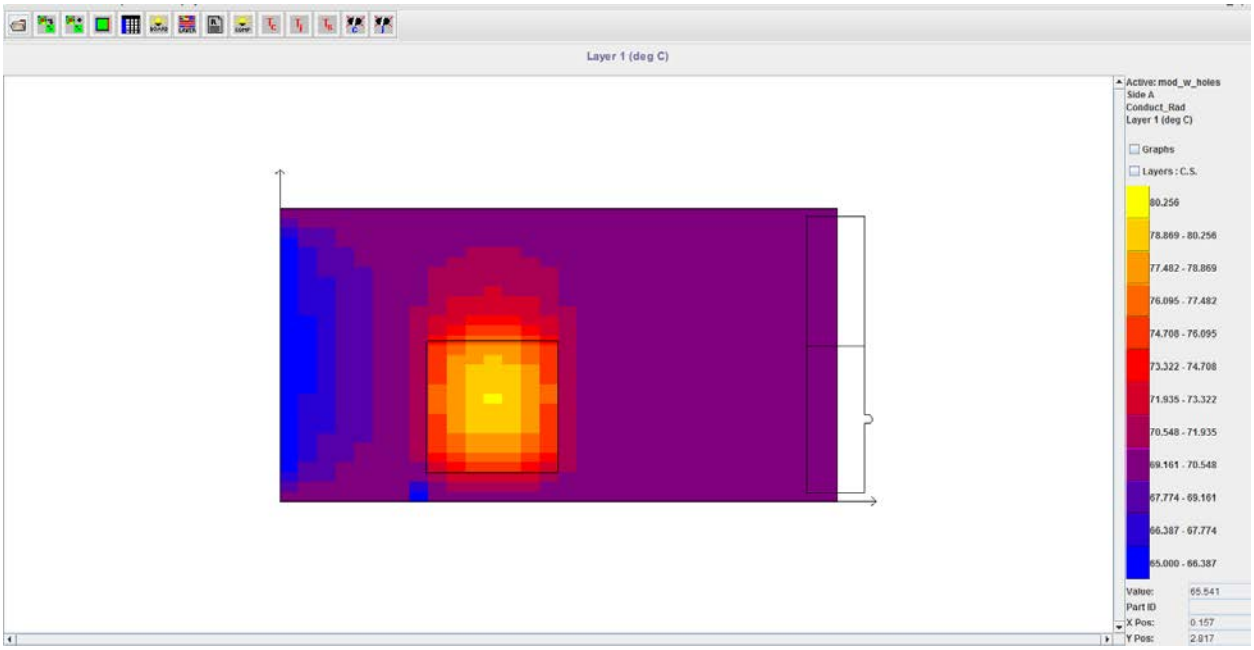



*Figure 9 - Steady state PWB temperature map for the high temperature protoflight case (ambient temperature 65°C ).*

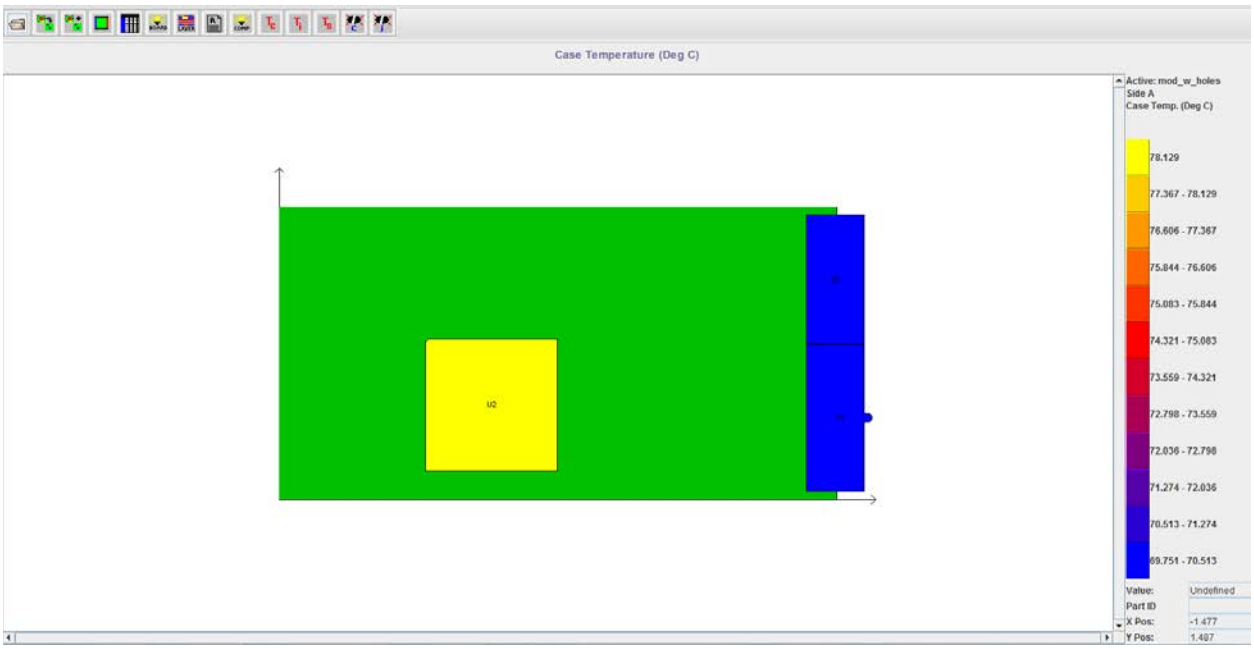



*Figure 10. Steady state component case temperatures for the high temperature protoflight case (ambient temperature 65°C ).*

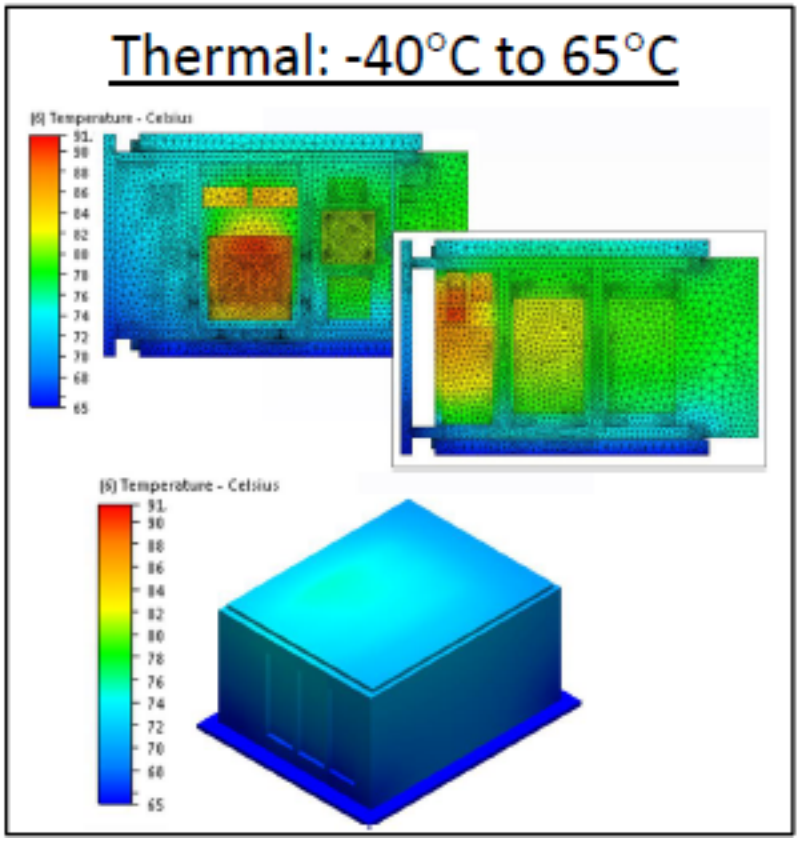



*Figure 11. Thermal analysis of similar (more components) Spacecube 2 PWA design shown for reference (box base temperature 65°C ) (Petrick, 2014).*

### 1.1.7 Thermal Vacuum Qualification/Protoflight Low Temperature

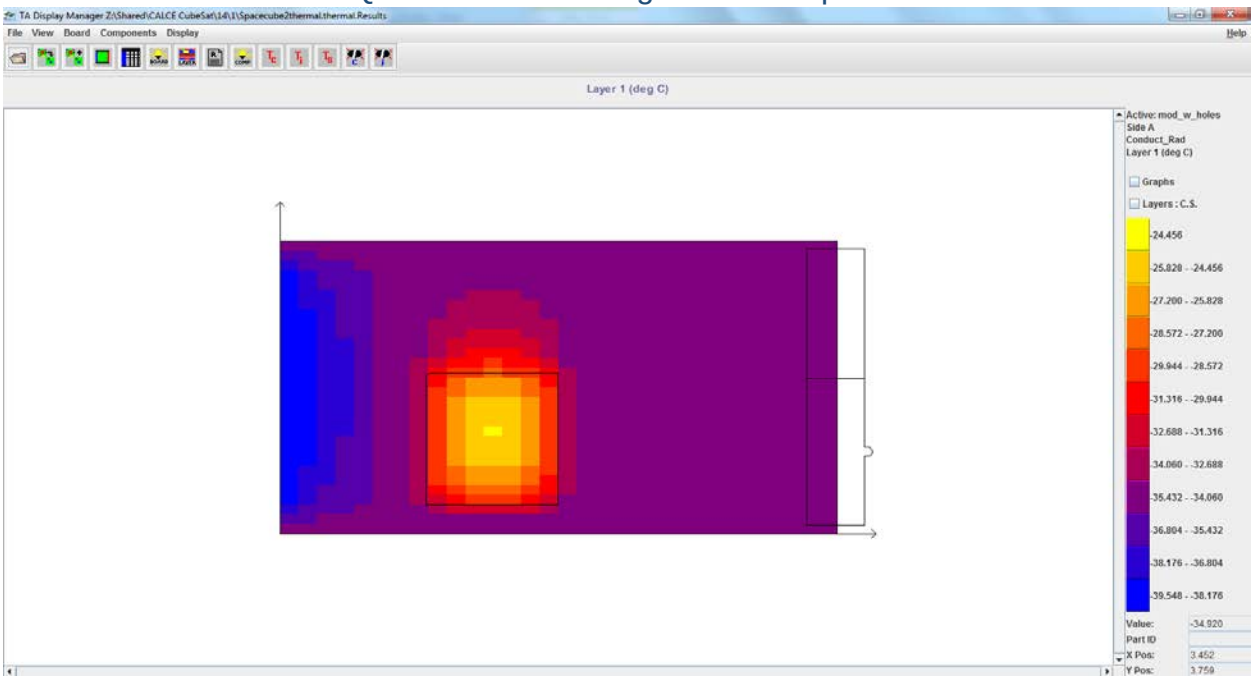



*Figure 12. Steady state temperatures for the low temperature protoflight case.*

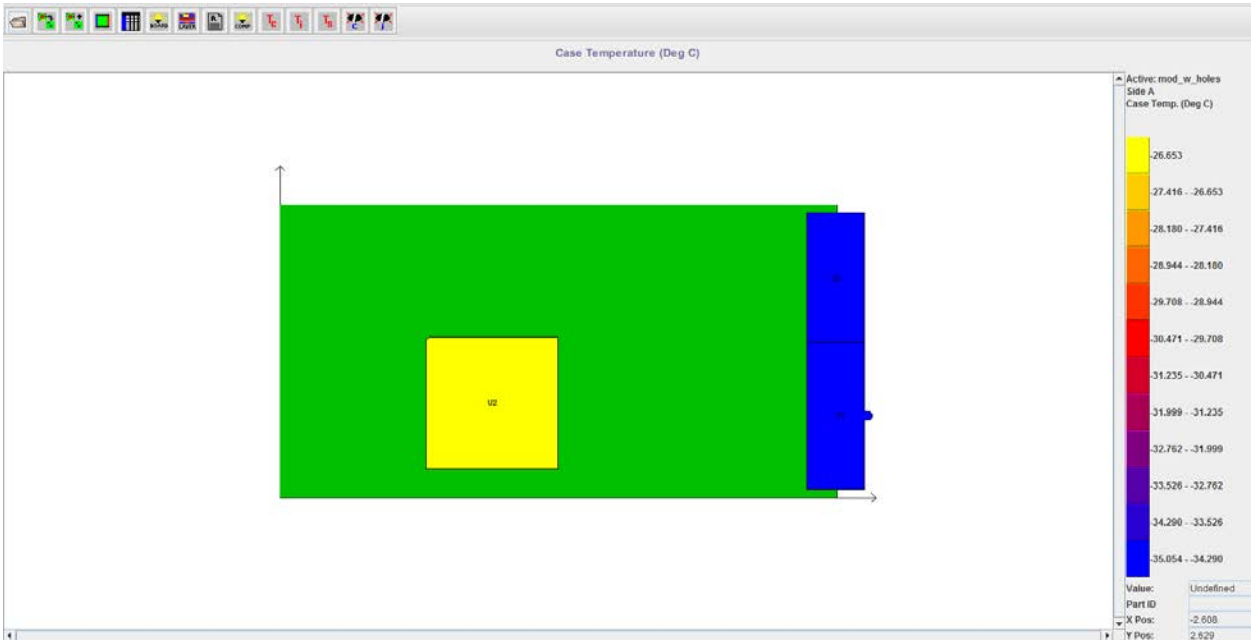



*Figure 13. Steady state component case temperatures for the low temperature protoflight case.*

### 1.1.8 On-orbit High Temperature

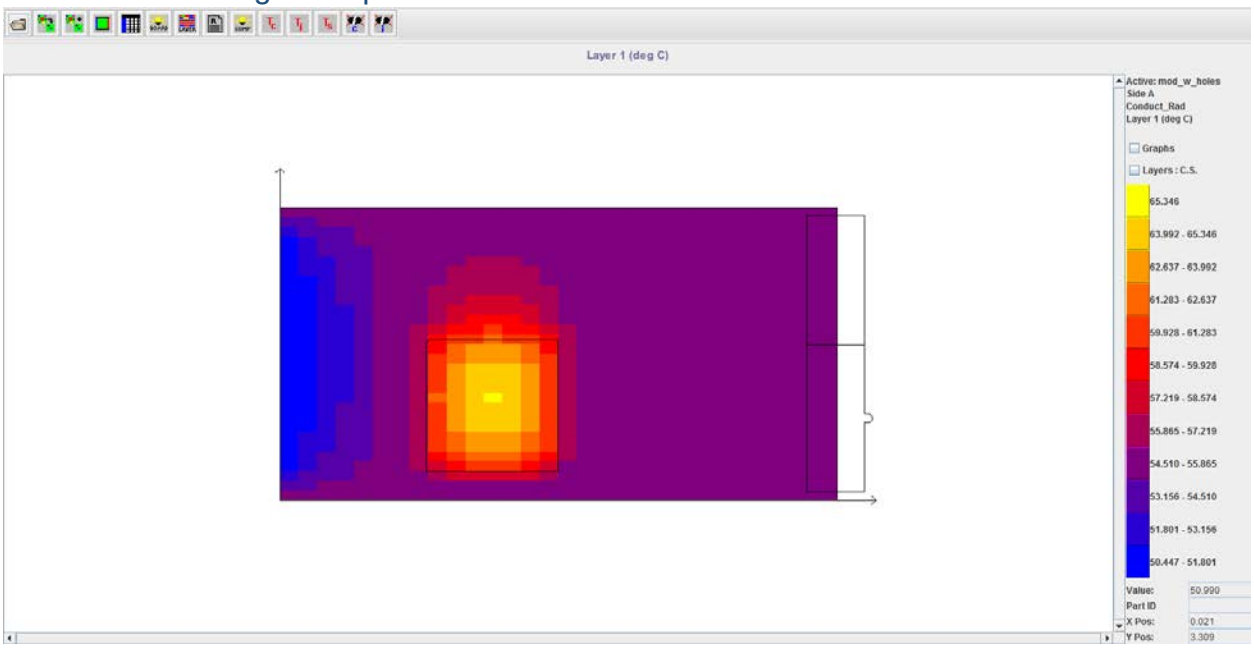



*Figure 14. Steady state PWB temperatures for the on-orbit high temperature case (box temperature 50°C ).*

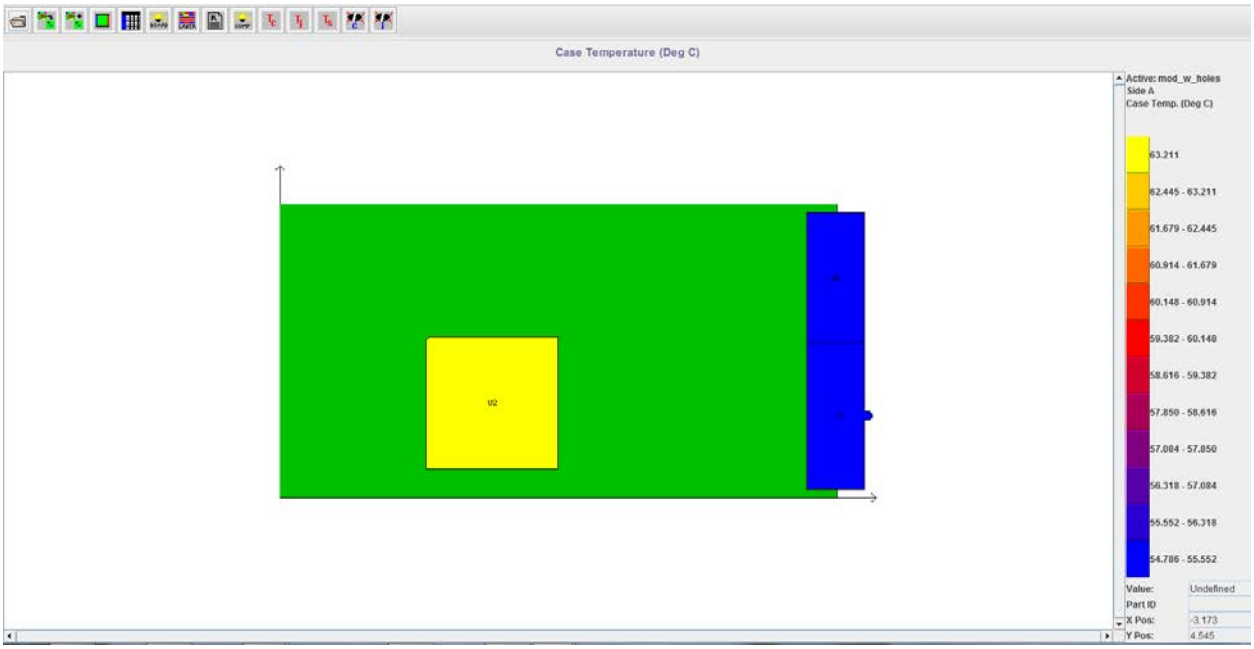



*Figure 15. Steady state component case temperatures for the on-orbit high temperature case (box temperature 50°C ).*

### 1.1.9 On-orbit Low Temperature without Thermal Control

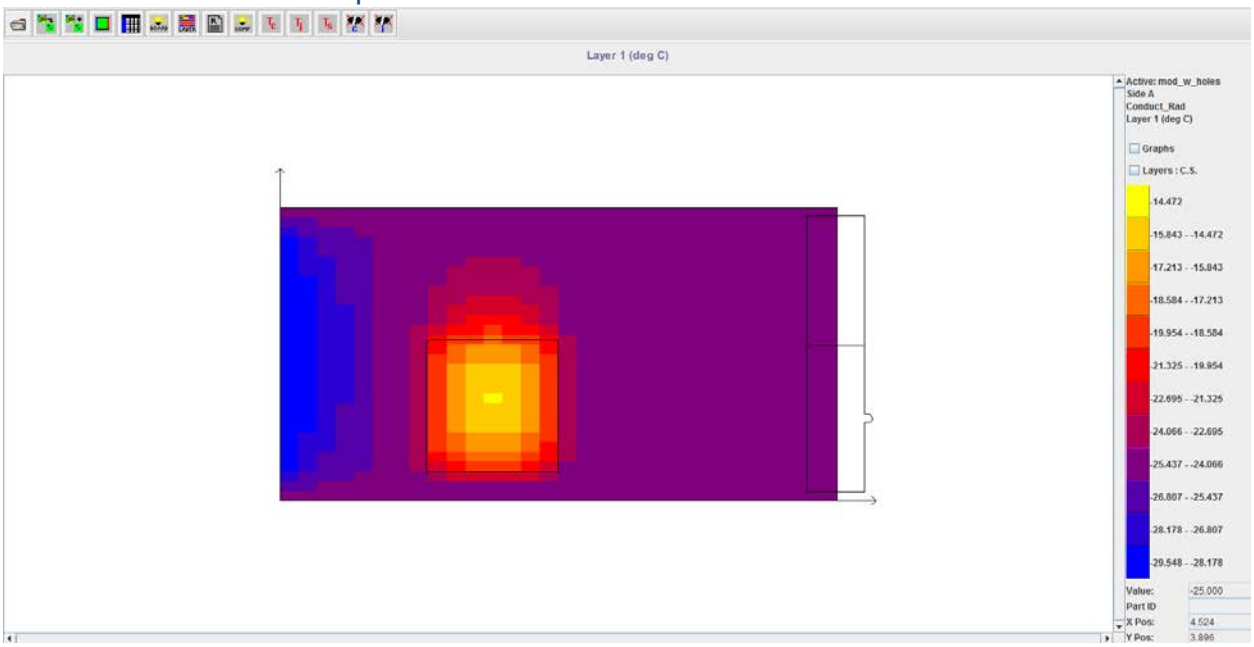



*Figure 16. Steady state PWB temperatures for the on-orbit low temperature case (box temperature -30°C).*

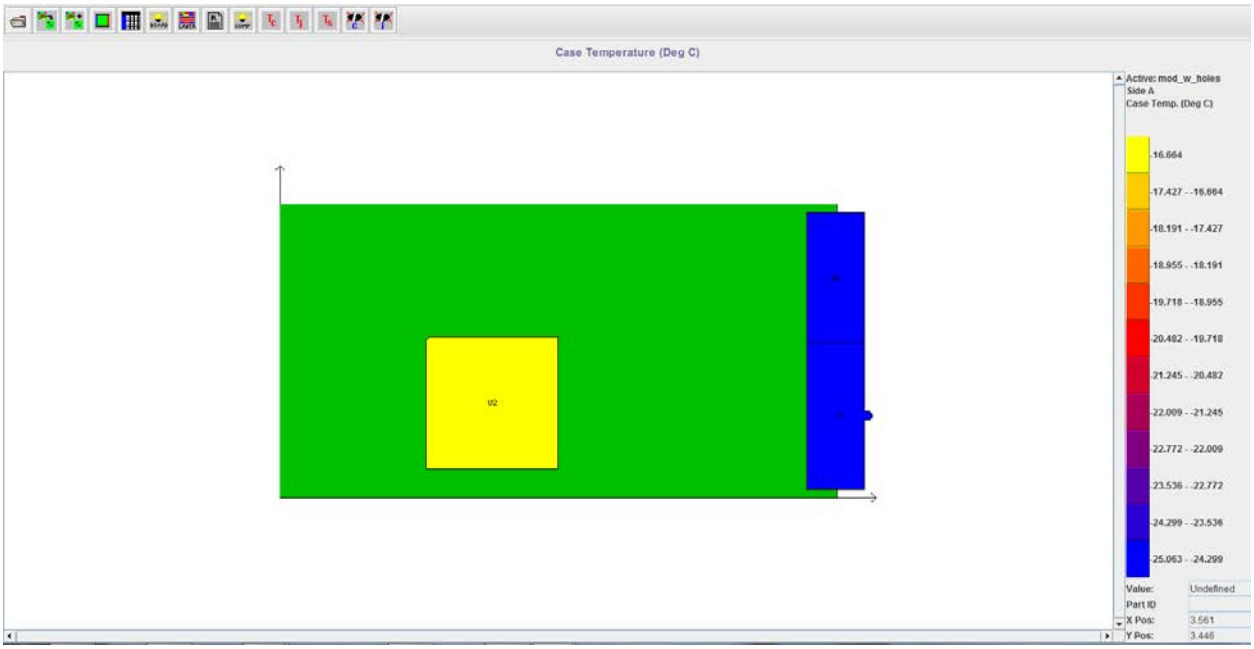



*Figure 17. Steady state component case temperatures for the on-orbit low case (box temperature -30°C).*

### 1.1.10 On-orbit with Thermal Control (Board Temp Maintained at 20°C)

To reflect typical designs, a case was constructed to include the presence of thermostatically controlled heaters with a set point of 20°C. To keep the analysis reasonably straightforward, heaters were not added to the model. Instead, thermal boundary conditions were selected at a value that would render a steady state PWB temperature response at or near 20°C. It is recognized that the heaters can be added to the model as standalone components, and could potentially alter some of the results due to local heating effects. Those effects were not considered in this study due to the small number of parts

populated in the model.  This is considered forward work for a more densely populated version of this PWA.

In order to “force” the board temperature close to 20°C, the boundary conditions (box temperature) were set to 15°C based on the previous results that indicate the board temperature steady state temperature is roughly 5°C higher than the boundary conditions.

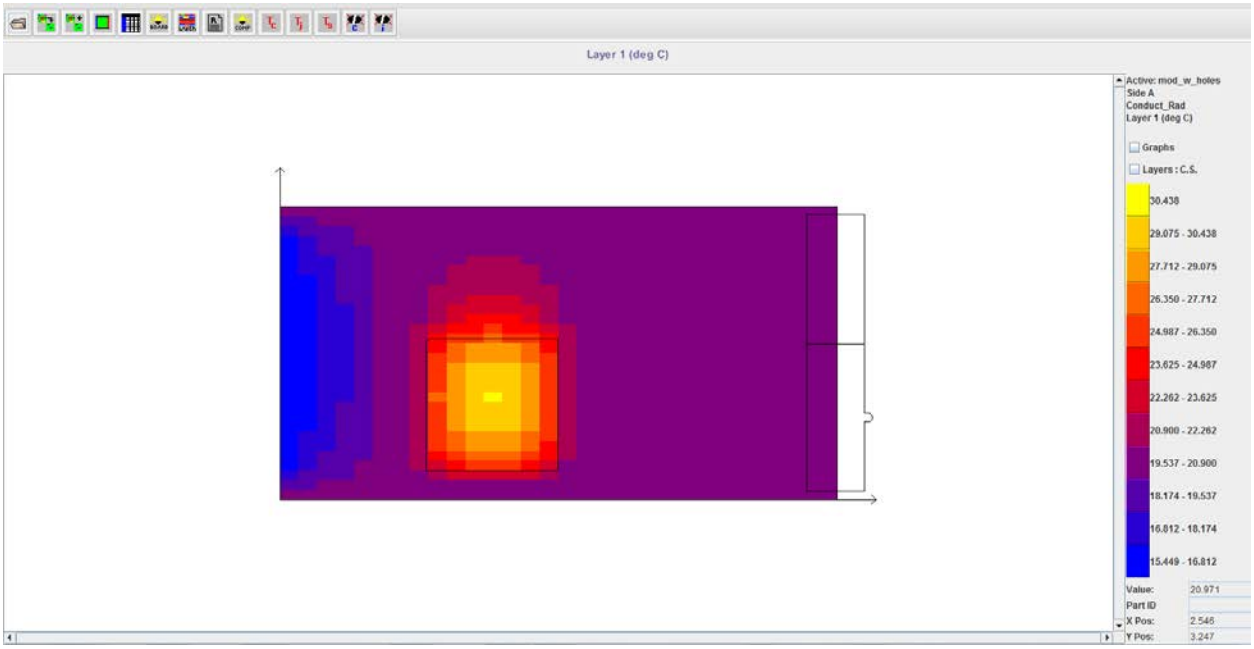



*Figure 18.  Steady state PWB temperatures for the on-orbit low temperature case with board heaters set to 20°C (box temperature 15°C ).*

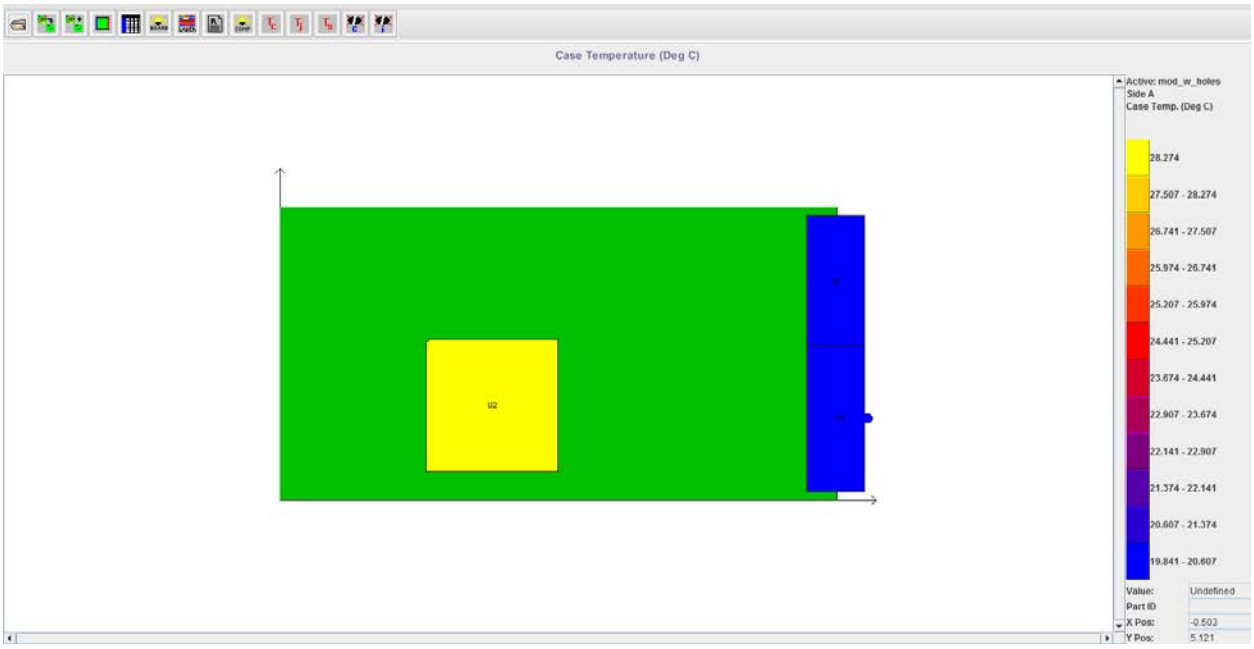



*Figure 19.  Steady state component case temperatures for the on-orbit cold case with board heaters set to 20°C  (box temperature 15°C ).*

The results of each of these analyses were imported into, and used as the inputs to the appropriate life cycle profile which will be discussed in later sections.

# Vibration Analysis

## Vibration Boundary Conditions

The processor card is mounted in a fixture with card guides (not shown). The PWA is clamped (sandwiched) between two aluminum holding fixtures with screws that extend through the thickness of both supports via holes through the board to maintain its location in the assembly.

These were replicated in the model by affixing clamped supports on both sides, restricting the board's out-of-plane motion along those bars (shown as the red bars in Figure 20).

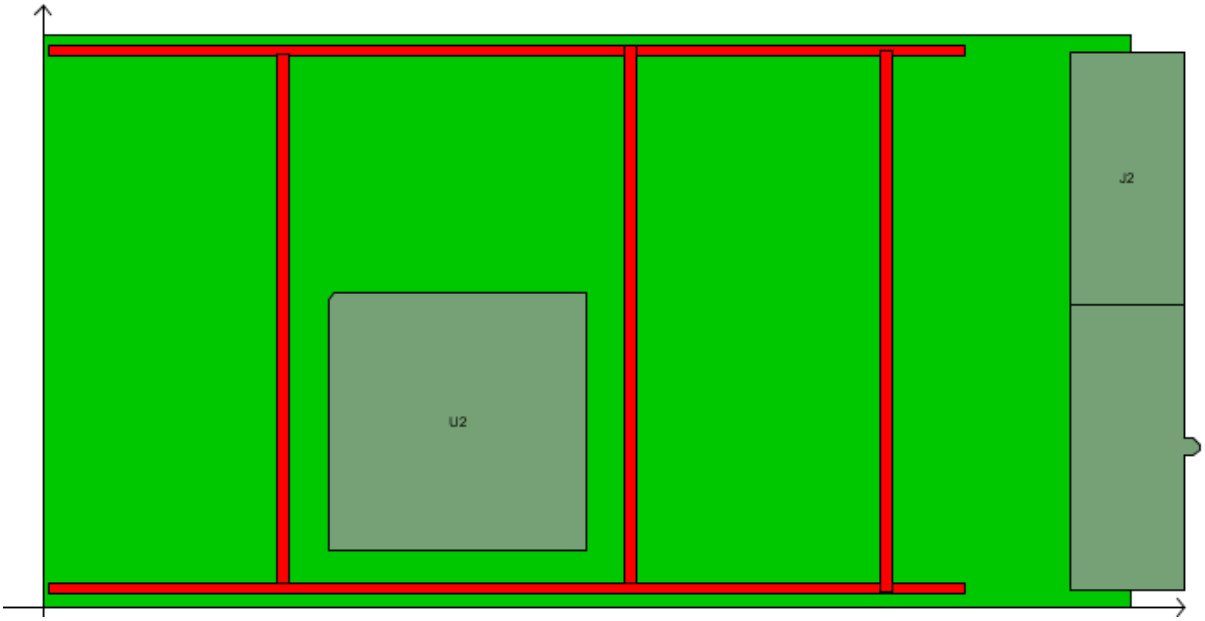



*Figure 20. Mounting Fixture in CALCE SARA.*

Once the model was imported and the boundary conditions were set, the load profile was input into the CALCE SARA PWA vibration tool. For this PWA design, two different load conditions were input and two different responses were needed: one to simulate the loads and response from protoflight qualification random vibration and one for acceptance/launch loads.

There is a connector plate on the left side of the assembly (not shown), but was omitted and assumed that it did not affect the clamping of the board to the structure since it is bolted to the ends of the supports and is only connected to the processor card via a test connector (not modeled in this analysis). It could possibly act to constrain the board in the Z axis at that point, and upon observation would tend to raise the frequency and lower the amplitude of the response at that end of the board if considered as additional

boundary conditions. Omitting those features simplifies the analysis, and is conservative given that this location is excited by the 3rd mode of the response.

## Random Vibration Inputs for Qualification and Acceptance Levels

The loading conditions for qualification and acceptance levels were specified as per GSFC-STD-7000A, General Environmental Verification Standard (GEVS) for GSFC Flight Programs and Projects, Section 2.4.2 (NASA Goddard Space Flight Center, Greenbelt, MD, 2013). They are both random vibration load profiles, but the protoflight power spectral density is higher than the acceptance/launch load levels.

These were done to simulate the loads and responses for those encountered during integration & testing (I&T) as well as during launch. Qualification levels were assumed since it is unknown at this time whether the design will be flown as a protoflight version, or if it will be built based on a qualified design and tested to acceptance levels. The qualification/protoflight loads are a conservative approach to this and will be representative of testing in I&T. For this analysis, the acceptance loads will be representative of the actual launch random vibration loads rather than a redundant acceptance test during I&T.

Similar to the thermal analysis results, the results of the random vibration loading will later be used as inputs to the life profile described in later sections of this report.

The duration of the random vibration specified in GEVS is 2 minutes in each of the 3 axes, however it should be pointed out that CALCE SARA PWA only performs the analysis in the Z axis (perpendicular to the plane of the page), and that the Z axis responses and stresses are the only one simulated for this design.

### 1.1.11 Qualification Level Random Vibration Inputs

The random qualification/protoflight level power spectral density used as load inputs are shown in Table 5 and Figure 21.

*Table 5. Random vibration loading profile for protoflight/qualification of components under 50lb per GEVS.*

| POINT | FREQ. (Hz) | PSD (G^2/Hz) |
|---|---|---|
| 1 | 20.0 | 0.026 |
| 2 | 50.0 | 0.16 |
| 3 | 800.0 | 0.16 |
| 4 | 2000.0 | 0.026 |

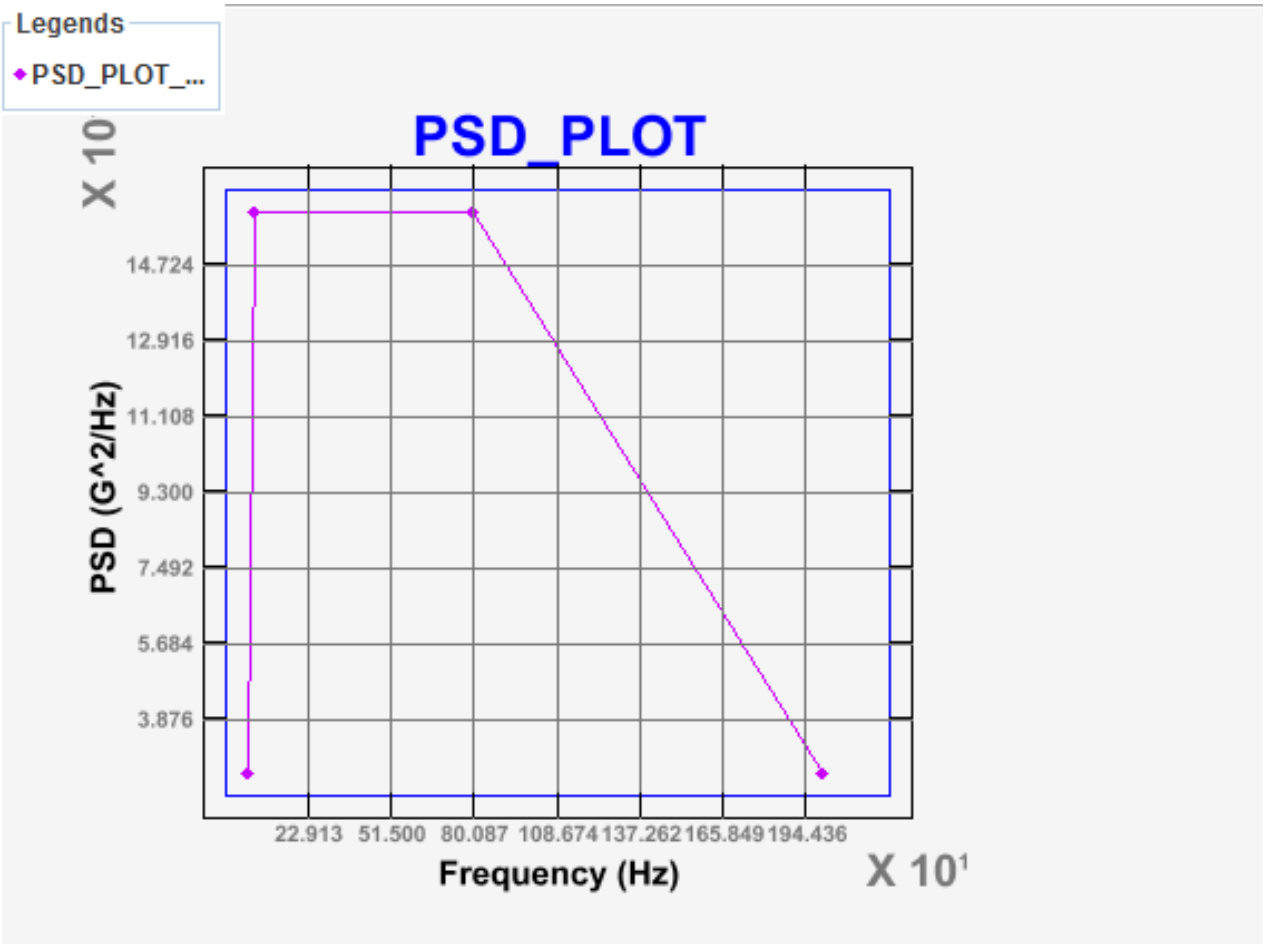



*Figure 21. Power spectral density input plot of protoflight/qualification random vibration.*

### 1.1.12 Acceptance Level Random Vibration Inputs

As with the qualification level inputs above, the range of frequencies is the same, but the PSD inputs are lower in magnitude as shown in Table 6 and Figure 22.

*Table 6. Random vibration loading as specified in GEVS for acceptance levels and random vibration at launch.*

| POINT | FREQ. (Hz) | PSD (G^2/Hz) |
|---|---|---|
| 1 | 20.0 | 0.013 |
| 2 | 50.0 | 0.08 |
| 3 | 800.0 | 0.08 |
| 4 | 2000.0 | 0.013 |

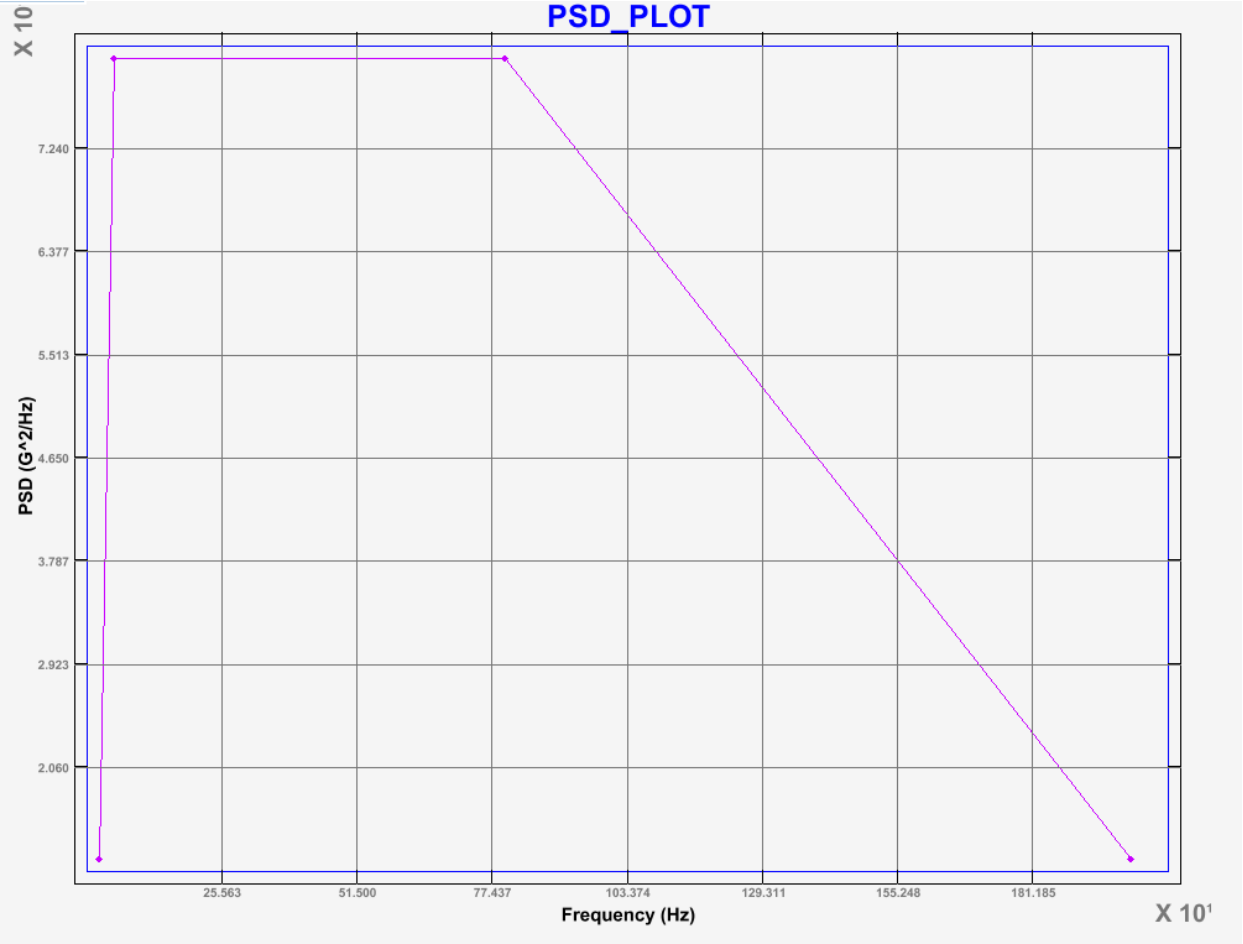



*Figure 22. PSD input plot for acceptance loads.*

## Vibration Analysis Results

With the design imported, the boundary conditions set, and the loading specified, the simulations were run for each case. CALCE SARA PWA provides a number of display options for the board response for parameters of interest (first through fifth modes, displacement, relative curvature, animations, etc.), but not all will be shown in this report. For this board, only the first three modes were selected for each PSD case.

### 1.1.13 Protoflight/Qualification Response

For the qualification level random vibration response, the summary of the steps performed in the CALCE software is shown in Figure 23 and Figure 24.

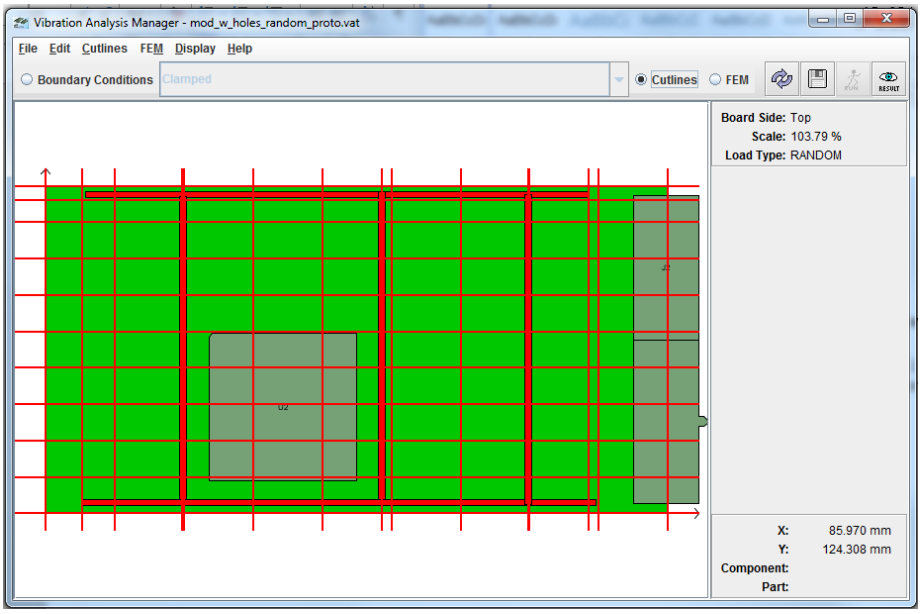



*Figure 23. Diagram of the PWB showing the selected cutlines for the finite element mesh.*

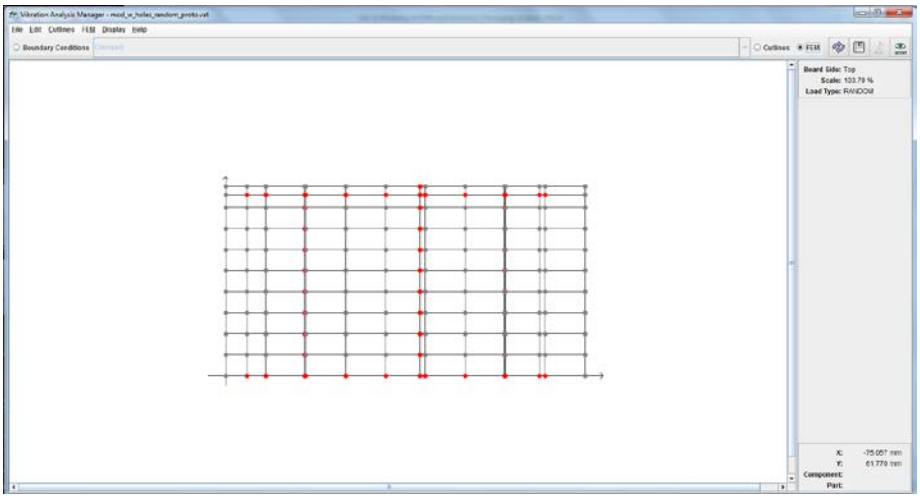


*Figure 24. The cut lines converted to the FEM view that pulls in the stiffness matrix values of the PWA model.*

Results from the qualification level simulation are shown below; the first three response modes are shown on the top right of Figure 25. The first two modes (1104 Hz, and 2039 Hz, respectively) show responses at the location of the J1 and J2 connectors. The higher response at that location is due to a combination of the added mass of the connectors and the absence of a local clamped boundary condition to shorten the free length of that section of board. The third mode response (2118 Hz) is seen at the end opposite of J1 and J2, and is again associated with the absence of a local clamped constraint.

The CALCE software did not indicate any critical areas due to the response to the inputs with respect to displacements or excessive board curvature. The sections of the board containing the U2 and U3 components do not indicate sensitivity to the input PSD.

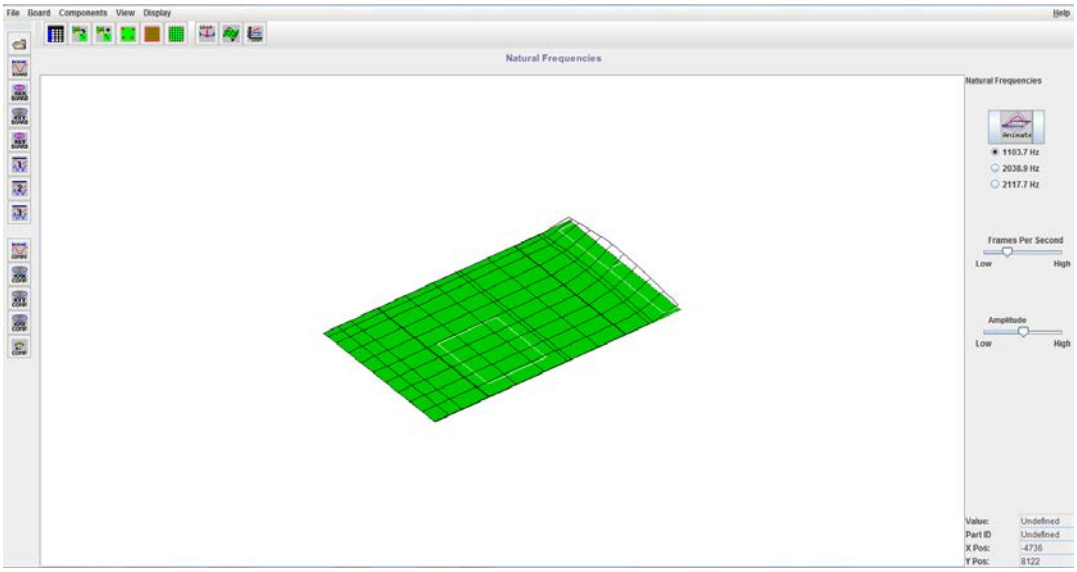



*Figure 25. 1st mode board response from GEVS qualification level random vibration.*

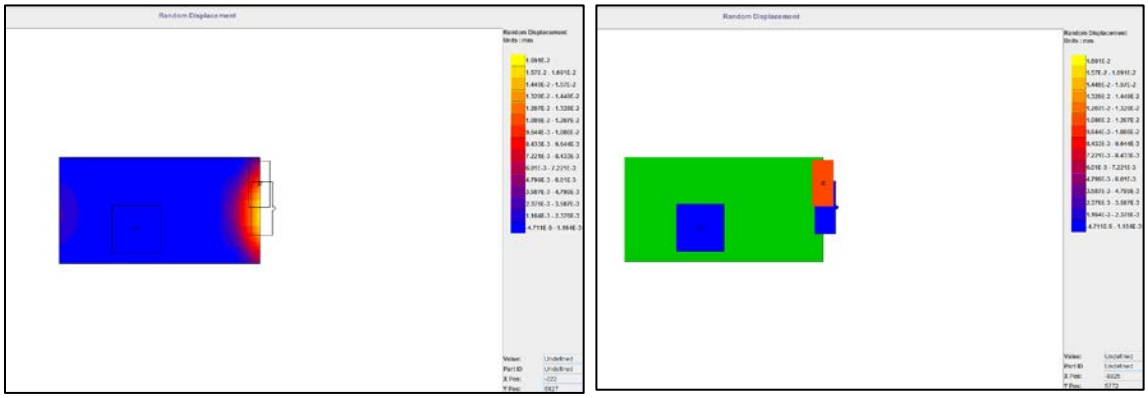


*Figure 26. Board (left) and component (right) random vibration displacement response, qualification/protoflight levels in mm (all frequency responses).*

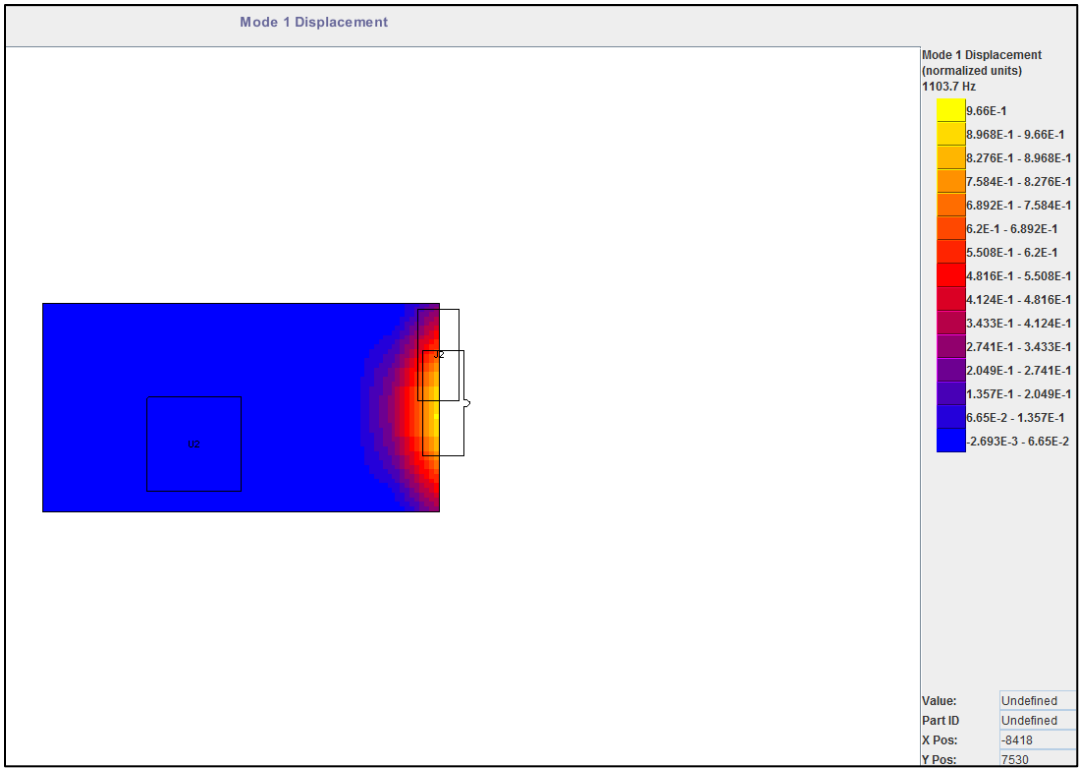



*Figure 27. First mode normalized displacements, qualification/protoflight vibration levels..*

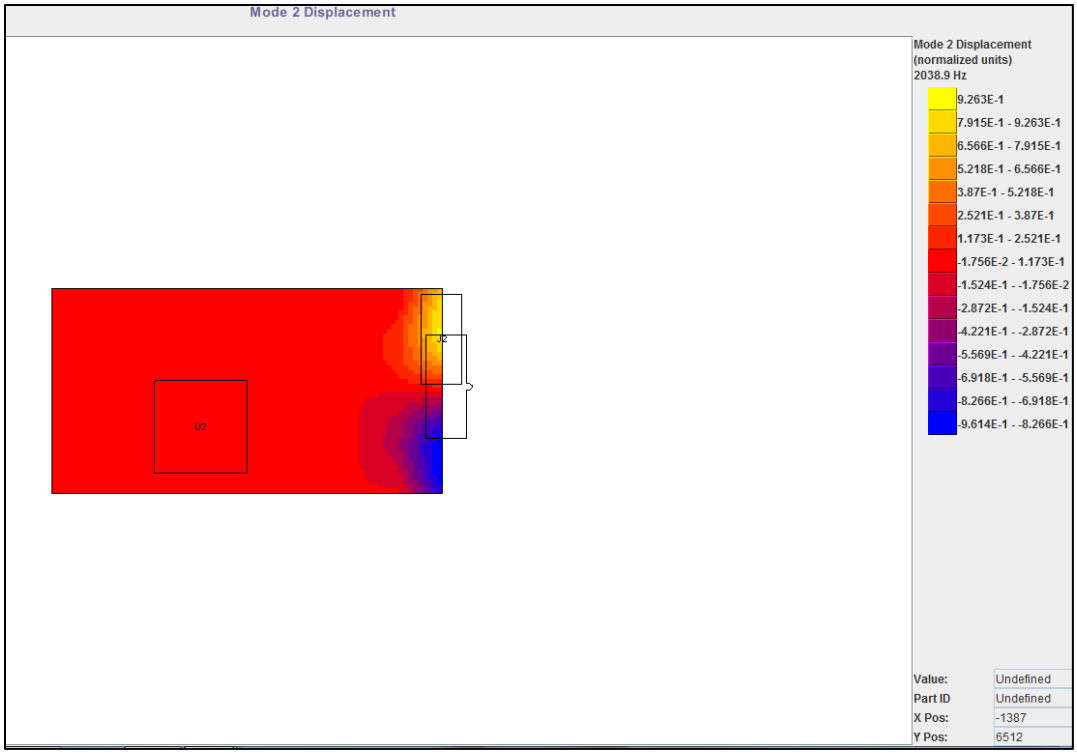



*Figure 28. Second mode response, qualification/protoflight vibration levels.*

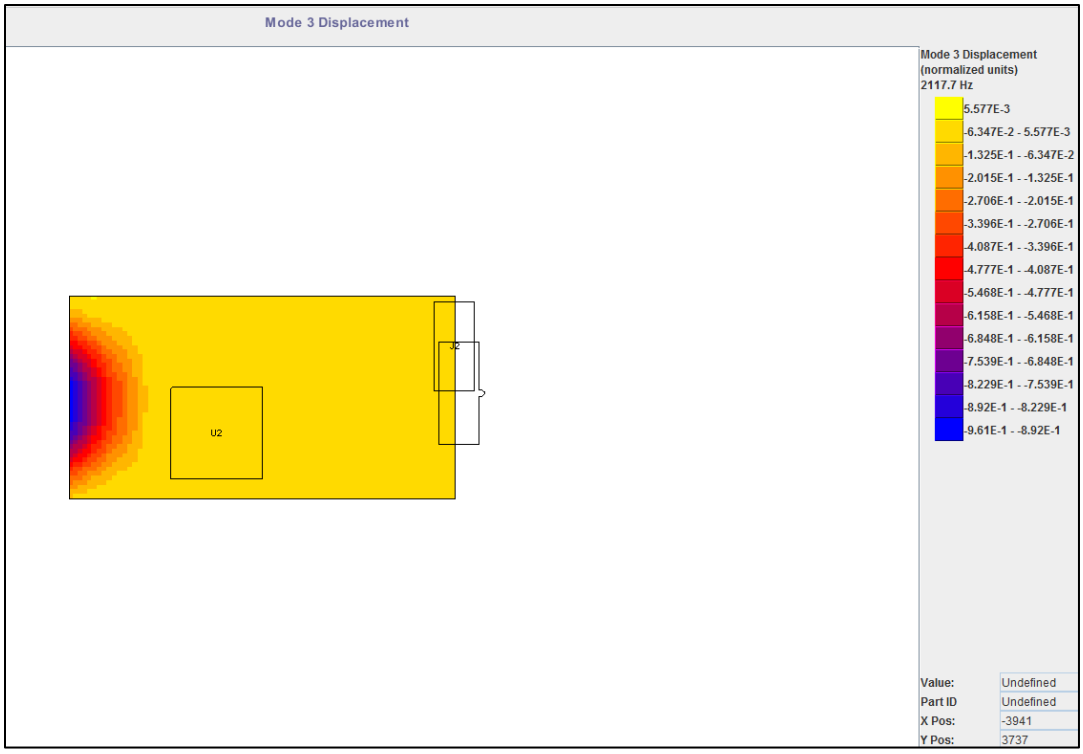



*Figure 29. Third mode response, qualification/protoflight levels.*

### 1.1.14 Acceptance/Launch Random Vibration Levels

As expected, the resulting response with the random vibration PSD at acceptance levels show the first three modes occurring at the same frequencies as the qualification/protoflight random vibration levels.

Board displacement response given the GEVS acceptance level PSD input is roughly 30% less than with the GEVS qualification/protoflight PSD.

Overall response is visually shown in Figure 30 and Figure 31.

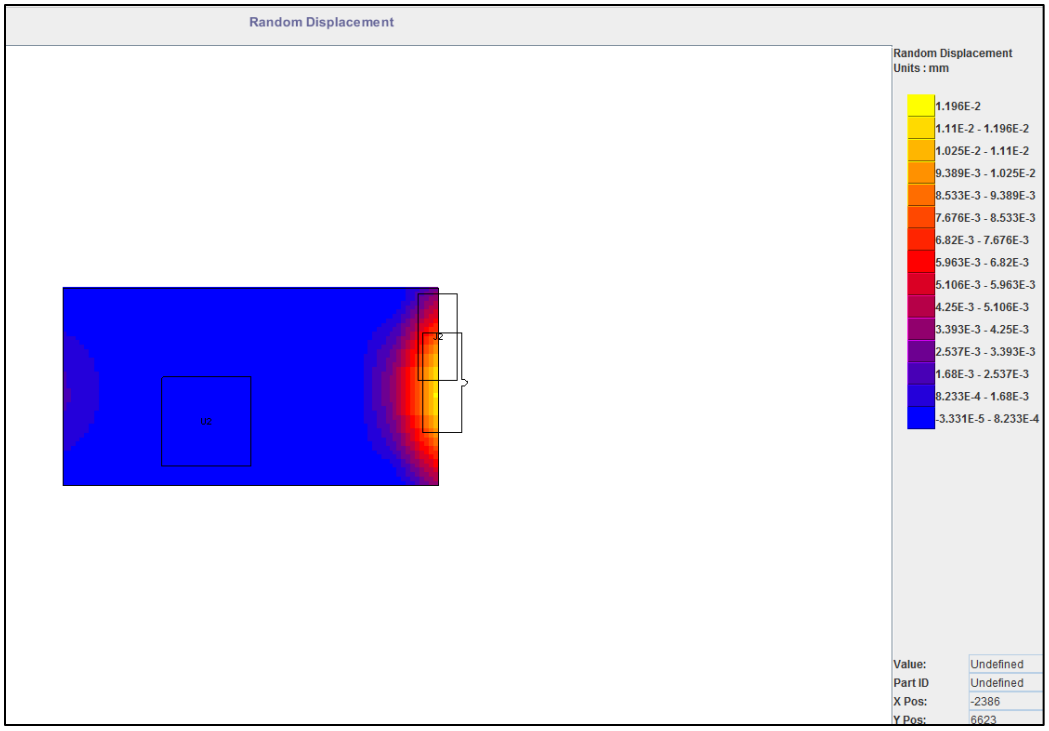



*Figure 30. Board displacement response at GEVS acceptance level PSD input.*

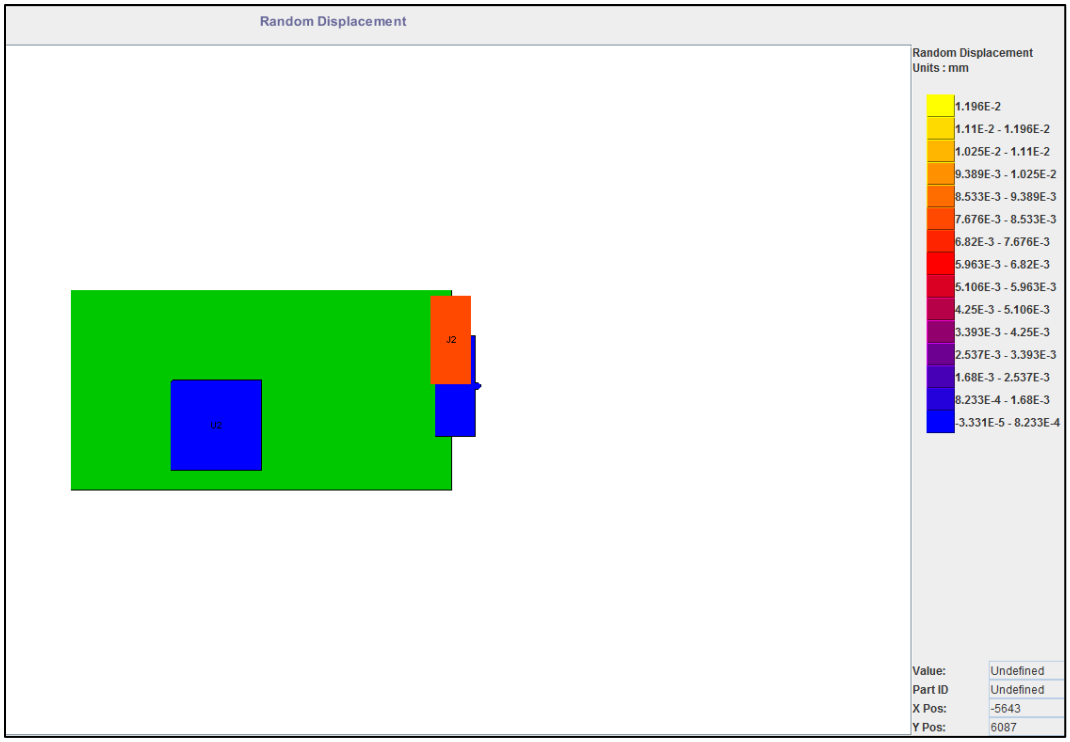



*Figure 31. Component displacement response given the GEVS acceptance level PSD input.*

# Failure Analysis

## Life Cycle Profile Parameters

CALCE provides tools to build life cycle profile models that describe the loads a PWA will see over the course of its lifetime, and estimates the cumulative life lost due to the induced stresses and strains for each of the phases comprising the life cycle. For the two low earth orbit cases discussed below, the life cycle consists of four phases: two that are reflective of Integration and test conditions described in GSFC-STD-7000A:

- Component protoflight random vibration (<50lb) –stresses imposed from protoflight random PSD input
- Component protoflight level thermal vacuum testing—stresses imposed from a qualification level thermal profile per GSFC-STD-7000A

The remaining two life cycle phases consist of the ascent loads and thermal cycling loads in low earth orbit:

- Random vibration loads from an expendable launch vehicle (ELV) which were modeled as the acceptance level PSD input loads for 2 minutes.
- Low earth orbit cold and hot cycles occurring 16 times per day; they are described in the thermal analysis section above.

The individual analysis results obtained in the previous sections were used as inputs to the profile, and the duration and frequency each are applied to the PWA are specified in the life cycle profile.

## Monte Carlo Analysis

One feature of the CALCE SARA PWA software has is the ability to run a Monte Carlo simulation to probabilistically determine the lifetimes of each of the failure modes (discussed in the next section). A distribution set can be specified for variables of interest in order to account for uncertainty introduced by the assumptions used to create the analysis models. For this study, all resultant temperatures are allowed to vary +/-5°C uniformly around the expected temperature values resulting in the thermal models. This distribution set is defined in the lifecycle profile segment, but is not implemented until the failure analysis is run.

There are 2 cases that have been created to compare the effective life of the PWB under study in low earth orbit thermal cycles after undergoing qualification testing during I&T and random vibrations due to launch conditions.

The difference in the two cases is the cold cycle of the LEO thermal profile:

- Case 1 does not consider active thermal controls on the PWA and allows it to attain its natural steady state temperature based on its steady state boundary conditions.
- Case 2 employs the necessary boundary temperature conditions that do not allow the board temperature to drop below 20°C, which is a typical thermostat setting for a Kapton heater.

Apart from this, the life cycles are defined similarly with identical qualification testing, on-orbit temperature cycle frequencies and dwell times.

### 1.1.15 Lifecycle Case 1: No Active Board Heating on Cold Side of LEO

The lifecycle profile is defined below in Figure 32:

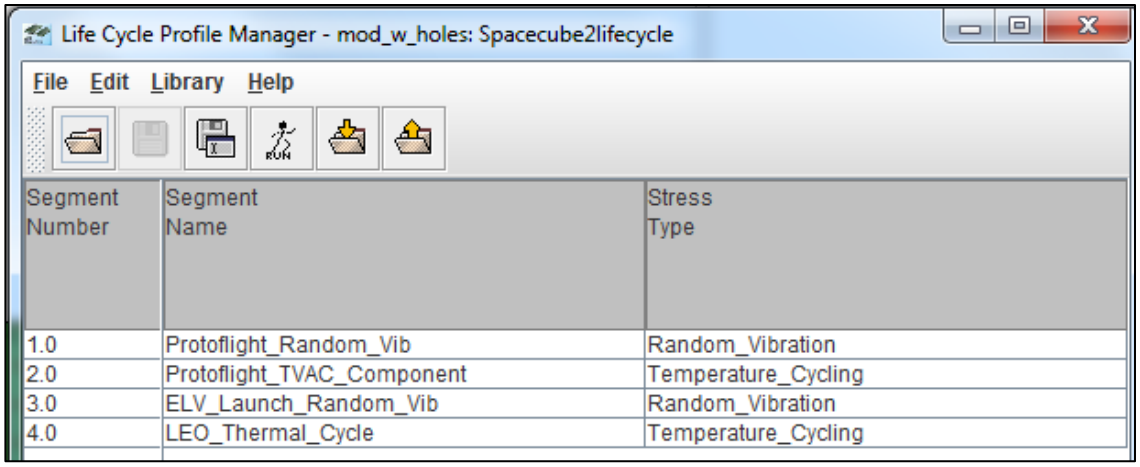



*Figure 32. Life cycle profile for Case 1; LEO with no active board heating.*

The CALCE software then performs what amounts to a review of the information provided to it from the input process and determines which failure models it is able to perform. Figure 33 shows the results of the screening and the failure models it will run.

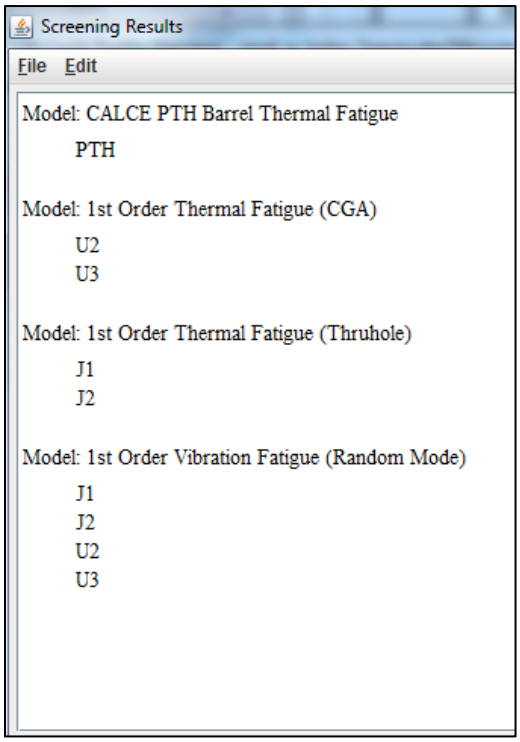
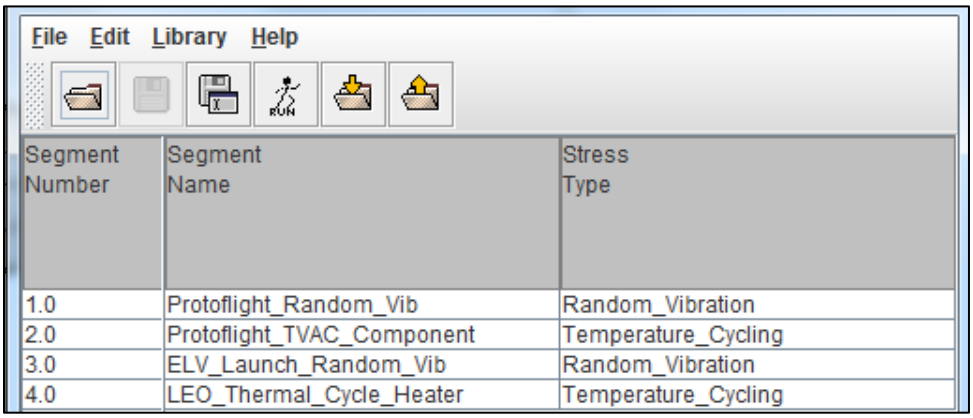



*Figure 33. Failure model screening results from CALCE SARA PWA.*

### 1.1.16 Lifecycle Case 2: Active Board Heating With Thermostatically Controlled Heaters on Cold Side of LEO




| Segment Number | Segment Name | Stress Type |
|---|---|---|
| 1.0 | Protoflight_Random_Vib | Random_Vibration |
| 2.0 | Protoflight_TVAC_Component | Temperature_Cycling |
| 3.0 | ELV_Launch_Random_Vib | Random_Vibration |
| 4.0 | LEO_Thermal_Cycle_Heater | Temperature_Cycling |

*Figure 34. Life cycle profile for Case 2; LEO with active board heaters maintaining 20°C on the cold side of orbit.*

## Failure Analysis Results

### 1.1.17 Case 1 Failure Modes and Lifetimes

Figure 35 shows the results of 2000 Monte Carlo runs given the specified life cycle and the distribution sets discussed previously. Notice that the top failure mode is an open solder joint on the U2 and U3 components in under 60 days on-orbit (16 orbits per day). This is the 1% failure life of that failure mode given the cumulative damage of the life profile. The red cells show that the components do not meet the stated life criteria (1% failure at 5 years). The remaining failure modes and components do meet that criteria. The information shown under Figure 35 is the numerical details of the on-orbit portion of the "U2-solder-open" failure mode, including the 2000 individual life time estimates. That data is not shown here but summarized in the data analysis sections.

In Figure 35, the information under the "Damage Criteria" column shows the 1% failure duration (discussed above) as well as the DR, or damage ratio which sums the damage across the applicable life cycle phases. This should be less than 1 for the lifecycle if it is to meet the criteria.

The damage ratio shown is an evaluation of the failure mechanism evaluated by the model, for the selected failure site, under the defined condition of the load segment will be for the specified ***Desired percent failure***. Note: this damage ratio is used with complimentary failure model evaluation results in a Palmgren-Miner approach to determine the total damage due to the applied life cycle profile. (University of Maryland, College Park, MD, 2014)

In its current configuration, the analysis results indicate that it is extremely unlikely that this board can attain its desired reliability goal at 5 years.

Results

| SNo. | Site-Mode | #Eval | Prime Failure Model | Damage Criteria | |
|---|---|---|---|---|---|
| 1 | U2-solder-open | 2 | 1ST_TF_CGA | 56.39 days (DR:31.52) | View |
| 2 | U3-solder-open | 2 | 1ST_TF_CGA | 59.12 days (DR:30.08) | View |
| 3 | J1-solder-open | 2 | 1ST_TF_TH | 8.14 years (DR:0.61) | View |
| 4 | J2-solder-open | 2 | 1ST_TF_TH | 8.58 years (DR:0.58) | View |
| 5 | PTH-barrel-open | 2 | CALCE_PTH | > 30 years (DR:0.05) | View |
| 6 | J1-interconnect-open | 2 | 1ST_VF_RM | > Specified (DR:0.00) | View |
| 7 | J2-interconnect-open | 2 | 1ST_VF_RM | > Specified (DR:0.00) | View |
| 8 | U2-interconnect-open | 2 | 1ST_VF_RM | > Specified (DR:0.00) | View |
| 9 | U3-interconnect-open | 2 | 1ST_VF_RM | > Specified (DR:0.00) | View |

*Figure 35. Failure modes of Case 1 components.*

**First Order Thermal Fatigue Model for Column Grid Array (1% Failure at 5 Years at LEO)**

Part Id: U2
Condition Name: LEO_Thermal_Cycle
Conditon Number: 4
*Cycles To Failure:* *928*
Damage Ratio: 31.495921
Distribution Type: MonteCarlo

Value Reported is (1E0) Percent Failure
MC Sample Size: 2000
MC Mean: 2540.320303
MC Standard Dev.: 755.949283
MC Min: 728.763135
MC Max: 5182.530790

## Problem Information

Package Factor: 1.000000
Package Length: 45.000000 mm
Package Width: 45.000000 mm
Interconnect Span X: 41.000000 mm
Interconnect Span Y: 41.000000 mm
Joint Height: 0.010252 mm
Package CTE: 5.63805e-006 1/°C
Board CTE: 1.473067e-005 1/°C

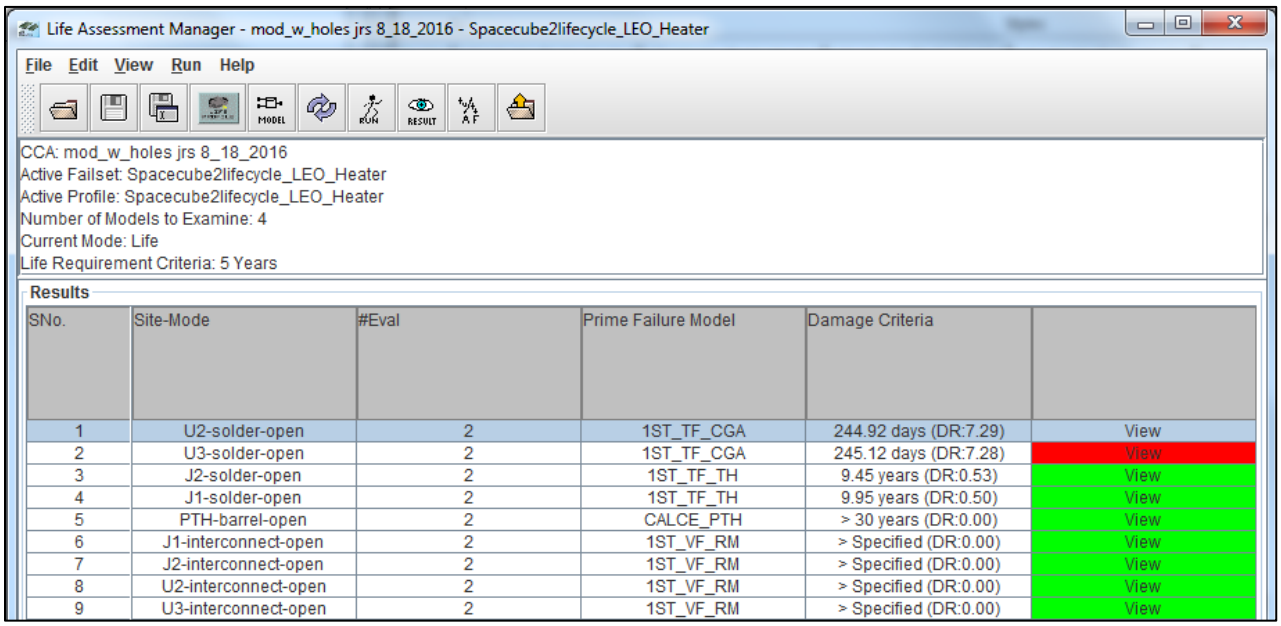
## Stress Condition

Max Package Temperature: 61.257082 °C

| | |
|---|---|
| Max Board Temperature: | 61.142716 °C |
| Min Package Temperature: | -20.2899 °C |
| Min Board Temperature: | -18.753 °C |
| Average Temp: | 22.786865 °C |
| Dwell Time: | 22.000000 min |

### 1.1.18 Case 2 Failure Modes and Lifetimes

Figure 36 shows the failure modes and 1% failure lives for the case that includes limiting the low temperature on-orbit to 20°C through the use of board heaters. It can be seen that the U2 and U3 solder-open failure modes still govern, and still do not meet minimum life criteria, but have improved failure lives by roughly 4 times the duration over Case 1. The reduction in temperature differential lowers the strains experienced by the solder joints, and is also seen with the other failure models.




| SNo. | Site-Mode | #Eval | Prime Failure Model | Damage Criteria | |
|---|---|---|---|---|---|
| 1 | U2-solder-open | 2 | 1ST_TF_CGA | 244.92 days (DR:7.29) | View |
| 2 | U3-solder-open | 2 | 1ST_TF_CGA | 245.12 days (DR:7.28) | View |
| 3 | J2-solder-open | 2 | 1ST_TF_TH | 9.45 years (DR:0.53) | View |
| 4 | J1-solder-open | 2 | 1ST_TF_TH | 9.95 years (DR:0.50) | View |
| 5 | PTH-barrel-open | 2 | CALCE_PTH | > 30 years (DR:0.00) | View |
| 6 | J1-interconnect-open | 2 | 1ST_VF_RM | > Specified (DR:0.00) | View |
| 7 | J2-interconnect-open | 2 | 1ST_VF_RM | > Specified (DR:0.00) | View |
| 8 | U2-interconnect-open | 2 | 1ST_VF_RM | > Specified (DR:0.00) | View |
| 9 | U3-interconnect-open | 2 | 1ST_VF_RM | > Specified (DR:0.00) | View |

*Figure 36. Failure modes and lives for Case 2, which uses board heaters to minimize temperature differential.*

**First Order Thermal Fatigue Model for Column Grid Array (1% at 5 Years at LEO)**

| | |
|---|---|
| Part Id: | U2 |
| Condition Name: | LEO_Thermal_Cycle_Htr |
| Conditon Number: | 4 |
| *Cycles To Failure:* | *4025* |
| Damage Ratio: | 7.259418 |
| Distribution Type: | MonteCarlo |

Value Reported is (1E0) Percent Failure

| | |
|---|---|
| MC Sample Size: | 2000 |
| MC Mean: | 19000.258988 |
| MC Standard Dev.: | 22493.345207 |
| MC Min: | 2137.162644 |
| MC Max: | 269699.253384 |

**Problem Information**

| | |
|---|---|
| Package Factor: | 1.000000 |
| Package Length: | 45.000000 mm |
| Package Width: | 45.000000 mm |
| Interconnect Span X: | 41.000000 mm |
| Interconnect Span Y: | 41.000000 mm |
| Joint Height: | 0.069803 mm |
| Package CTE: | 5.99599e-006 1/°C |
| Board CTE: | 1.473067e-005 1/°C |

**Stress Condition**

| | |
|---|---|
| Max Package Temperature: | 59.965828 °C |
| Max Board Temperature: | 60.677842 °C |
| Min Package Temperature: | 30.931090 °C |
| Min Board Temperature: | 24.199484 °C |
| Average Temp: | 45.255775 °C |
| Dwell Time: | 22.000000 min |

# Processor Card Analysis

### 1.1.19 Case 3: Thermal Vacuum Testing of Unpowered Board

A life profile was created to simulate the thermal cycling test being performed by the SpaceCube project in a GSFC thermal vacuum chamber. The board was populated with the U2 and U3 FPGAs and J1 and J2 cPCI connectors, and cycled in a thermal chamber from -55 ºC to 100 ºC at a rate of 3 ºC/minute and 30 minute dwell times. All components were unpowered.

The results of the Monte Carlo simulation using the same distribution set as in Case 1 and 2 are provided in Figure 37. The same solder open failure modes on U2 and U3 govern, and the damage ratio is based on specified lifetime of 10000 cycles at 1% failure. The number of cycles is not based on any criteria; it was specified to obtain the 2000 Monte Carlo lifetime data points which are discussed in a later section.

At the time of this writing, the thermal vacuum testing conducted by the Space Cube project at the stated thermal ambient conditions has resulted in a single failure of the test at 364 cycles. This value falls below the Monte Carlo mean given below but above the 1% failure life. This will be discussed further in the data analysis section below.

A possibility for this case is using it as an accelerated test to evaluate the fidelity of the CALCE SARA PWA model, but more than a single failure would be required to do so.

Results

| SNo. | Site-Mode | #Eval | Prime Failure Model | Damage Criteria | |
|---|---|---|---|---|---|
| 1 | U3-solder-open | 1 | 1ST_TF_CGA | < Specified (DR:53.03) | View |
| 2 | U2-solder-open | 1 | 1ST_TF_CGA | < Specified (DR:52.92) | View |
| 4 | J1-solder-open | 1 | 1ST_TF_TH | > Specified (DR:0.62) | View |
| 5 | J2-solder-open | 1 | 1ST_TF_TH | > Specified (DR:0.61) | View |
| 3 | PTH-barrel-open | 1 | CALCE_PTH | > Specified (DR:0.97) | View |

*Figure 37. Unpowered thermal vacuum chamber simulation results. Lives and damage ratios are based on cycles rather than days on-orbit.*

**First Order Thermal Fatigue Model for Column Grid Array (Thermal Vacuum Testing -55°C to 100°C )**

Part Id: U3

Condition Name: temp_cycling

Conditon Number: 1

Cycles To Failure: 189

Damage Ratio: 53.033767

Damage: 5.303377e+001

Distribution Type: MonteCarlo

Value Reported is (1E0) Percent Failure

MC Sample Size: 2000

| | |
|---|---|
| MC Mean: | 450.372406 |
| MC Standard Dev.: | 99.540484 |
| MC Min: | 158.202369 |
| MC Max: | 680.152022 |

Problem Information

| | |
|---|---|
| Package Factor: | 1.000000 |
| Package Length: | 45.000000 mm |
| Package Width: | 45.000000 mm |
| Interconnect Span X: | 41.000000 mm |
| Interconnect Span Y: | 41.000000 mm |
| Joint Height: | 0.054951 mm |
| Package CTE: | 5.86013e-006 1/°C |
| Board CTE: | 1.473067e-005 1/°C |

Stress Condition

| | |
|---|---|
| Max Package Temperature: | 100.865914 °C |
| Max Board Temperature: | 102.426342 °C |
| Min Package Temperature: | -55.5629 °C |
| Min Board Temperature: | -54.3419 °C |
| Average Temp: | 22.500000 °C |
| Dwell Time: | 30.000000 min |

# Analysis of the Monte Carlo Data

Since it was the governing failure mode for each of the 3 life cycle cases, the resulting ranges of the "solder open" failure lives of the U2 and U3 components were further analyzed to determine how well the failure data fit within a commonly used reliability distribution. Histograms of the data (Monte Carlo critical values are summarized in Sections 11 and 12) are shown below in Figure 38. Visual inspection shows the resulting histograms do not generally have the same characteristic shapes, with the most obvious

difference being the skew of each. The data in the top histogram appears to have the most normally distributed data, but closer inspection reveals that it has a statistical tail at the higher failure lives.

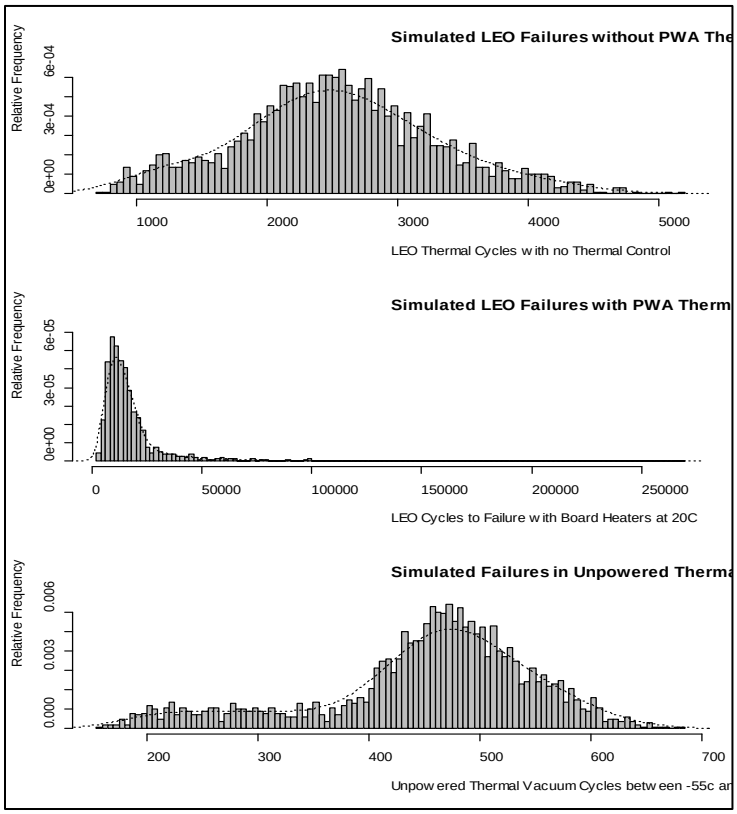



*Figure 38. Histograms of Monte Carlo lifetime data for U2 and U3 solder joint failures in thermal cycling. (R Core Team, 2016)*

## Fitting the Monte Carlo Lifetime Data to a Weibull Distribution

Hazard plots of the data were then generated to determine how well the data fit the Weibull distribution. A two parameter Weibull was plotted for each case as well as a 3 parameter Weibull plot utilizing a location parameter, $t_0$, which was taken as a potential failure free duration. The values of $t_0$ used were taken as the minimum values of the Monte Carlo data for each case. The resulting plots are shown below in Figure 39.

In the bottom row of plots, a single failure point resulting from a life test conducted at GSFC matching the design and thermal cycling conditions in the thermal vacuum test case (Case 3) is shown as a large red dot on the plotted points. This failure data from the testing may be helpful in validating the as-designed model, but more points would be required in order to adequately do so.

The fitted parameters are shown in the top left hand corner of each plot. The first column of plots are the Monte Carlo failure data fitted to a 2 parameter Weibull, and the second column of plots is the 3 parameter Weibull plot of the same data using the Monte Carlo minimum lives as the location parameters.

As can be seen in the plots, using the location parameter as failure free period does not improve the fit of the data for Cases 1 and 3, but does for the Case 2 data (LEO thermal conditions with active thermal control).

The data for Case 2 however does not have as strong a correlation as cases 1 and 3. Even with the improvement seen with using the location parameter (Abernethy, 3.4 Curved Weibulls & the t0 Correction, 1996), the $R^2$ only improves to around 0.87 with 2000 data points. In addition to that, the resulting curve maintains its concave down shape in both the 2 and 3 parameter forms. This could suggest that a lognormal model may be more appropriate (Abernethy, 3.5 Curved Weibulls & the Lognormal Distribution, 1996) to describe the Case 2 life model, but the correlation was not as strong as that of the Weibull fit. This case has some failure lives at extremely high life cycles which may have an effect on the data fit, but all data points were retained for the analysis, and further data manipulation is reserved for forward work.

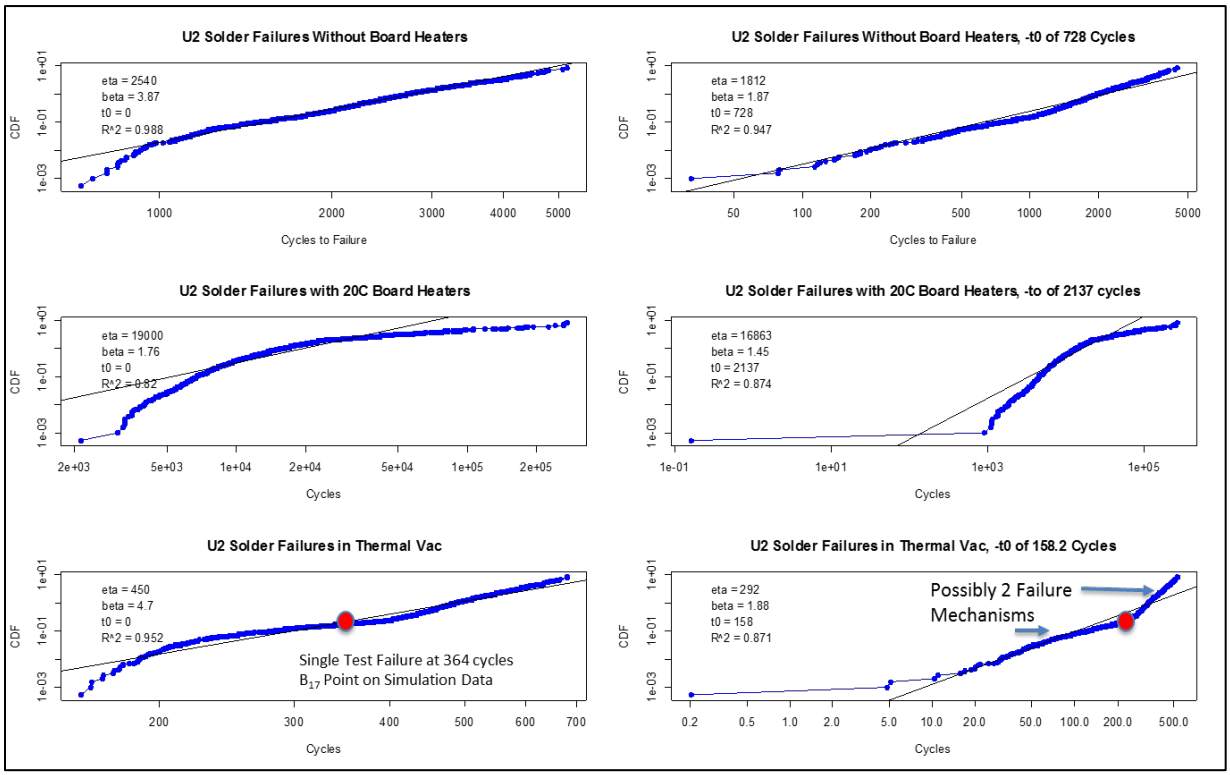



*Figure 39. 2 parameter and 3 parameter Weibull plots of the solder failures in U2 and U3. Each row of 2 plots represents the data from each of the 3 cases under study. (R Core Team, 2016)*

The resulting plots all indicate a wear out failure mode (beta term/ Weibull slope between 1.5 and 5) which seems to be logical for a thermal cycling fatigue analysis.

The resulting fitted parameters in cases 1 and 3 are consistent with an observed beta of approximately 4 (Engelmaier, 1991) for leadless or stiff leaded attachments.

The beta of 1.76 (1.45 with a $t_0$/location factor of 2137 cycles) in case 2 is more indicative of components with compliant leads, having a typical observed beta of approximately 2 (Engelmaier, 1991), and may actually be due more in part to the overall lower stress levels from to the reduced LEO temperature cycle differential rather than increased compliance since the design has not changed between cases.

After the original analysis was completed for the as-designed PWA configuration, select board parameters were modified to observe sensitivities to expected life. These included the overall board thickness, dielectric material, and the joint bond area, and are discussed in section 14 below.

# Thermal Cycling Sensitivity Analysis

To better explore the parameters that affect the reliability of the SpaceCube Processor Card, a sensitivity analysis was performed on the test case with the unpowered board in TVAC (Case 3 above). The objective was to identify potential design/reliability improvements by varying materials and geometries. A Monte Carlo distribution was not used in this subset; instead, the mean cycles to failure was used to gauge relative reliability. The screening results of the failure analysis included PTH Barrel Thermal Fatigue, First Order Thermal Fatigue for the CGAs, and First Order Thermal Fatigue for the cPCI through-holes. However since the CGA and PTH were dominant failure modes, the cPCI through-hole failure modes were considered negligible and is not discussed in this section.

## Thermal Cycling Life Analysis Results, As-Designed Baseline

The baseline results for the sensitivity analysis of Case 3 are shown below.

**CALCE PTH Barrel Thermal Fatigue Barrel Failure**

| | |
|---|---|
| Part Id: | PTH |
| Condition Name: | temp_cycling |
| Conditon Number: | 1 |
| *Cycles To Failure:* | *9624* |
| Damage Ratio: | 0.103907 |
| Delta T: | 155.00 K |
| Stress in plating: | 4.355740e+004 |
| Strain in plating: | 3.430108e-003 |

(Stress value is in Pa.)

# First Order Thermal Fatigue Model For Column Grid Array

| | |
|---|---|
| Part Id: | U2 |
| Condition Name: | temp_cycling |
| Conditon Number: | 1 |
| *Cycles To Failure:* | *473* |
| Damage Ratio: | 21.138780 |
| *Damage:* | *2.113878e+001* |

## Strain information

| | |
|---|---|
| Ld: | 1.000170 |
| Strain Range: | 0.038682 |
| Solder fatigue exponent: | -0.411770 |

## Problem Information

| | |
|---|---|
| Package Factor: | 1.000000 |
| Package Length: | 45.000000 mm |
| Package Width: | 45.000000 mm |
| Interconnect Span X: | 41.000000 mm |
| Interconnect Span Y: | 41.000000 mm |
| Joint Height: | 0.100000 mm |
| Package CTE: | 5.500000e-006 1/°C |
| Board CTE: | 1.473067e-005 1/°C |

## Stress Condition

| | |
|---|---|
| Max Package Temperature: | 100.000000 °C |
| Max Board Temperature: | 100.000000 °C |
| Min Package Temperature: | -55.000000 °C |
| Min Board Temperature: | -55.000000 °C |
| Average Temp: | 22.500000 °C |
| Dwell Time: | 30.000000 min |

**Messages:**

*Using Leadless Approximation. Estimates below 1000 cycles may be invalid.*

# First Order Thermal Fatigue Model For Insertion Mount PGA Packages

| | |
|---|---|
| Part Id: | J1 |
| Condition Name: | temp_cycling |
| Conditon Number: | 1 |
| *Cycles To Failure:* | *29881* |
| Damage Ratio: | 0.033466 |
| Strain: | 7.02E-3 |
| Solder Max Stress: | 5.05E6 Pa |
| Board Type: | Plated |
| Local Stress: | 2.36E6 Pa |

## Lead Geometry

| | |
|---|---|
| Lead Modulus: | 1.206625e+005 MPa |
| Lead Poisson's Ratio: | 3.500000e-001 |
| Lead K11: | 5.455623e+006 N/m |
| Lead K22: | 1.391221e+007 N/m |
| Lead K33: | 3.013276e+007 N/m |

## Package Information

| | |
|---|---|
| Connection Type: | Plated |
| Package Thickness: | 11.000000 mm |
| Package E: | 1.590000e+004 MPa |
| Package CTE: | 1.500000e-005 1/°C |

## Board Information

| | |
|---|---|
| Board Thickness: | 2.872740 mm |
| Board E : | 6.757650e+004 MPa |
| Board CTE: | 1.473067e-005 1/°C |
| Board CTE(Z): | 4.955703e-005 1/°C |

## Cycle Information

| | |
|---|---|
| Max Package Temperature: | 100.000000 °C |
| Max Board Temperature: | 100.000000 °C |
| Min Package Temperature: | -55.000000 °C |
| Min Board Temperature: | -55.000000 °C |

## Thermal Cycling Life Analysis, Variable Board Thickness

The first variable explored was the dielectric thickness. The processor card has a larger stack-up for a PCB design, and so a slight change in dielectric thickness multiplied across the 22 layers would noticeably change the overall board thickness. Thicker boards produce higher stresses in the PTH; finite element analysis (FEA) performed by Intel Corporation showed that a 20% increase in overall board thickness resulted in an 8~30% increase in the copper layer stress for plated through holes (Goyal, Azimi, Chong, & Lii, 1997).

To understand the effects of the dielectric thickness on this assembly, each layer was both increased and reduced by 0.5 mils (0.0127 mm). The resultant overall board thickness was changed by 10.5 mils (0.2667 mm). The results are summarized in the table below.

*Table 7. Life Analysis, Variable Board Thickness.*

| | Datum (As designed) | Dielectric+0.5 mils | Dielectric-0.5 mils |
|---|---|---|---|
| **Board thickness [mm]** | 2.873 | 3.139 | 2.606 |
| **Board elastic modulus [Pa]** | 6.7577e+004 | 6.5394e+004 | 7.0020e+004 |
| **Board CTE (X&Y) [1/ºC]** | 1.4731e-005 | 1.4638e-005 | 1.4834e-005 |
| **Strain Range** | 0.0387 | 0.0383 | 0.0391 |
| **Cycles to Failure, FPGA** | 473 | 485 | 460 |
| **Cycles to Failure, PTH** | 9624 | 9131 | 10260 |

As expected, the cycles to failure for the PTH was lowered with an increase in dielectric. However the change in the FPGA reliability was much less noticeable. The CALCE-derived elastic modulus and lateral CTE of the board decreased as the dielectric was increased.

## Thermal Cycling Life Analysis, Variable Board Material

The next variable of interest was the dielectric material. The processor card had been fabricated with a high-reliability polyimide material in ISOLA P95. To compare, an epoxy fiberglass material from the CALCE library (pwb.epoxyF) was chosen, as well as a manually-created material to replicate Arlon 85NT polyimide. (See Table 8 for comparison of all material properties.) The Arlon 85NT material is reinforced with aramid, which helps to control the in-plane expansion and reduces the strain at the solder joint interconnects. However it's greater Z-axis expansion lends to less PTH barrel life.

*Table 8. Life Analysis, Variable Board Material.*

| | Isola P95 | Epoxy Fiberglass | Arlon 85NT |
|---|---|---|---|
| **Dielectric elastic modulus [MPa]** | 26834 | 17200 | 22063 |
| **Dielectric CTE (X&Y) [1/ºC]** | 13 | 17.6 | 9 |
| **Dielectric CTE (Z) [1/ºC]** | 55 | 70 | 93 |
| **Board elastic modulus [Pa]** | 6.7577e+004 | 6.8720e+004 | 6.9966e+004 |
| **Board CTE (X/Y) [1/ºC]** | 1.4731e-005 | 1.7302e-005 | 1.2873e-005 |
| **Cycles to Failure, FPGA** | 473 | 260 | 816 |
| **Cycles to Failure, PTH** | 9624 | 3576 | 1054 |

The epoxy material is greatly outperformed by the design-selected ISOLA P95 polyimide dielectric, given superior control of the expansion in both the lateral and out-of-plane directions. However, the Arlon 85NT exhibited better performance for the FPGA interconnect, although trading lower performance for the PTH.

For potential future redesigns or rebuilds of this PWA, a change in the dielectric material to better control the X&Y expansion is worth consideration, as seen in these results.

## Thermal Cycling Life Analysis, Solder Joint Bond Area

To further examine the FPGA columns, the failure site in question, the solder joint bond area was selected as a parameter of interest. The baseline simulated area was defined by the manufacturer-recommended solder land area for the FPGA, however reductions could exist given variability in manufacturing. The area was reduced by 10% and 20%, and also increased by 10% for comparison.

*Table 9. Life Analysis, Solder Joint Bond Area.*

| | As Designed Area | 10% Reduction | 20% Reduction | 10% Increase |
|---|---|---|---|---|
| **Solder joint bond area [mm$^2$]** | 0.385 | 0.3465 | 0.308 | 0.4235 |
| **Strain Range** | 0.0387 | 0.0430 | 0.0484 | 0.352 |
| **Cycles to Failure, FPGA** | 473 | 366 | 275 | 596 |

As expected, the reduction at the solder joint significantly decreased the estimated life. Given the same forces exerted on the solder joint from the thermal expansion mismatch between the laminate material, copper pads, and part body, the reduced area would increase the stress in the solder and accelerate the fatigue failure.

# Conclusions

Given the outputs of the various on-orbit cases, and that the single thermal life test failure result falls within the simulated thermal vacuum data, it would seem reasonable that the CALCE SARA PWA model of the SpaceCube processor created in this study could be a predictor of the estimated lifetime in low earth orbit.

More actual failure data would be required to validate the model, but given that the predicted lifetime is so much lower than the needed life at 1% failure, it may be more cost effective to step back and look at other material combinations prior to performing additional testing in the current design configuration.

If the model described above is a reasonable predictor, then changes to both the PWB materials and the thermal design should be implemented in order to attain the desired reliability at the maximum designated mission life per NASA NPR 8705.4.

A trade study should be conducted to specify a board material that more closely matches coefficients of thermal expansion between the column grid array component chip carriers and the PWB material, and should be mindful of introducing other failure modes that compromise the desired reliability, such as a plated through hole failure. The CALCE SARA PWA software tool can be helpful in providing insight into the various trades.

# References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