National Aeronautics and
Space Administration

High-Performance Spaceflight Computing (HPSC) Program Overview

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Acronym List

AFRL	Air Force Research Laboratory	GB/s	Gigabytes Per Second	RTOS	Real Time Operating System
AMBA	ARM Advanced Microcontroller Bus Architecture	GNC	Guidance Navigation and Control	S/C	Spacecraft
ASIC	Application Specific Integrated Circuit	GOPS	Giga Operations Per Second	SCP	Self Checking Pair
BW	Bandwidth	GSFC	Goddard Space Flight Center	SMD	Science Mission Directorate
CFS	Core Flight Software	HEOMD	Human Exploration and Operations Directorate	SpW	SpaceWire
CPU	Central Processing Unit	HPSC	High Performance Spaceflight Computing	SRAM	Static Random Access memory
C&DH	Command and Data Handling	JPL	Jet Propulsion Laboratory	SRIO	Serial RapidIO
DDR	Double Data Rate	KHz	Kilohertz	SSR	Solid State Recorder
DMR	Dual Modular Redundancy	Kpps	Kilo Packets Per Second	STMD	Space Technology Mission Directorate
DRAM	Dynamic Random Access memory	Mbps	Megabits Per Second	TTE	Time Triggered Ethernet
EEPROM	Electrically Erasable Programmable Read-Only Memory	MCM	Multi Chip Module	TTGbE	Time Triggered Gigabit Ethernet
FCR	Fault Containment Region	MRAM	Magnetoresistive Random Access Memory	TMR	Triple Modular Redundancy
FPGA	Field Programmable Gate Array	NASA	National Aeronautics and Space Administration	TRCH	Timing Reset Configuration and Health
FSW	Flight Software	NVRAM	Nonvolatile Random Access memory	XAUI	10 Gigabit Media Independent Interface)
Gb/s	Gigabits Per Second	PCB	Printed Circuit Board	VMC	Vehicle Management Computer

Outline

- HPSC Overview
- HPSC Contract
- Chiplet Architecture
- HPSC Middleware
- NASA HPSC Use Cases

High Performance Spaceflight Computing (HPSC) Overview

- The goal of the HPSC program is to dramatically advance the state of the art for spaceflight computing
- HPSC will provide a nearly two orders-of-magnitude improvement above the current state of the art for spaceflight processors, while also providing an unprecedented flexibility to tailor performance, power consumption, and fault tolerance to meet widely varying mission needs
- These advancements will provide game changing improvements in computing performance, power efficiency, and flexibility, which will significantly improve the onboard processing capabilities of future NASA and Air Force space missions
- HPSC is funded by NASA's Space Technology Mission Directorate (STMD), Science Mission Directorate (SMD), and the United States Air Force
- The HPSC project is managed by Jet Propulsion Laboratory, and the HPSC contract is managed by NASA Goddard Space Flight Center (GSFC)

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HPSC Background

- HPSC began with a NASA internal study, which identified several use cases for high performance spaceflight computing

Human Spaceflight (HEOMD) Use Cases	Science Mission (SMD) Use Cases
Cloud Services	Extreme Terrain Landing
Advanced Vehicle Health Management	Proximity Operations / Formation Flying
Crew Knowledge Augmentation Systems	Fast Traverse
Improved Displays and Controls	New Surface Mobility Methods
Augmented Reality for Recognition and Cataloging	Imaging Spectrometers
Tele-Presence	Radar
Autonomous & Tele-Robotic Construction	Low Latency Products for Disaster Response
Automated Guidance, Navigation, and Control (GNC)	Space Weather
Human Movement Assist	Science Event Detection and Response
	Immersive Environments for Science Ops / Outreach

- Following this study, a AFRL/NASA Next Generation Space Processor (NGSP) analysis program engaged industry to define and benchmark future multi-core processor architectures

- Based on the results of this program, the Government generated the conceptual reference architecture and detailed requirements for the HSPC “Chiplet”

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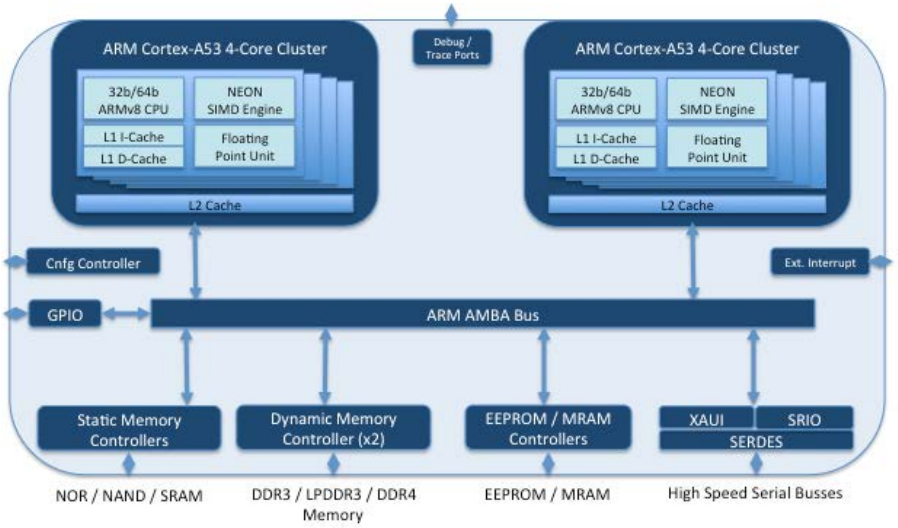
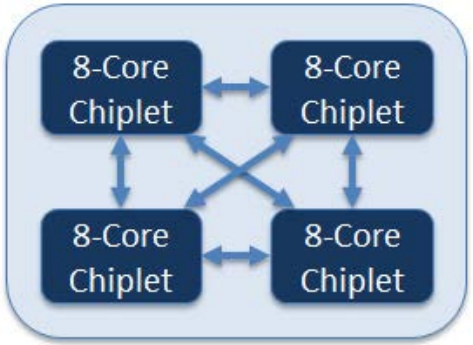
HPSC Background

- Reference design features power-efficient **ARM 64-bit processor cores (8)** and on-chip interconnects scalable **and** extensible in MCM (Multi-Chip Module) or on PCB (Printed Circuit Board) via XAUI and SRIO (Serial RapidIO) 3.1 high-speed links
  - Multi-Chiplet configurations (tiled or cascaded) provide increased processing throughput and/or increased fault tolerance (e.g. each Chiplet as separate fault containment regions, NMR)
  - Chiplets may be connected to other XAUI/SRIO devices
    - e.g. FPGAs, GPUs, or ASIC co-processors
- Supports multiple hardware-based and software-based fault tolerance techniques



HPSC "Chiplet" Reference Design



Multi-Chiplet Configuration

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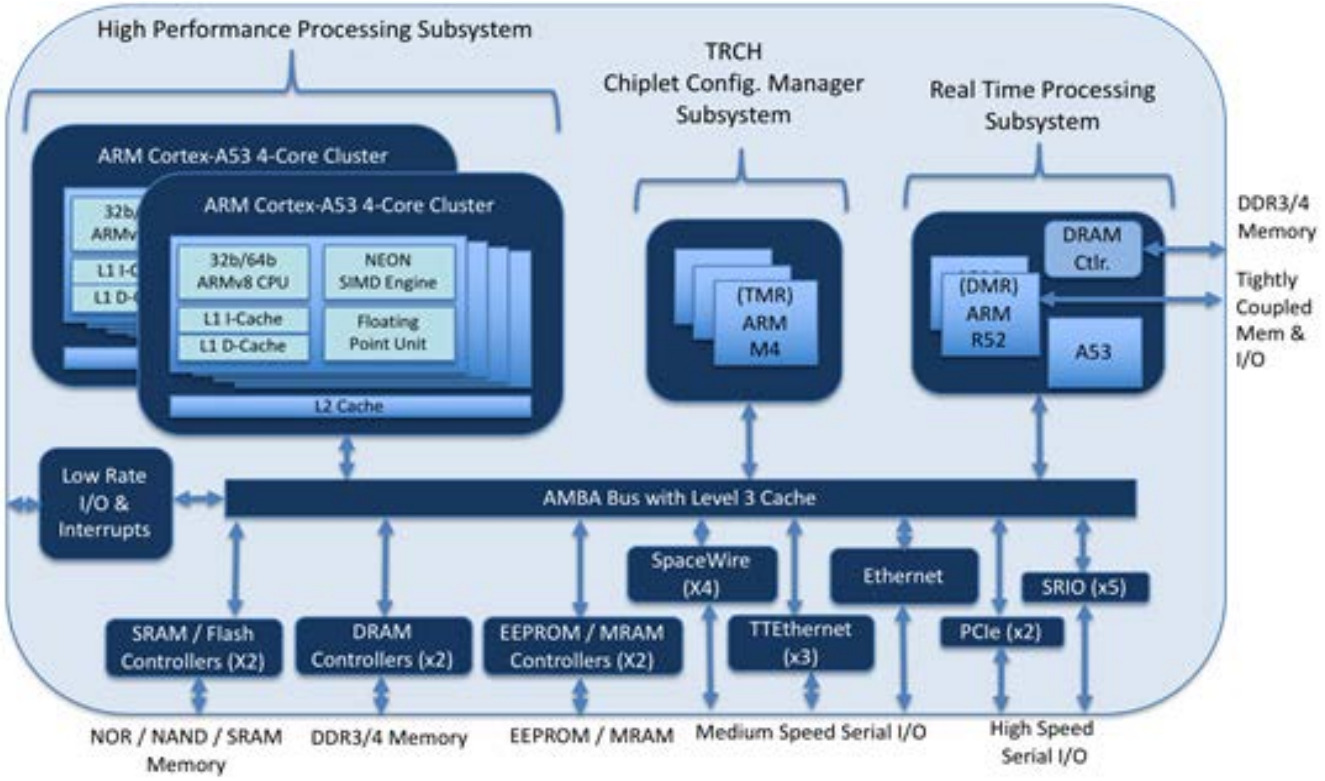
HPSC Contract

- Following a competitive procurement, the HPSC cost-plus fixed-fee contract was awarded to Boeing
- Under the base contract, Boeing will provide:
  - Prototype radiation hardened multi-core computing processors (Chiplets), both as bare die and as packaged parts
  - Prototype system software which will operate on the Chiplets
  - Evaluation boards to allow Chiplet test and characterization
  - Chiplet emulators to enable early software development
- Five contract options have been executed to enhance the capability of the Chiplet
  - On-chip Level 3 cache memory
  - Dual real-time processors
  - Dual Time Triggered Ethernet (TTE) interfaces
  - Dual SpaceWire interfaces
  - Package amenable to spaceflight qualification
- Contract deliverables are due April 2021

Chiplet Architecture

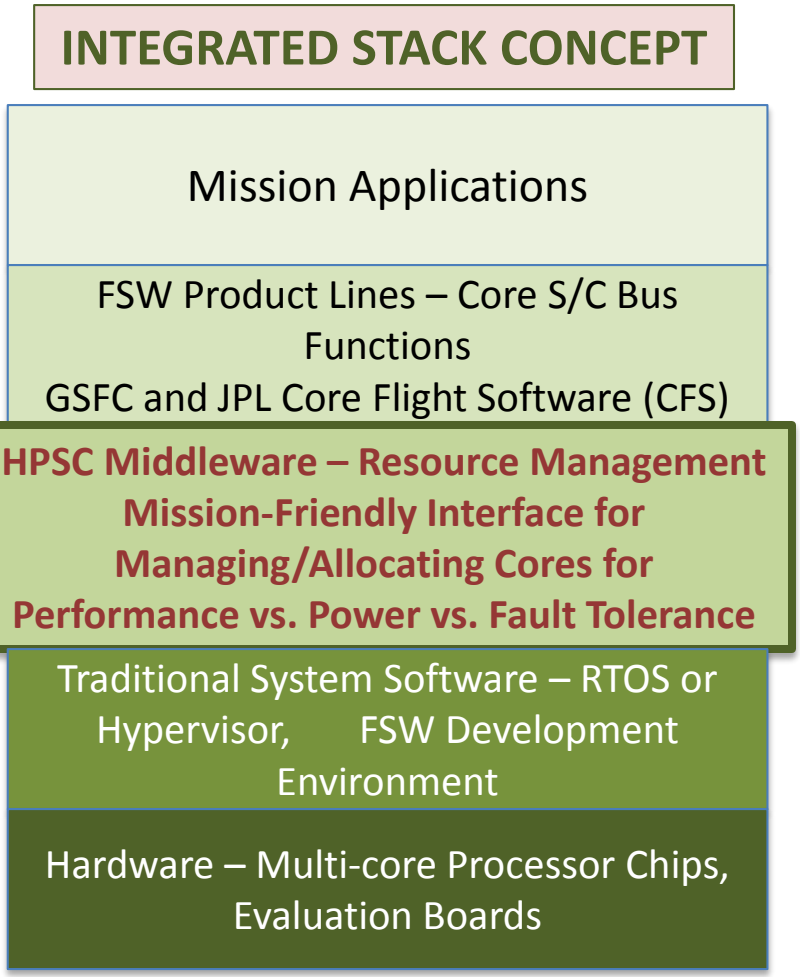
- With the contract options awarded and the preliminary design completed, the Chiplet architecture has evolved from the original reference architecture



HPSC Chiplet Architecture

HPSC Middleware

- AFRL is funding JPL and NASA GSFC to develop HPSC Middleware
- Middleware will provide a software layer that provides services to the higher-level application software to achieve:
  - Configuration management
  - Resource allocation
  - Power/performance management
  - Fault tolerance capabilities of the HPSC chiplet
- Serving as a bridge between the upper application layer and lower operating system or hypervisor, the middleware will significantly reduce the complexity of developing applications for the HPSC chiplet



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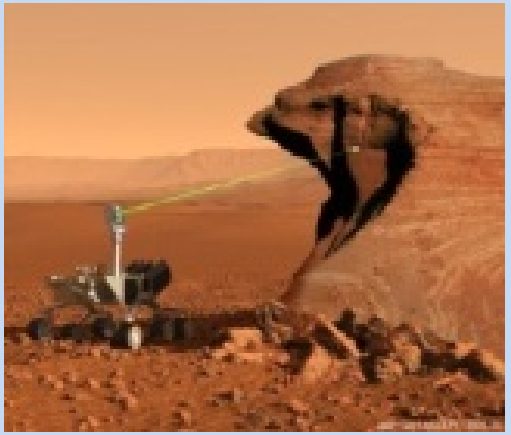
HPSC Use Cases

Rover

Compute Needs
- Vision Processing
- Motion/Motor Control
- GNC/C&DH
- Planning
- Science Instruments
- Communication
- Power Management
- Thermal Management
- Fault detection/recovery

- **System Metrics**
- 2-4 GOPs for mobility(10x RAD750)
- >1Gb/s science instruments
- 5-10GOPs science data processing
- >10KHz control loops
- 5-10GOPS, 1GB/s memory BW for model based reasoning for planning



Lander

Compute Needs
- Hard Real time compute
- High rate sensors w/zero data loss
- High level of fault protection/ fail over

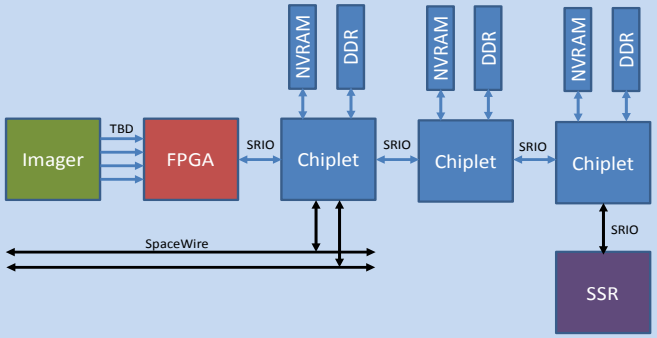
- **System Metrics**
- >10 GOPs compute
- 10Gb/s+ sensor rates
- Microsecond I/O latency
- Control packet rates >1Kpps
- Time tagging to microsecond accuracy

HPSC – High Bandwidth Instrument and SmallSats / Constellations Use Cases

High Bandwidth Instrument

Compute Needs
- Soft real time
- Non-mission critical
- High rate sensors
- Large calibration sets in NV memory

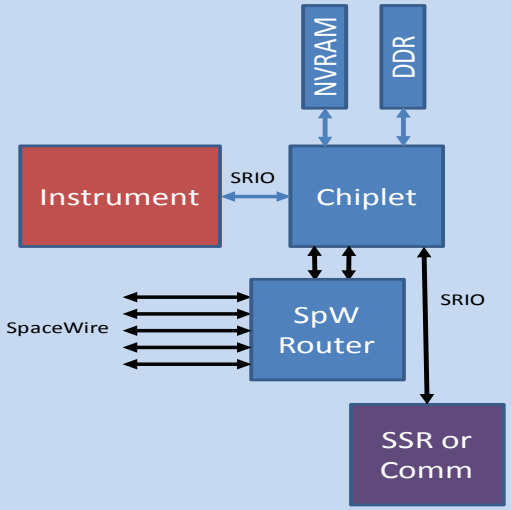
- **System Metrics**
- 10-20 GOPs compute
- >10GB/s memory bandwidth
- >20Gbps sensor IO data rates



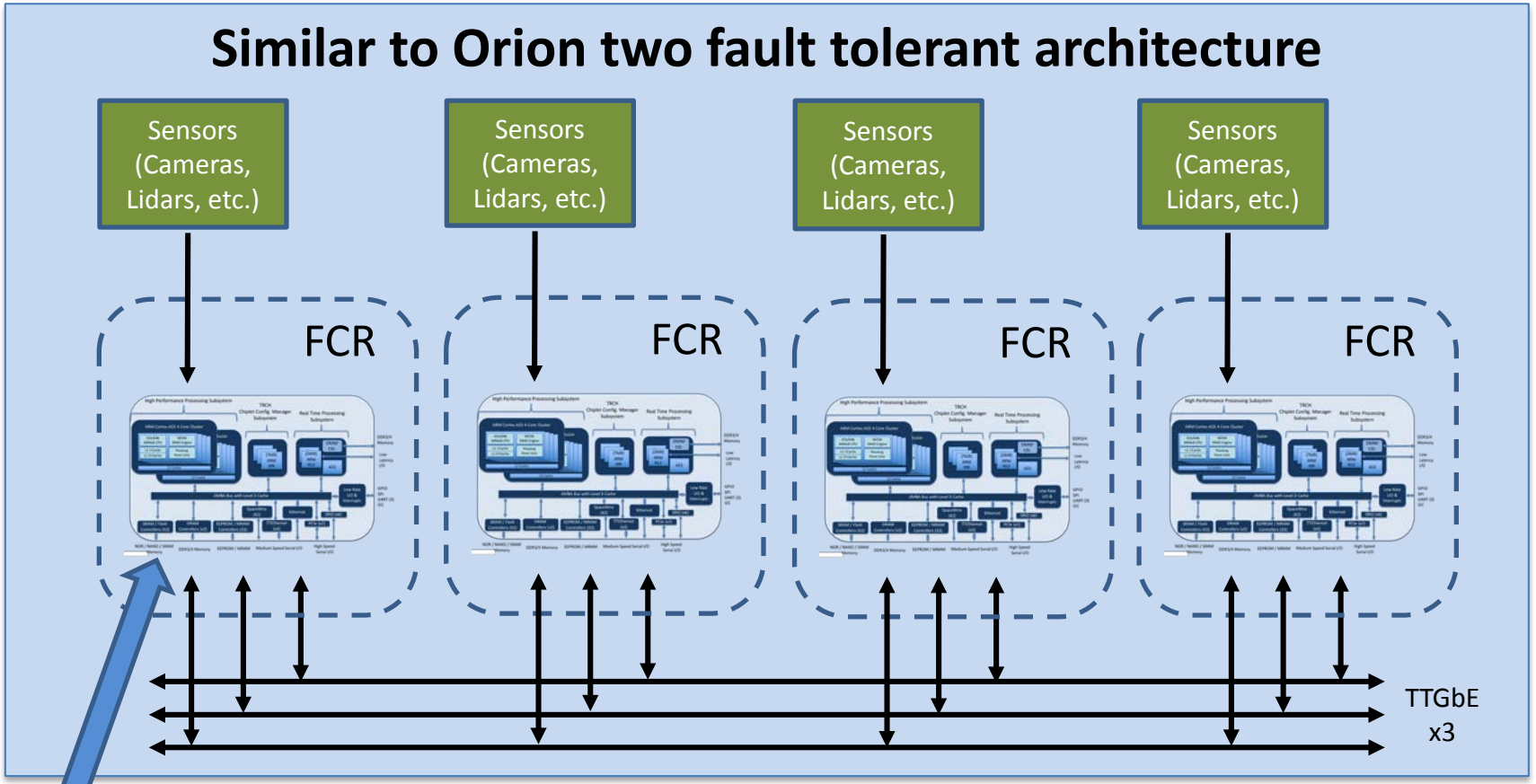
Smallsat

Compute Needs
- Hard and Soft real time
- GNC/C&DH
- Autonomy and constellation(cross link comm)
- Sensor data processing
- Autonomous science

- **System Metrics**
- 2-5Gbps sensor IO
- 1-10GOPs
- 1GB/s memory bandwidth
- 250Mbps cross link bandwidth



HPSC – HEO Habitat/Gateway Use Case



- A single HPSC exceeds the performance metrics of a Orion Vehicle Management Computer (VMC)
- A VMC contains three Self-Checking Pairs (SCP)

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Conclusion

- Future space mission scenarios call out for significantly improved spaceflight computing capability
- Improved spaceflight computing means enhanced computational performance, energy efficiency, and fault tolerance
- With the ongoing HPSC development, we are well underway to meeting future spaceflight computing needs
- The NASA-developed Middleware will allow the efficient infusion of the HPSC chiplet into those missions
- As illustrated by the NASA use cases, our future missions demand the capabilities of HPSC

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